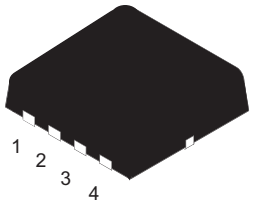
STL8N10F7

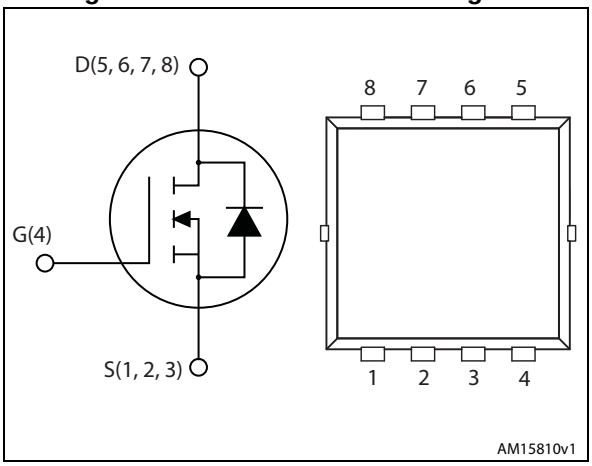
N-channel 100 V, 0.017 Ω typ., 35 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet - preliminary data



PowerFLAT™ 3.3 x 3.3

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STL8N10F7	100 V	0.02 Ω	35 A	50 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL8N10F7	8N10F	PowerFLAT™ 3.3 x 3.3	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	8	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	6	A
I_{DM} (1)(2)	Drain current (pulsed)	32	A
I_D (3)	Drain current (continuous) at T_{pcb} = 25 °C	35	A
I_D (3)	Drain current (continuous) at T_{pcb} = 100 °C	22	A
I_{DM} (2)(3)	Drain current (pulsed)	140	A
P_{TOT} (3)	Total dissipation at T_{case} = 25 °C	50	W
P_{TOT} (1)	Total dissipation at T_{pcb} = 25 °C	3.5	W
T_J	Operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature		°C

1. This value is rated according to $R_{thj\text{-}pcb}$.
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj\text{-}case}$.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	42.8	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA; V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS}= 0			1	µA
		V_{DS} = 100 V; V_{GS}= 0; T_C=125 °C			100	µA
I_{GSS}	Gate body leakage current	V_{GS} = 20 V; V_{DS}= 0			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 4 A		0.017	0.02	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =50 V, f=1 MHz, V_{GS}=0	-	1640	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD}=50 V, I_D = 8 A V_{GS} =10 V *Figure 14*	-	25	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=50 V, I_D= 4 A, R_G=4.7 Ω, V_{GS}= 10 V *Figure 13*	-	15	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	8	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 8 A, V_{GS}=0	-	-	1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD}=80 V, T_j=150 °C	-	53		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. Pulsed: pulse duration=300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

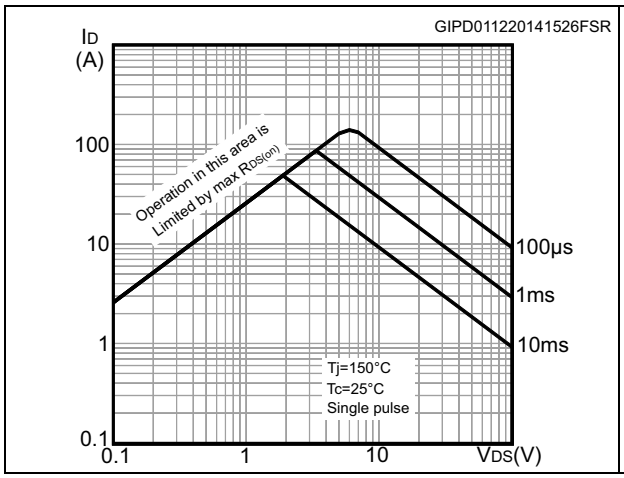


Figure 3. Thermal impedance

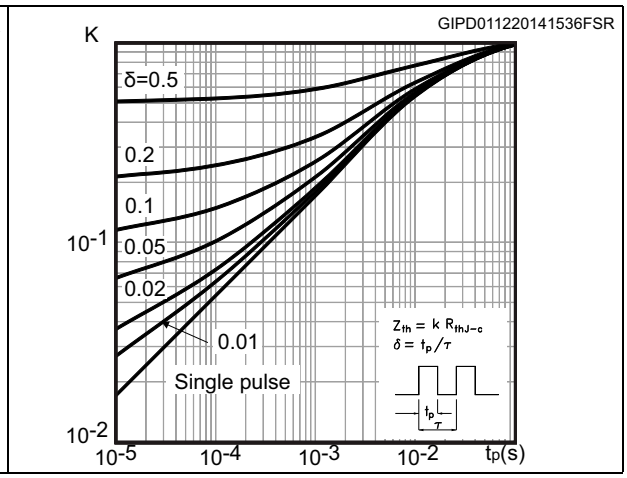


Figure 4. Output characteristics

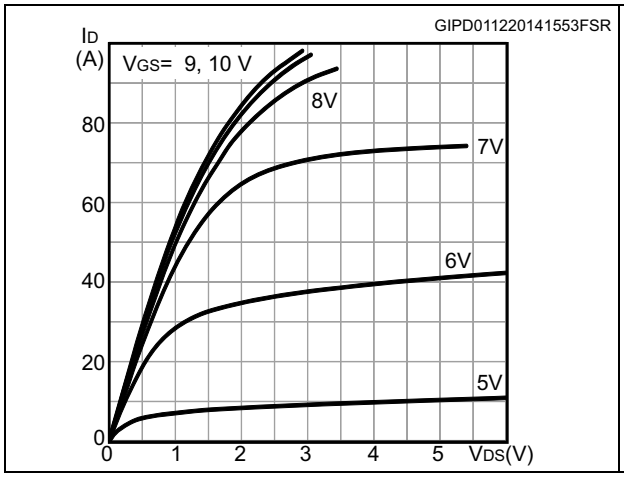


Figure 5. Transfer characteristics

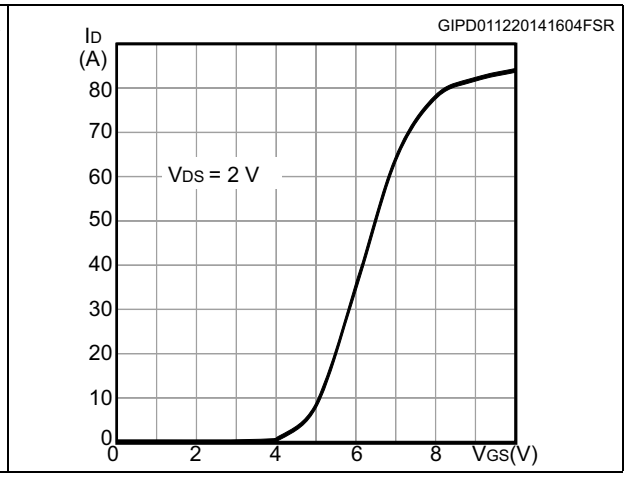


Figure 6. Normalized gate threshold voltage vs. temperature

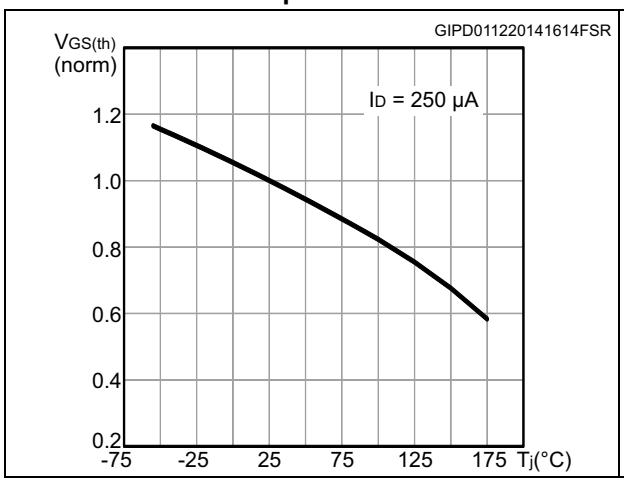


Figure 7. Normalized $V_{(BR)DSS}$ vs. temperature

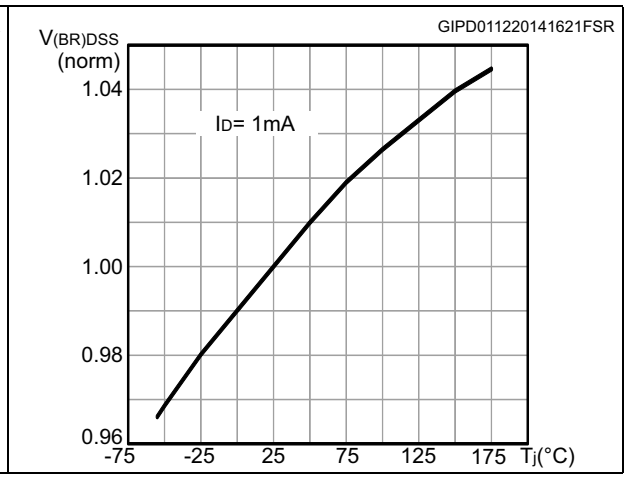


Figure 8. Static drain-source on-resistance

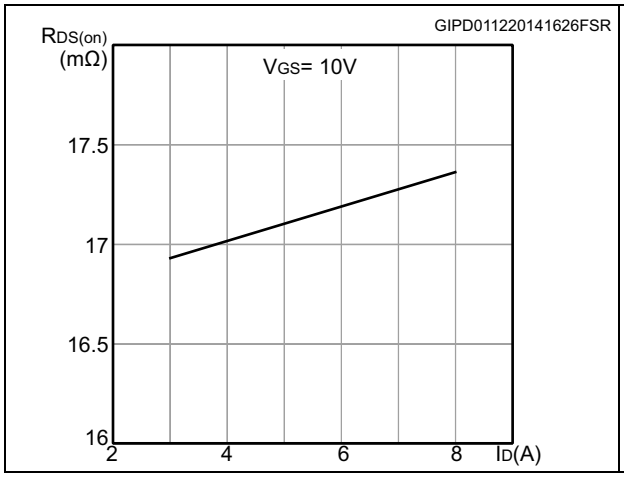


Figure 9. Normalized on-resistance vs. temperature

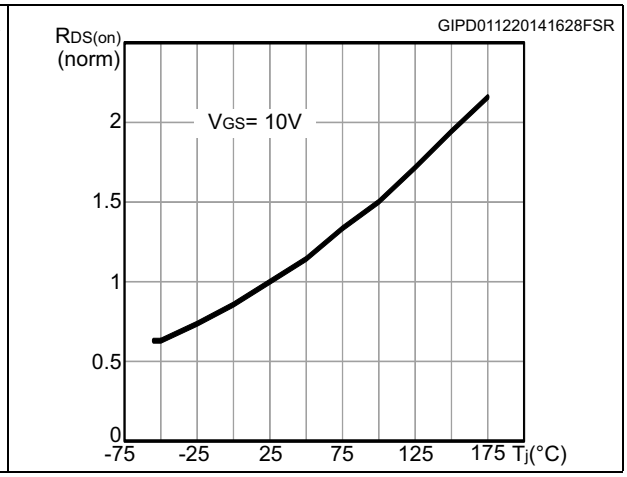


Figure 10. Gate charge vs. gate-source voltage

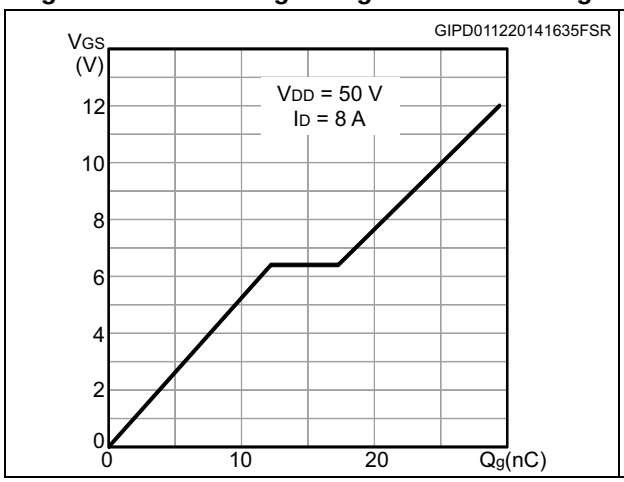


Figure 11. Capacitance variations

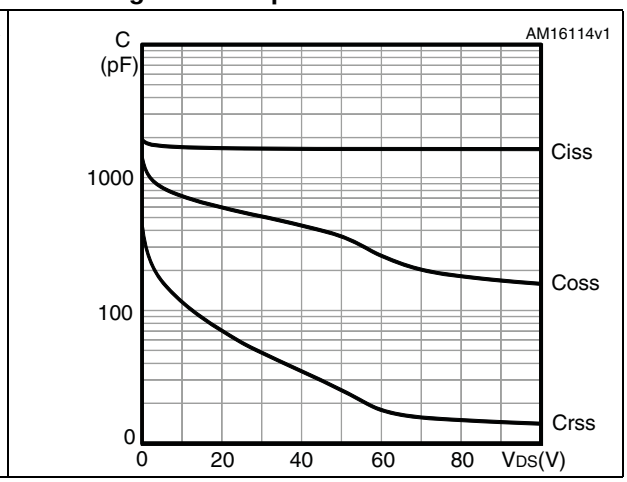
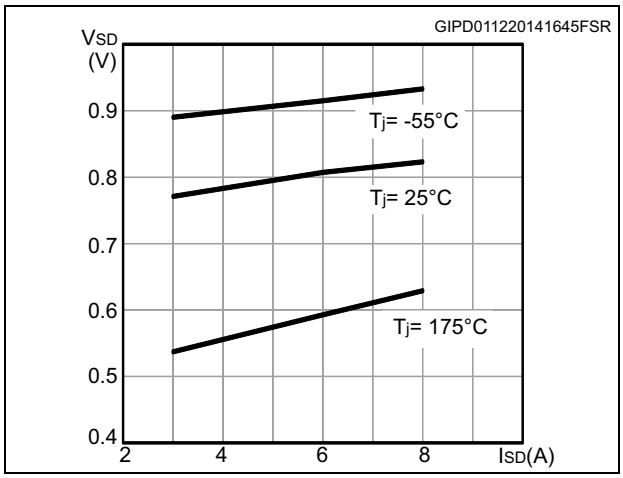


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

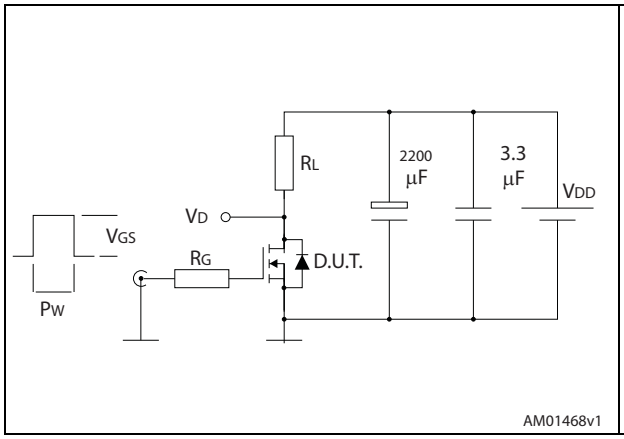


Figure 14. Gate charge test circuit

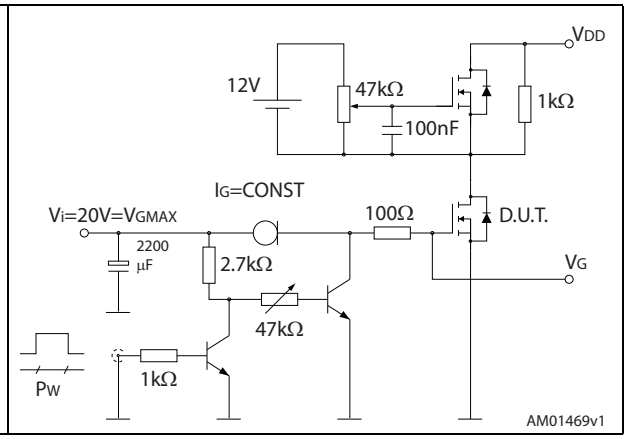


Figure 15. Test circuit for inductive load switching and diode recovery times

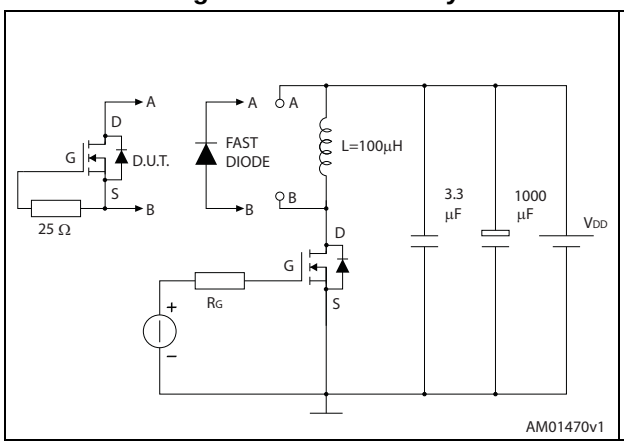


Figure 16. Unclamped inductive load test circuit

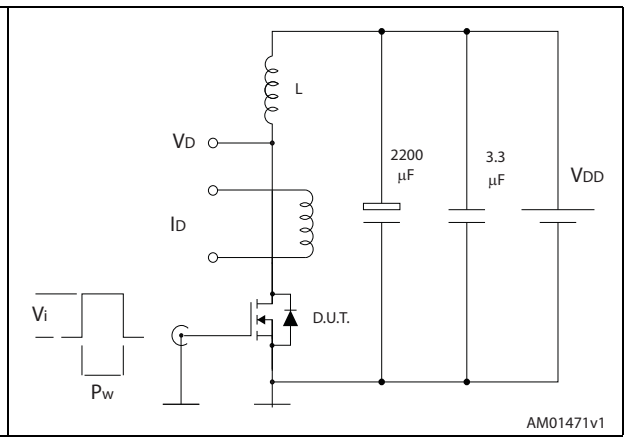


Figure 17. Unclamped inductive waveform

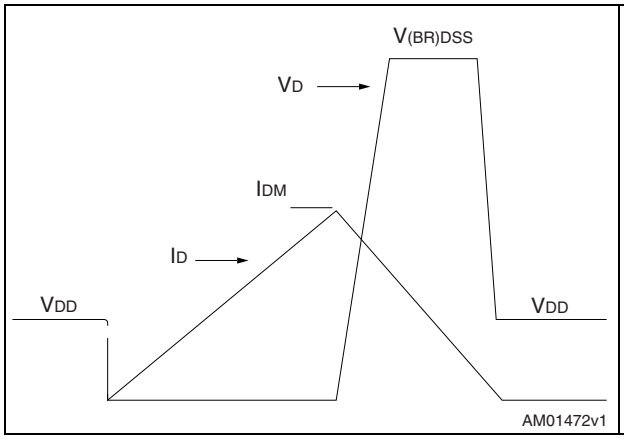
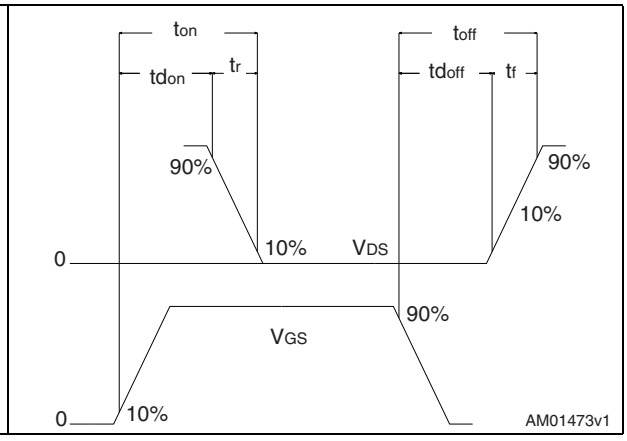


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 8.PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
ϑ	8°	10°	12°

Figure 19. PowerFLAT™ 3.3 x 3.3 drawing

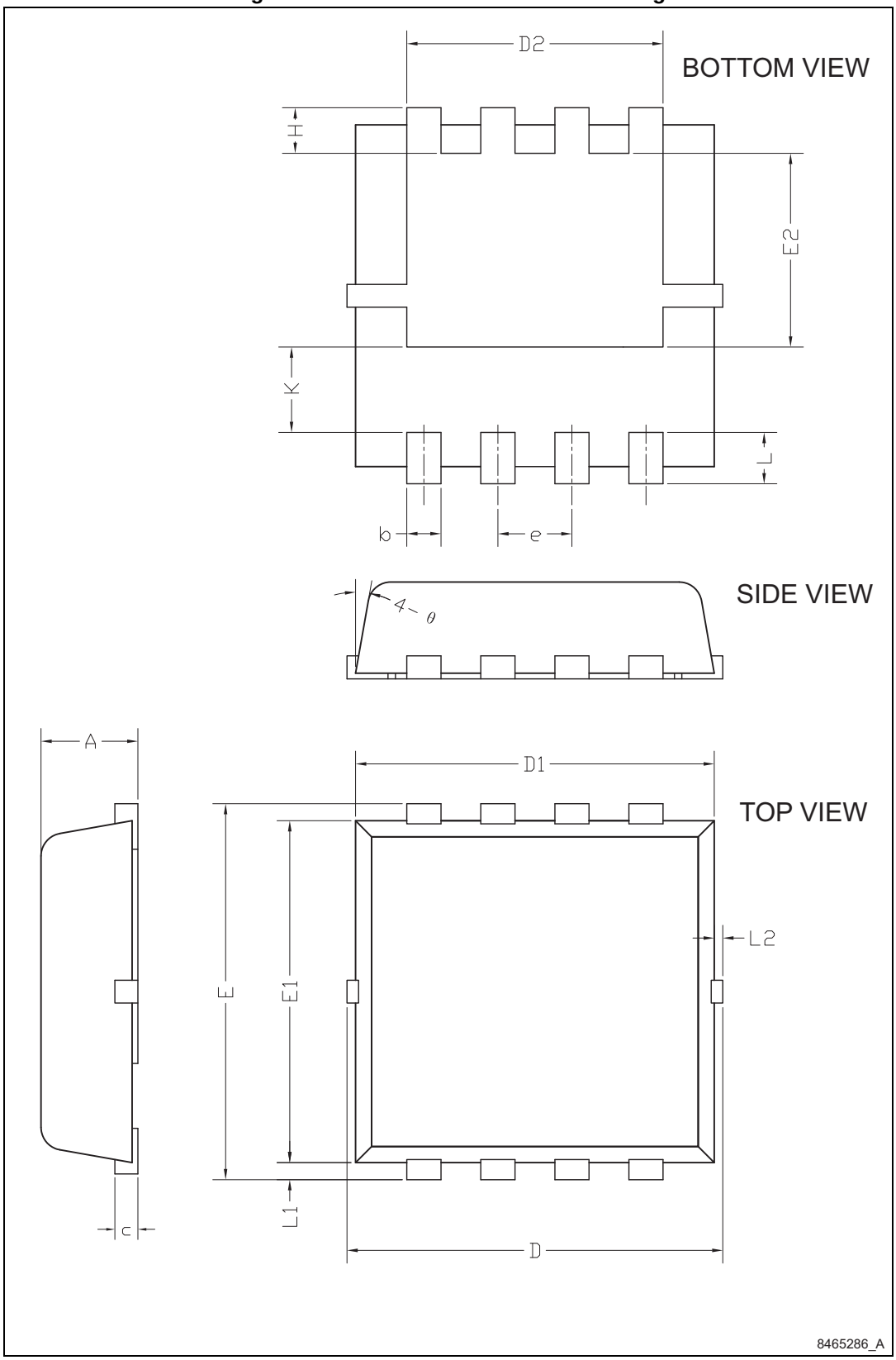
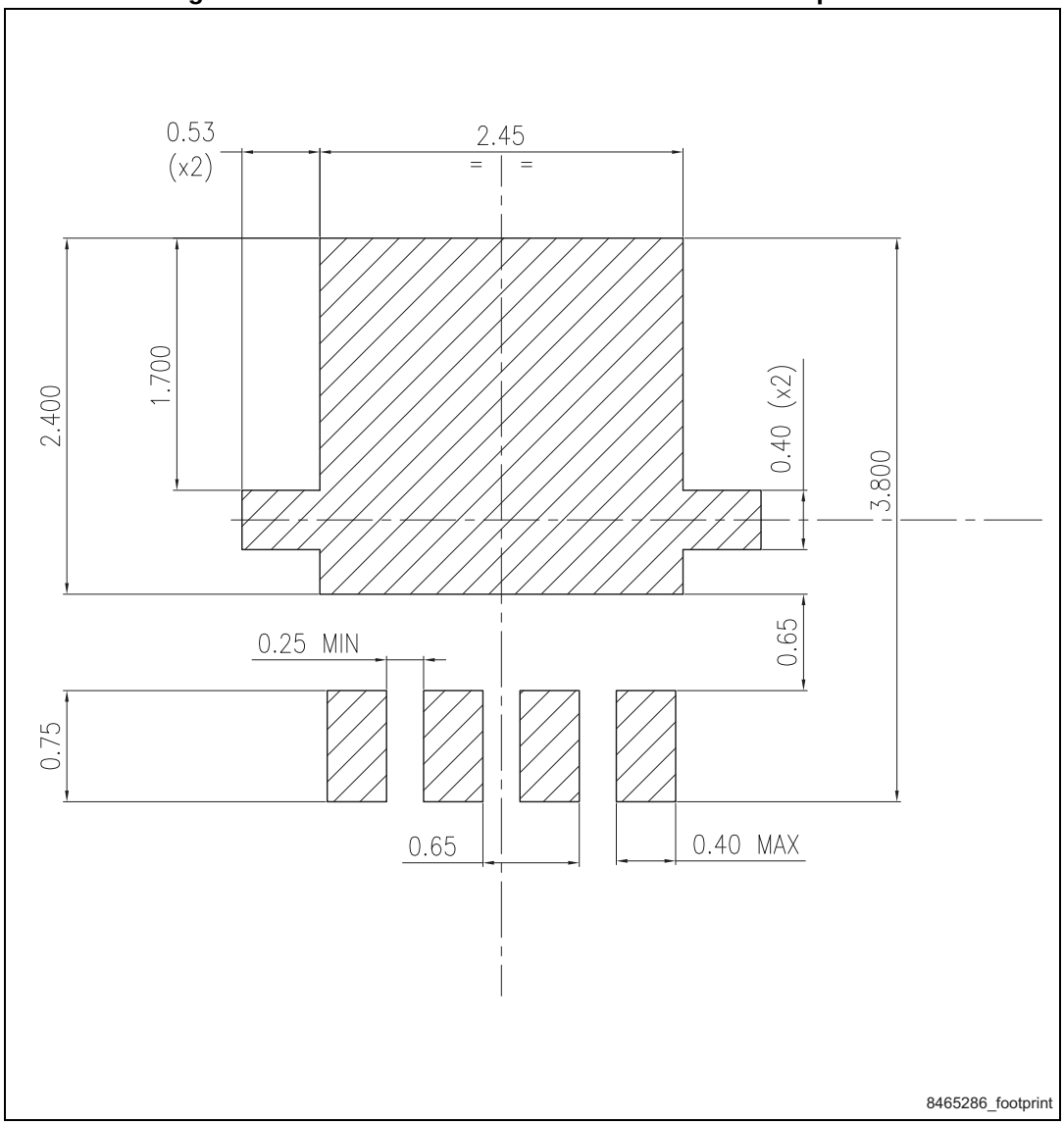


Figure 20. PowerFLAT™ 3.3 x 3.3 recommended footprint(a)



a. All dimensions are in millimeters

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
31-Jul-2013	1	First release.
05-Dec-2014	2	Document status promoted from preliminary to production data. Modified title, features and description in cover page. Modified: $R_{DS(on)}$ typical and max values in first page and in *Table 4: On/off states* Modified: *Section 4: Package mechanical data* Added *Section 2.1: Electrical characteristics (curves)*.