International IOR Rectifier

## StrongIRFET™
IRFR7546PbF
IRFU7546PbF

Application

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters
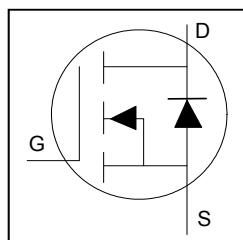
HEXFET® Power MOSFET

|	
V_{DSS}	60V
$R_{DS(on)}$ typ.	6.6mΩ
max	7.9mΩ
I_{D} (Silicon Limited)	71A①
I_{D} (Package Limited)	56A

Benefits

- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche SOA
- Enhanced body diode dV/dt and dI/dt capability
- Lead-free, RoHS compliant

D-Pak
IRFR7546PbF
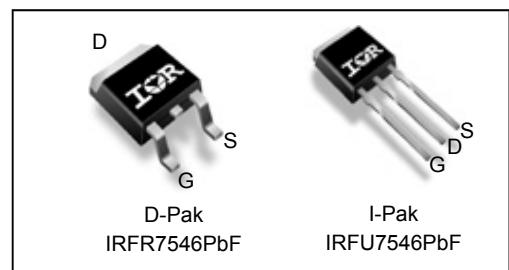
I-Pak
IRFU7546PbF

G	D	S
Gate	Drain	Source

| Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFR7546PbF	D-Pak	Tube	75	IRFR7546PbF
		Tape and Reel	2000	IRFR7546TRPbF
IRFU7546PbF	I-Pak	Tube	75	IRFU7546PbF
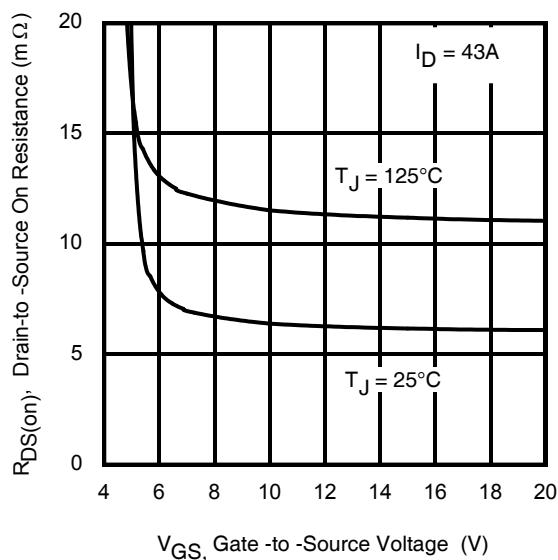
Fig 1. Typical On-Resistance vs. Gate Voltage
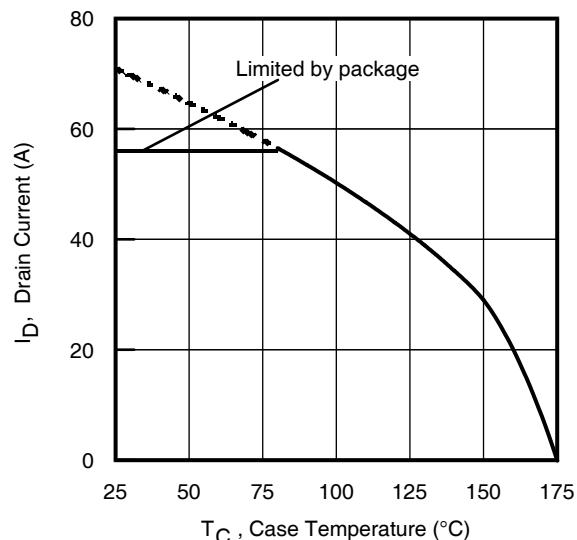
Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	71①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	50	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	56	
I_{DM}	Pulsed Drain Current ②	280	
P_D @T_C = 25°C	Maximum Power Dissipation	99	W
	Linear Derating Factor	0.66	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Max.	Units
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	120	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑩	178	
I_{AR}	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.52	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑨	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Static @ T_J = 25°C (unless otherwise specified)

| Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	47	——	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	6.6	7.9	mΩ	V_{GS} = 10V, I_D = 43A
		——	8.5	——		V_{GS} = 6.0V, I_D = 21A
$V_{GS(th)}$	Gate Threshold Voltage	2.1	——	3.7	V	V_{DS} = V_{GS}, I_D = 100µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	µA	V_{DS} = 60V, V_{GS} = 0V
		——	——	150		V_{DS} = 60V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	1.5	——	Ω	

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 130µH, R_G = 50Ω, I_{AS} = 43A, V_{GS} =10V.

④ $I_{SD} \leq$ 43A, di/dt $\leq$ 1020A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

⑤ Pulse width $\leq$ 400µs; duty cycle $\leq$ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑩ Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 19A, V_{GS} =10V.

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	56	——	——	S	V_{DS} = 25V, I_D = 43A
Q_g	Total Gate Charge	——	58	87		I_D = 43A
Q_{gs}	Gate-to-Source Charge	——	14	——	nC	V_{DS} = 30V
Q_{gd}	Gate-to-Drain Charge	——	18	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg – Qgd)	——	26	——		
$t_{d(on)}$	Turn-On Delay Time	——	8.1	——		V_{DD} = 30V
t_r	Rise Time	——	28	——		I_D = 43A
$t_{d(off)}$	Turn-Off Delay Time	——	36	——	ns	R_G= 2.7Ω
t_f	Fall Time	——	20	——		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	——	3020	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	280	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	180	——	pF	f = 1.0MHz, See Fig.7
$C_{oss eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	290			V_{GS} = 0V, V_{DS} = 0V to 48V⑦
$C_{oss eff.(TR)}$	Output Capacitance (Time Related)	——	370	——		V_{GS} = 0V, V_{DS} = 0V to 48V⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	71①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	280		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J = 25°C,I_S = 43A,V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery dv/dt	——	12	——	V/ns	T_J = 175°C,I_S = 43A,V_{DS} = 60V④
t_{rr}	Reverse Recovery Time	——	26	——	ns	T_J = 25°C V_{DD} = 51V
		——	29	——		T_J = 125°C I_F = 43A,
Q_{rr}	Reverse Recovery Charge	——	22	——	nC	T_J = 25°C di/dt = 100A/μs ⑤
		——	30	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	1.5	——	A	T_J = 25°C
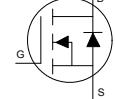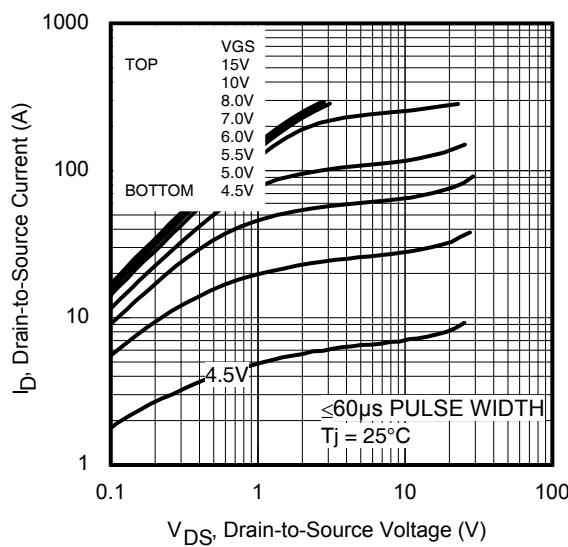
Fig 3. Typical Output Characteristics
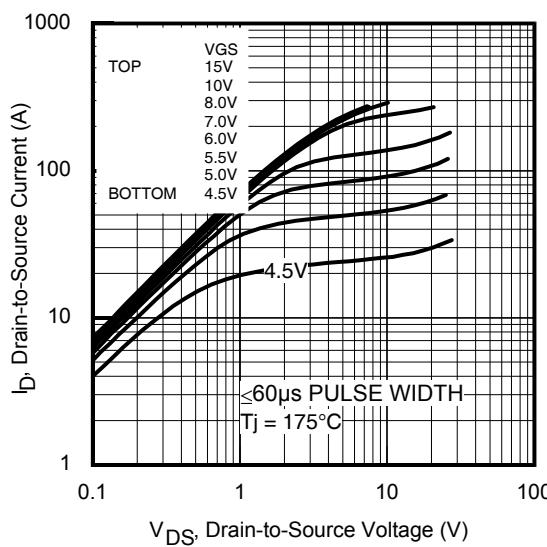
Fig 4. Typical Output Characteristics
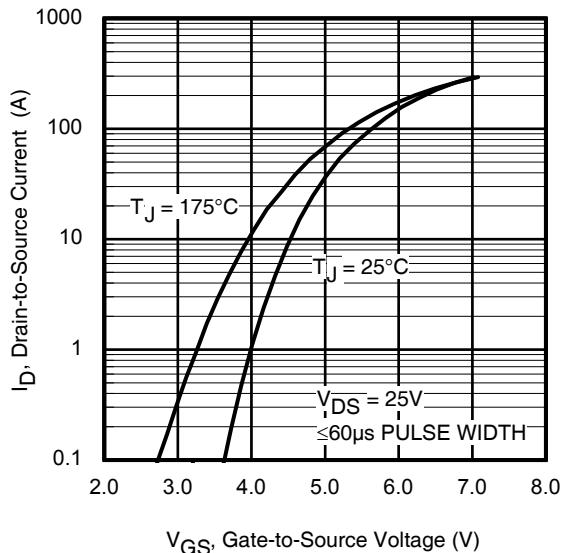
Fig 5. Typical Transfer Characteristics
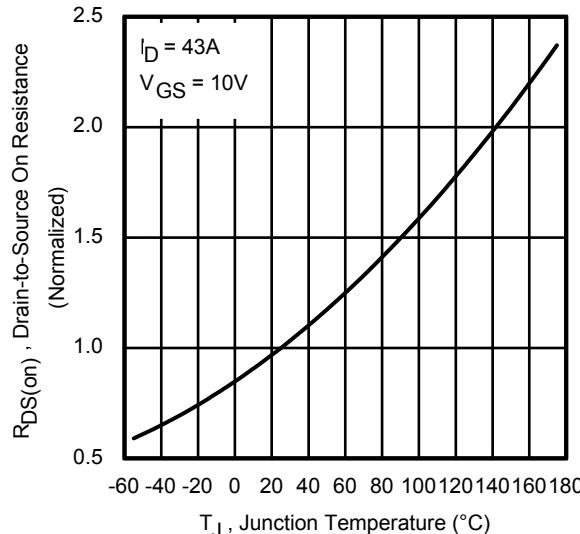
Fig 6. Normalized On-Resistance vs. Temperature
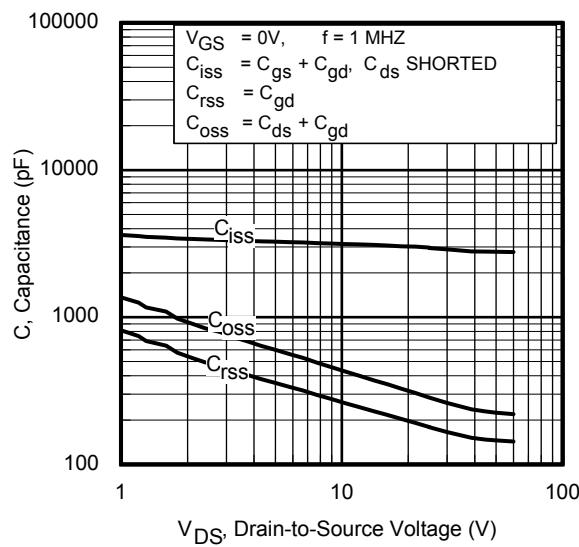
Fig 7. Typical Capacitance vs. Drain-to-Source Voltage
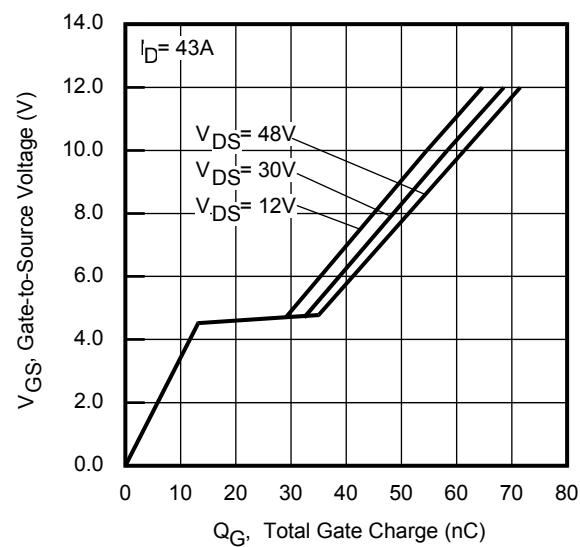
Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage
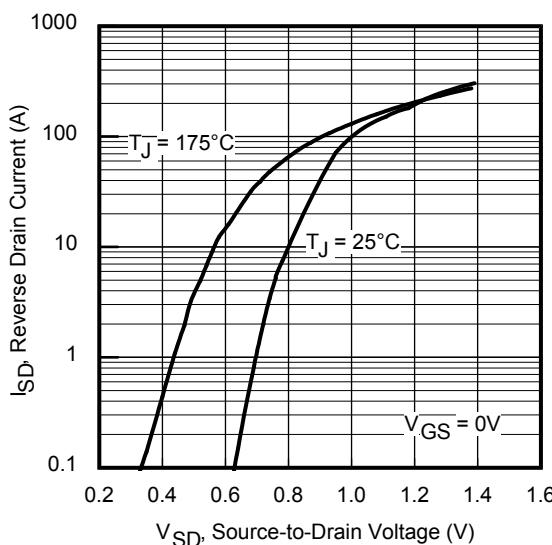
Fig 9. Typical Source-Drain Diode Forward Voltage
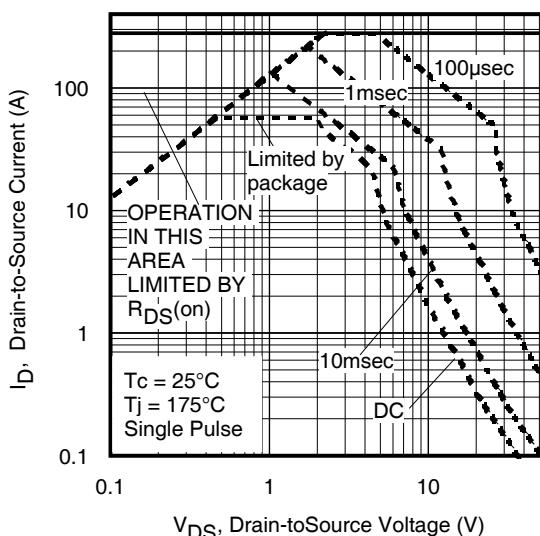
Fig 10. Maximum Safe Operating Area
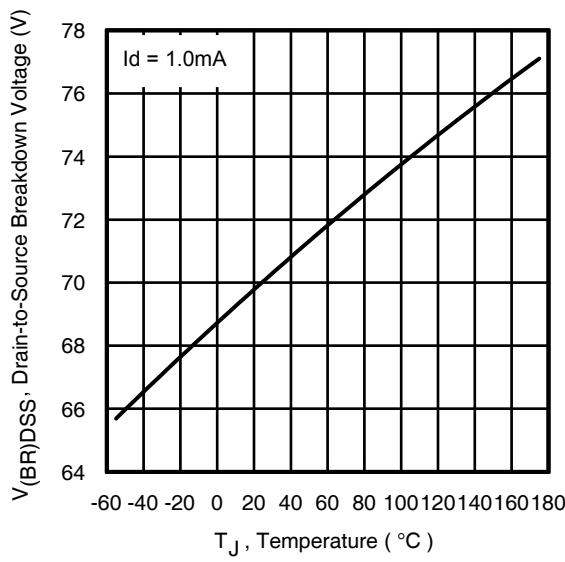
Fig 11. Drain-to-Source Breakdown Voltage
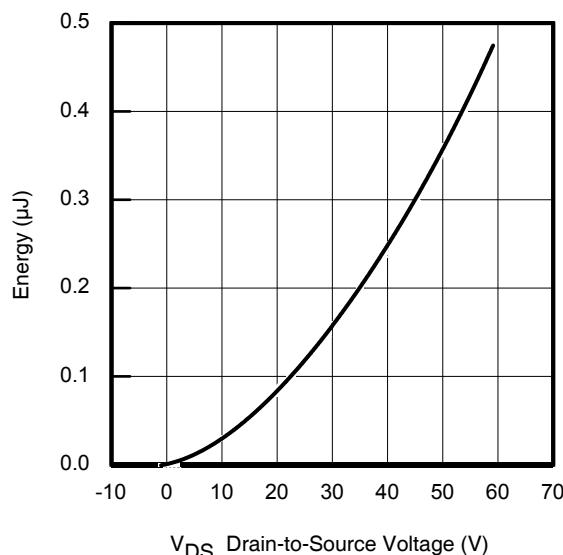
Fig 12. Typical C$_{oss}$ Stored Energy
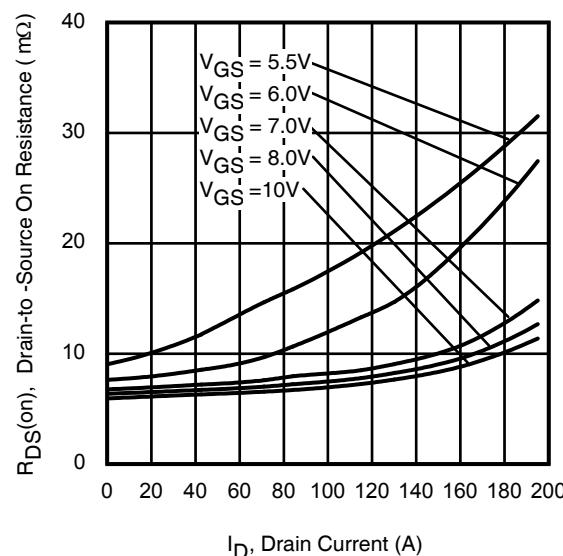
Fig 13. Typical On-Resistance vs. Drain Current
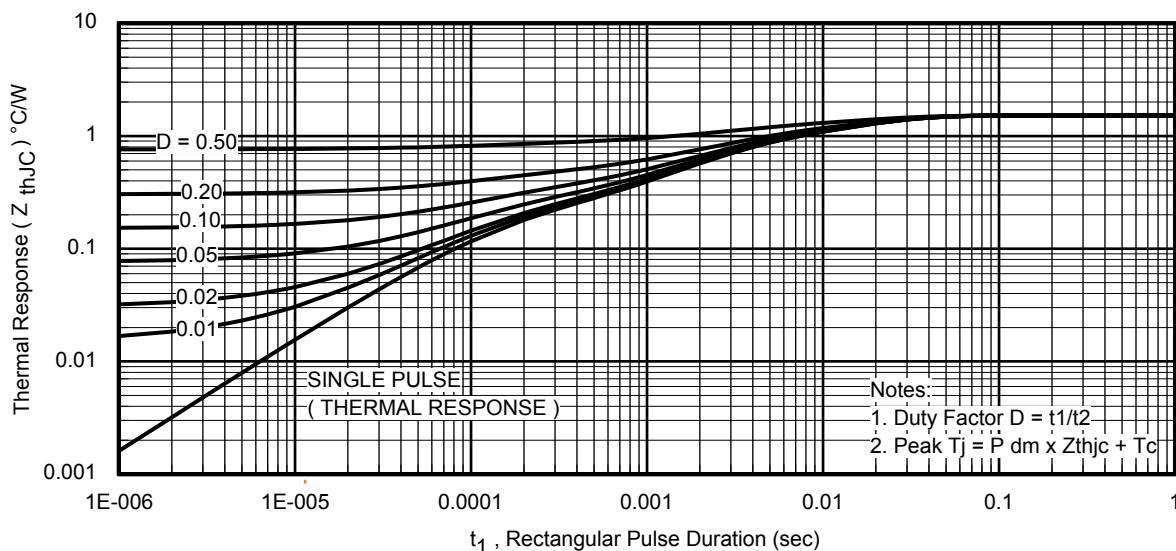
Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

SINGLE PULSE
(THERMAL RESPONSE)

Allowed avalanche Current vs avalanche pulsewidth, tav, assuming $\Delta Tj = 150°C$ and Tstart =25°C (Single Pulse)

Allowed avalanche Current vs avalanche pulsewidth, tav, assuming $\Delta Tj = 25°C$ and Tstart = 150°C.
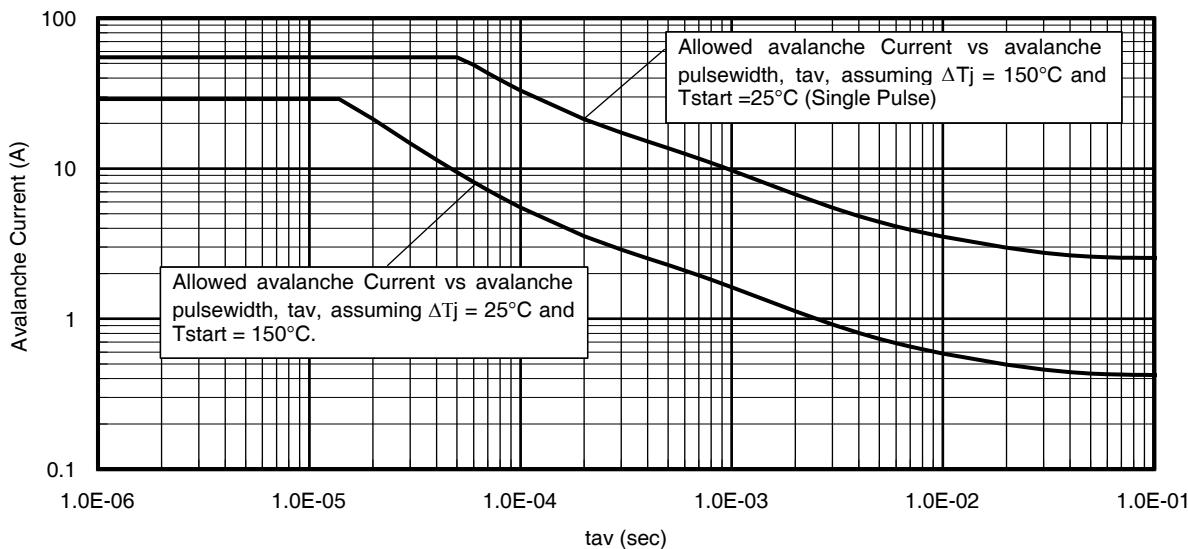
Fig 15. Avalanche Current vs. Pulse Width

TOP   Single Pulse
BOTTOM   1.0% Duty Cycle
$I_D = 43A$
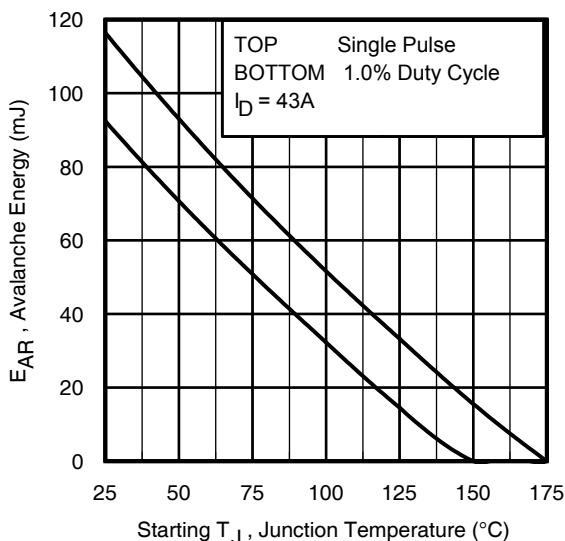
Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 14)
   $PD (ave) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
   $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
   $E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$
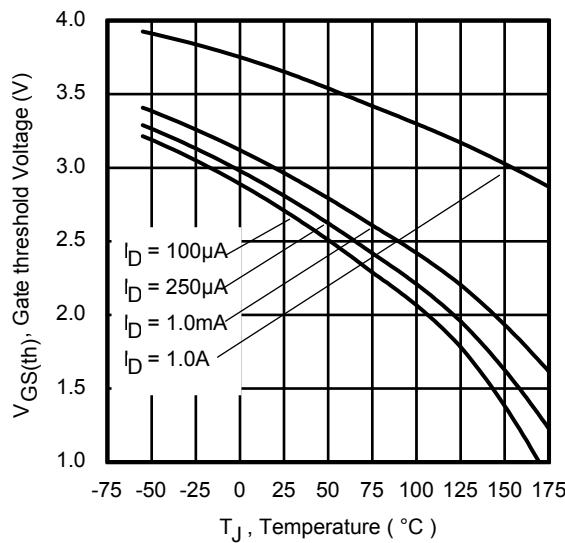
Fig 17. Threshold Voltage vs. Temperature
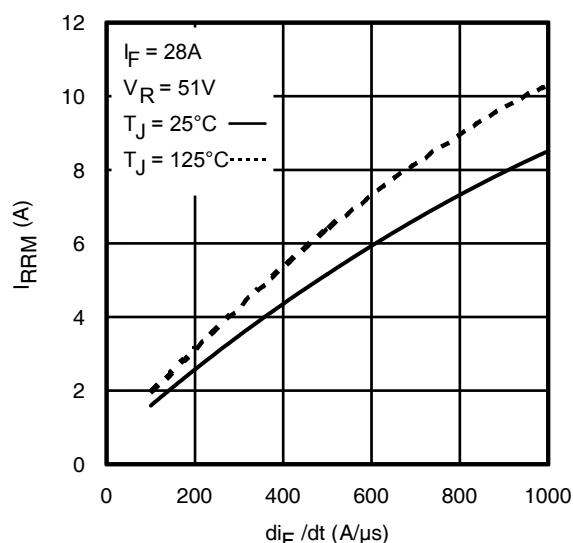
Fig 18. Typical Recovery Current vs. dif/dt
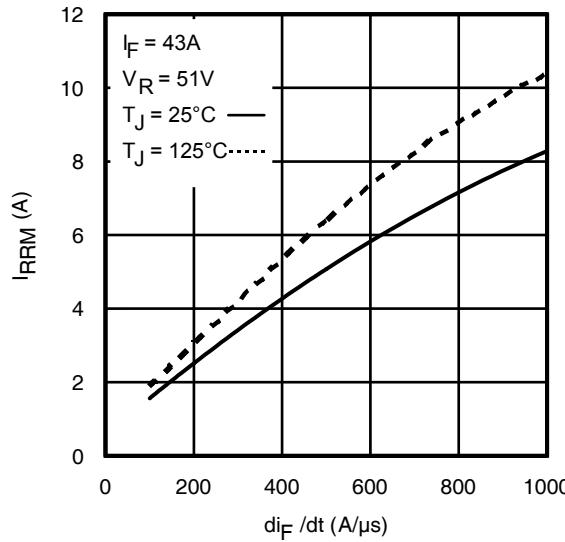
Fig 19. Typical Recovery Current vs. dif/dt
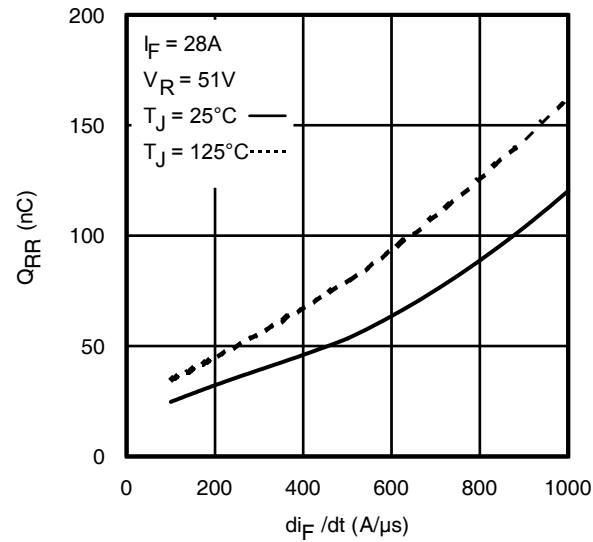
Fig 20. Typical Stored Charge vs. dif/dt
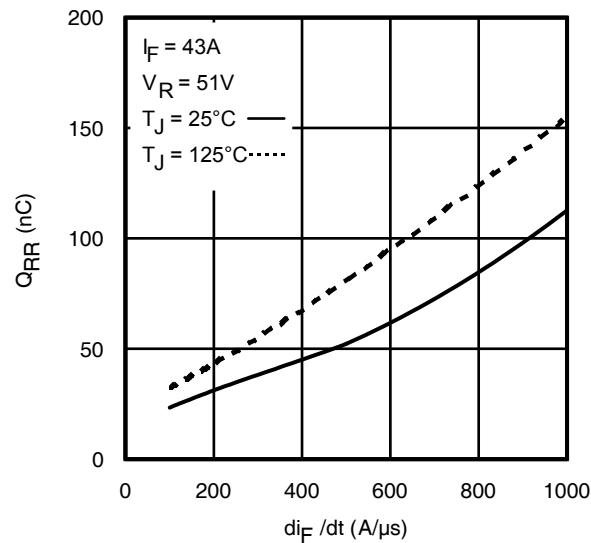
Fig 21. Typical Stored Charge vs. dif/dt
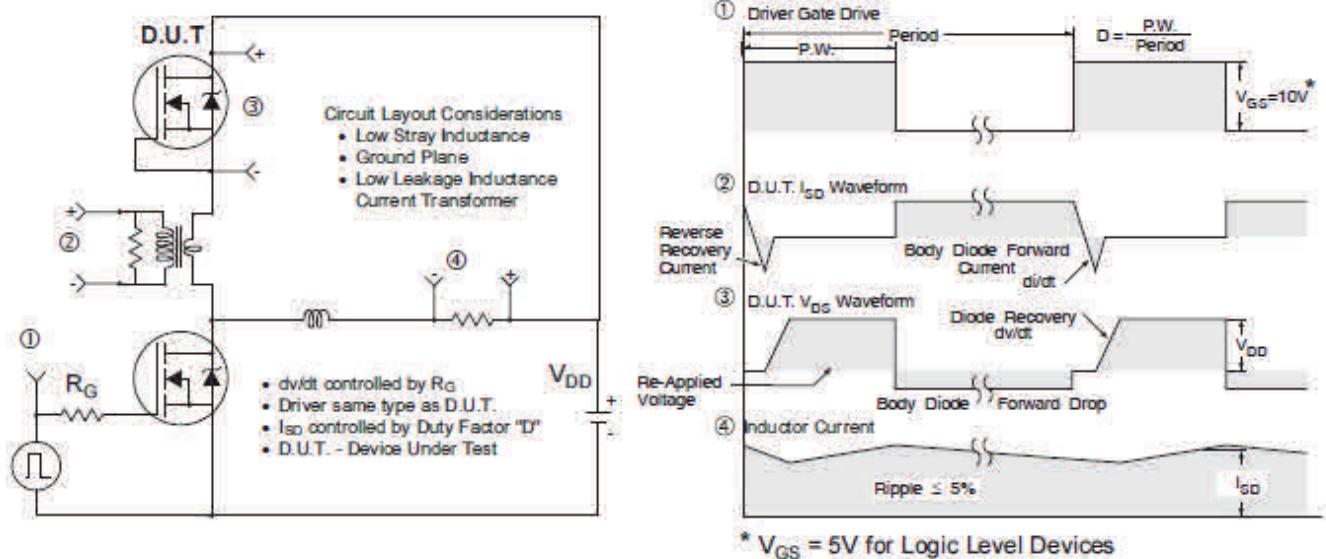
Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
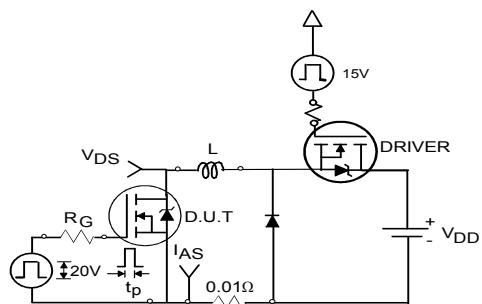
**Fig 23a.** Unclamped Inductive Test Circuit
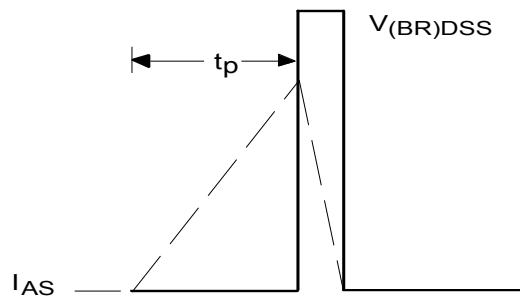
Fig 23b. Unclamped Inductive Waveforms
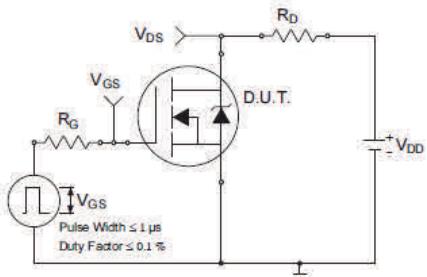
Fig 24a. Switching Time Test Circuit
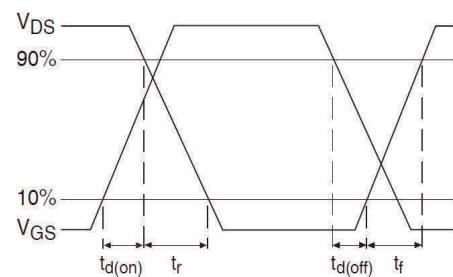

Fig 24b. Switching Time Waveforms
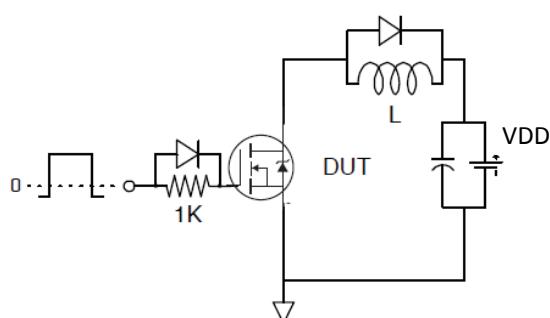
**Fig 25a.** Gate Charge Test Circuit
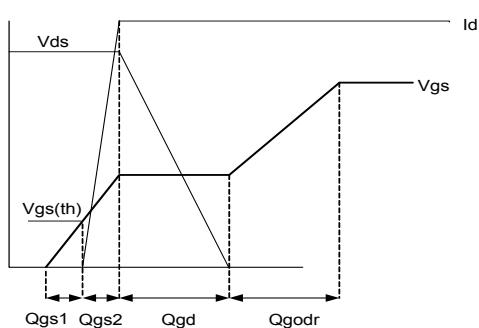
Fig 25b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))
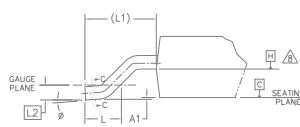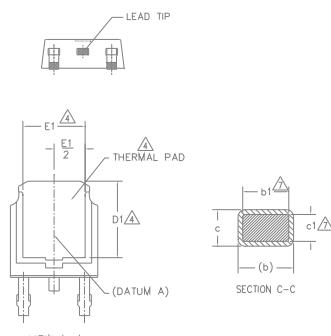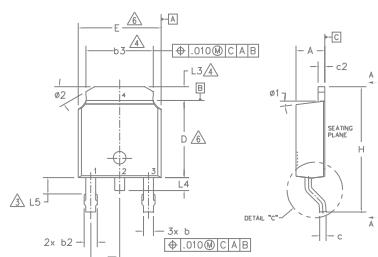
NOTES:
1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994
2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION UNCONTROLLED IN L5.
4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.– SECTION C−C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO−252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT & CoPAK
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P̄" in assembly line position indicates "Lead-Free" qualification to the consumer-level

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 1 = 2001
WEEK 16
LINE A

ASSEMBLY LOT CODE

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)

P̄ = DESIGNATES LEAD-FREE PRODUCT QUALIFIED TO THE CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001
WEEK 16
A = ASSEMBLY SITE CODE

ASSEMBLY LOT CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
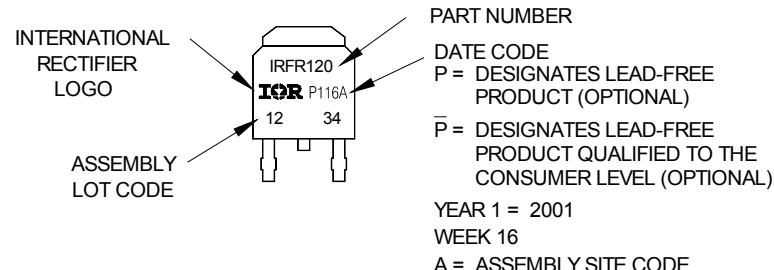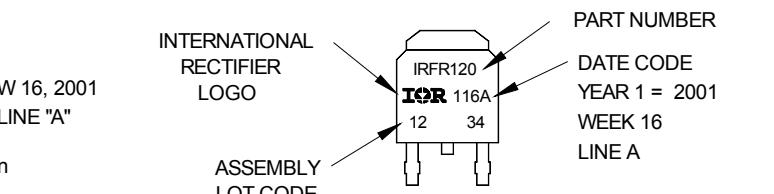
I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))
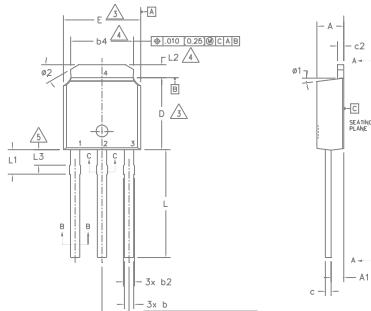
NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4.– THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

5.– LEAD DIMENSION UNCONTROLLED IN L3.

6.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–251AA (Date 06/02).

8.– CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	3
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	0.89	1.52	.035	.060	5
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	
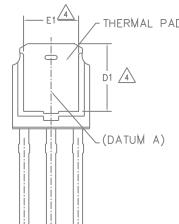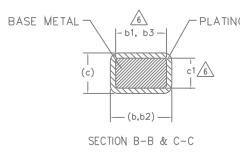
LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates Lead-Free"

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 1 = 2001
WEEK 19
LINE A

ASSEMBLY LOT CODE

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)

YEAR 1 = 2001
WEEK 19
A = ASSEMBLY SITE CODE

ASSEMBLY LOT CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
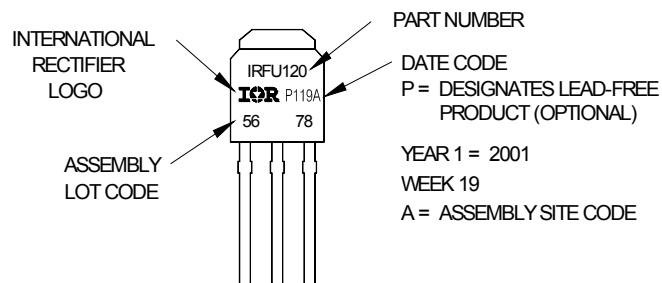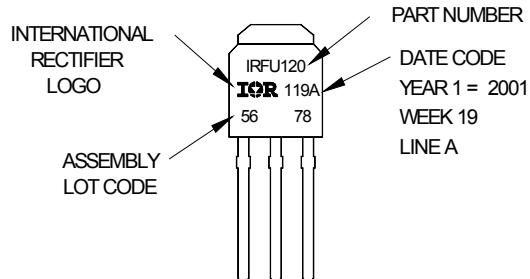
D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))

TR

TRR   TRL

16.3 (.641)
15.7 (.619)

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

8.1 (.318)
7.9 (.312)

FEED DIRECTION
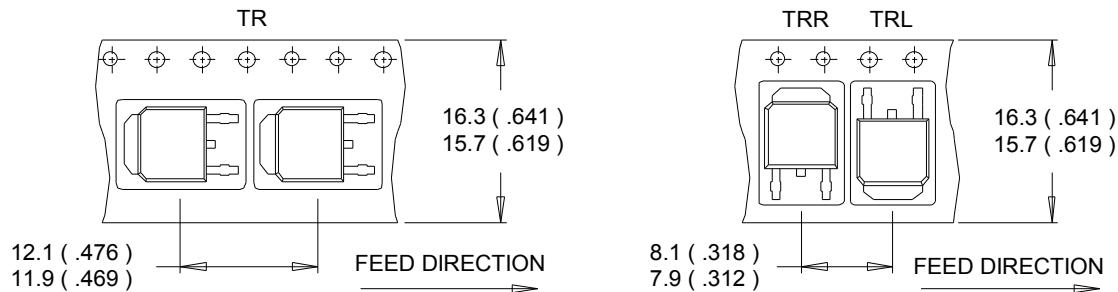
NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

$\varnothing$ 13 INCH

16 mm
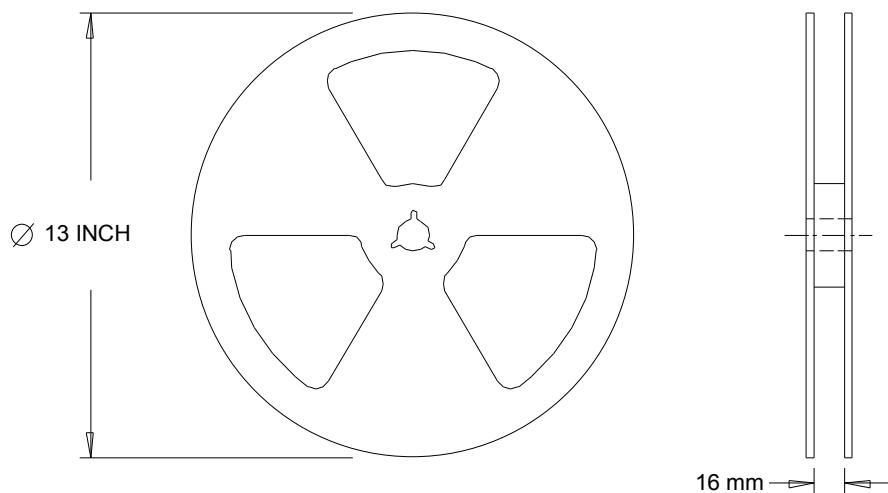
NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D-Pak	MSL1
	I-Pak	N/A
RoHS Compliant	Yes	

†   Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

††   Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
11/7/2014	• Updated $E_{AS\ (L=1mH)}$ = 178mJ on page 2 • Updated note 10 "Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 19A, V_{GS} =10V" on page 2 • Updated package outline on page 9 & 10

International
IƆR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/