![ANALOG DEVICES]

17.0 GHz to 20.0 GHz, GaAs, MMIC, I/Q Upconverter

Data Sheet **HMC7911**

FEATURES

- **Conversion gain: 18 dB typical**
- **Sideband rejection: 30 dBc typical**
- **Input power for 1 dB compression (P1dB): 2 dBm typical**
- **Output third-order intercept (OIP3): 33 dBm typical**
- **2× local oscillator (LO) leakage at RFOUT: 10 dBm typical**
- **2× LO leakage at the IF input: −25 dBm typical**
- **RF return loss: 13 dB typical**
- **LO return loss: 10 dB typical**
- **32-lead, 5 mm × 5 mm LFCSP package**

APPLICATIONS

- **Point to point and point to multipoint radios**
- **Military radars, electronic warfare (EW), and electronic intelligence (ELINT)**
- **Satellite communications**
- **Sensors**

GENERAL DESCRIPTION

The HMC7911 is a compact gallium arsenide (GaAs), pseudomorphic (pHEMT), monolithic microwave integrated circuit (MMIC) upconverter in a RoHS compliant, low stress, injection molded plastic LFCSP package that operates from 17 GHz to 20 GHz. This device provides a small signal conversion gain of 18 dB with 30 dBc of sideband rejection. The HMC7911 uses a variable gain amplifier preceded by an in-phase/quadrature (I/Q) mixer that is driven by an active 2× local oscillator (LO) multiplier. IF1 and IF2 mixer inputs are provided, and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC7911 is a much smaller alternative to hybrid style single sideband (SSB) upconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing techniques.

FUNCTIONAL BLOCK DIAGRAM

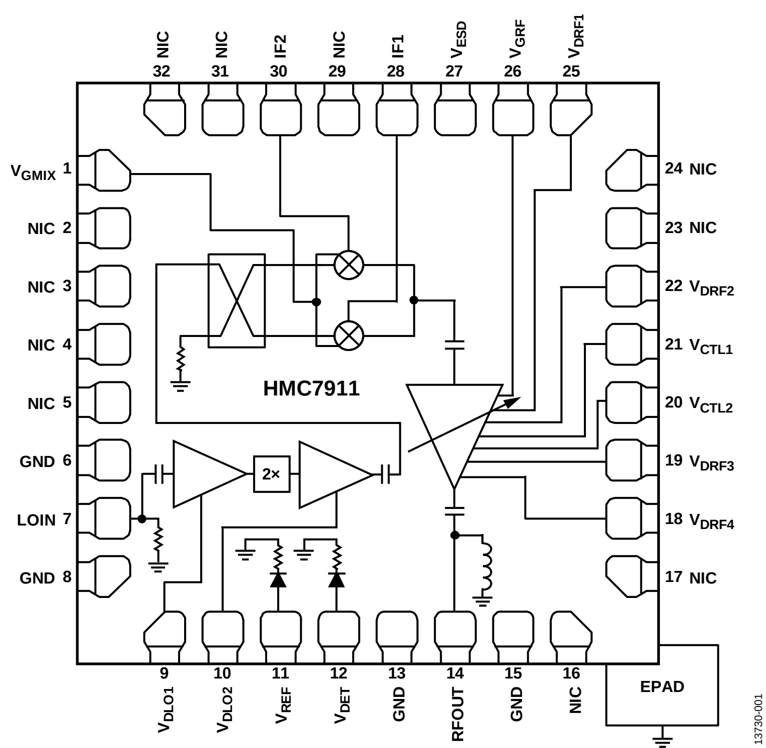

Figure 1.

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HMC7911* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC7911 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC7911: 17.0 GHz to 20.0 GHz, GaAs, MMIC, I/Q Upconverter Data Sheet

REFERENCE MATERIALS

Technical Articles

- The Changing Landscape of Frequency Mixing Components

DESIGN RESOURCES

- HMC7911 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC7911 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

6/2016—Rev. 0 to Rev. A

Change to Local Oscillator (LO) Parameter, Table 1 ... 3
Changes to Figure 76 to Figure 81 ... 18

4/2016—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 5 V, V_{DRFx} = 5 V, V_{CTLx} = −5 V, V_{ESD} = −5 V, V_{GMIX} = −0.5 V, LO = 4 dBm. Measurements performed with lower sideband selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
Radio Frequency (RF)	17		20	GHz
Local Oscillator (LO)	8.5		11.75	GHz
Intermediate Frequency (IF)	DC		3.5	GHz
LO Drive Range	4		8	dBm
PERFORMANCE				
Conversion Gain	13.5	18		dB
Conversion Gain Dynamic Range	30	34		dB
Sideband Rejection	25	30		dBc
Input Power for 1 dB Compression (P1dB)		2		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain	28	33		dBm
2× LO Leakage at RFOUT[1]		10		dBm
2× LO Leakage at IFx[2]		−25		dBm
Noise Figure		14		dB
Return Loss				
RF		13		dB
LO		10		dB
IFx[2]		18		dB
POWER SUPPLY				
Total Supply Current				
LO Amplifier		100		mA
RF Amplifier[3]		220		mA

[1] The LO signal level at the RF output port is not calibrated.
[2] Measurements taken without 90° hybrid at the IF ports.
[3] Adjust V_{GRF} between −2 V and 0 V to achieve a total variable gain amplifier quiescent drain current = 220 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	
V_{DRFx}, V_{DLOx}, V_{REF}, V_{DET}	5.5 V
Gate Bias Voltage	
V_{GRF}	−3 V to 0 V
V_{CTLx}, V_{ESD}	−7 V to 0 V
V_{GMIX}	−2 V to 0 V
LO Input Power	10 dBm
IF Input Power	10 dBm
Maximum Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Reflow Temperature	260°C
ESD Sensitivity (HBM)	250 V (Class 1A)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	31.66	24.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

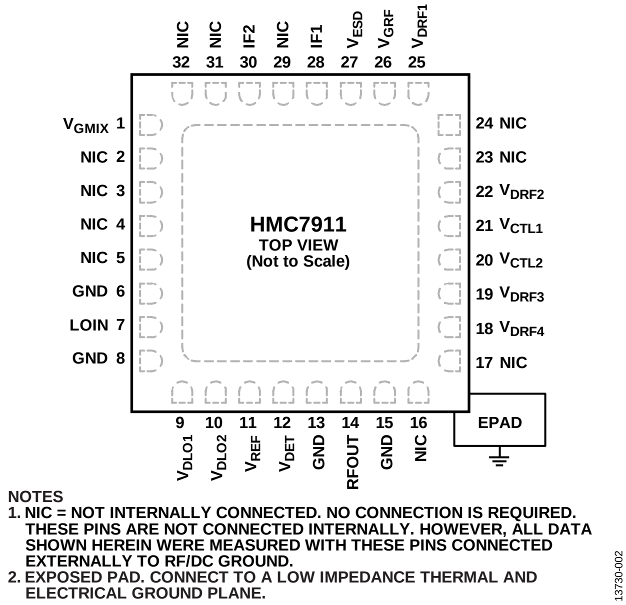

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{GMIX}	Gate Voltage for FET Mixer. See Figure 3. Refer to the typical application circuit for the required external components (see Figure 83).
2, 3, 4, 5, 16, 17, 23, 24, 29, 31, 32	NIC	Not Internally Connected. No connection is required. These pins are not connected internally. However, all data shown herein were measured with these pins connected externally to RF/dc ground.
6, 8, 13, 15	GND	Ground Connect. See Figure 4. These pins and package bottom must be connected to RF/dc ground.
7	LOIN	Local Oscillator Input. See Figure 5. This pin is dc-coupled and matched to 50 Ω.
9, 10	V_{DLO1}, V_{DLO2}	Power Supply Voltage for LO Amplifier. See Figure 6. Refer to the typical application circuit for the required external components (see Figure 83).
11	V_{REF}	Reference Voltage for the Power Detector. See Figure 7. V_{REF} is the dc bias of the diode biased through the external resistor used for temperature compensation of V_{DET}. Refer to the typical application circuit for the required external components (see Figure 83).
12	V_{DET}	Detector Voltage for the Power Detector. See Figure 8. V_{DET} is the dc voltage representing the RF output power rectified by diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 83).
14	RFOUT	Radio Frequency Output. See Figure 9. This pin is dc-coupled and matched to 50 Ω.
18, 19, 22, 25	V_{DRF4}, V_{DRF3}, V_{DRF2}, V_{DRF1}	Power Supply Voltage for the Variable Gain Amplifier. See Figure 10. Refer to the typical application circuit for the required external components (see Figure 83).
20, 21	V_{CTL2}, V_{CTL1}	Gain Control Voltage for the Variable Gain Amplifier. See Figure 11. Refer to the typical application circuit for the required external components (see Figure 83).
26	V_{GRF}	Gate Voltage for the Variable Gain Amplifier. See Figure 12. Refer to the typical application circuit for the required external components (see Figure 83).
27	V_{ESD}	DC Voltage for ESD Protection. See Figure 13. Refer to the typical application circuit for the required external components (see Figure 83).
28, 30	IF1, IF2	Quadrature IF Inputs. See Figure 14. For applications not requiring operation to dc, use an off chip dc blocking capacitor. For operation to dc, these pins must not source/sink more than ±3 mA of current or device malfunction and failure may result.
	EPAD	Exposed Pad. Connect to a low impedance thermal and electrical ground plane.

INTERFACE SCHEMATICS

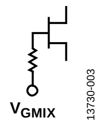

Figure 3. V_{GMIX} Interface

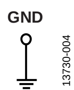

Figure 4. GND Interface

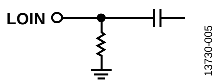

Figure 5. LOIN Interface

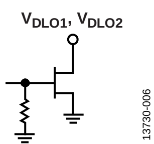

Figure 6. V_{DLO1}, V_{DLO2} Interface

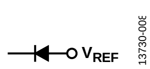

Figure 7. V_{REF} Interface

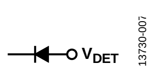

Figure 8. V_{DET} Interface

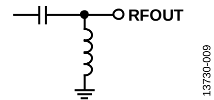

Figure 9. RFOUT Interface

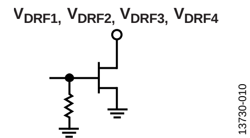

Figure 10. V_{DRF1}, V_{DRF2}, V_{DRF3}, V_{DRF4} Interface

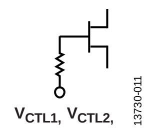

Figure 11. V_{CTL1}, V_{CTL2} Interface

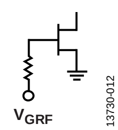

Figure 12. V_{GRF} Interface

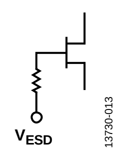

Figure 13. V_{ESD} Interface

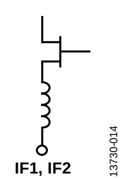

Figure 14. IF1, IF2 Interface

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

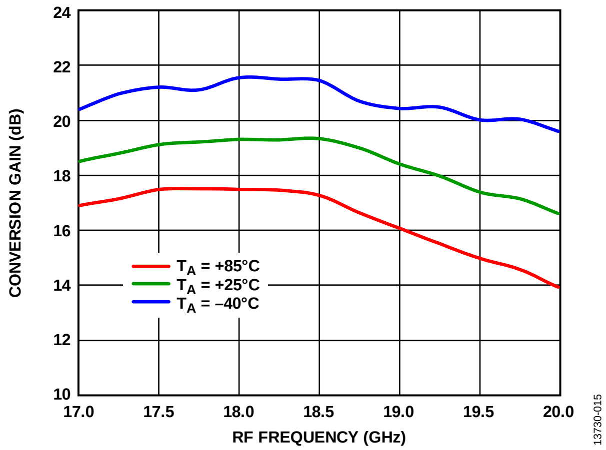

Figure 15. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 4 dBm

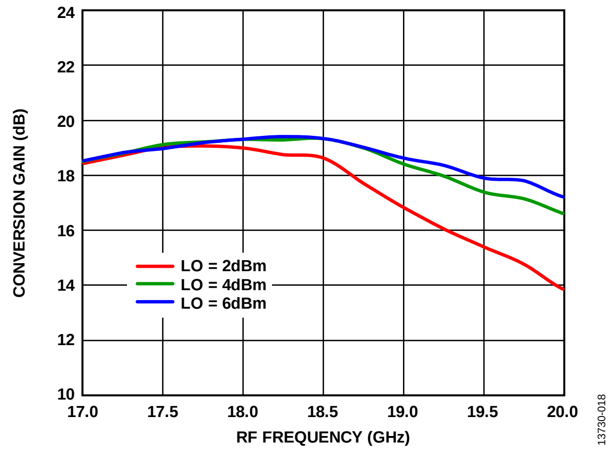

Figure 18. Conversion Gain vs. RF Frequency at Various LO Powers

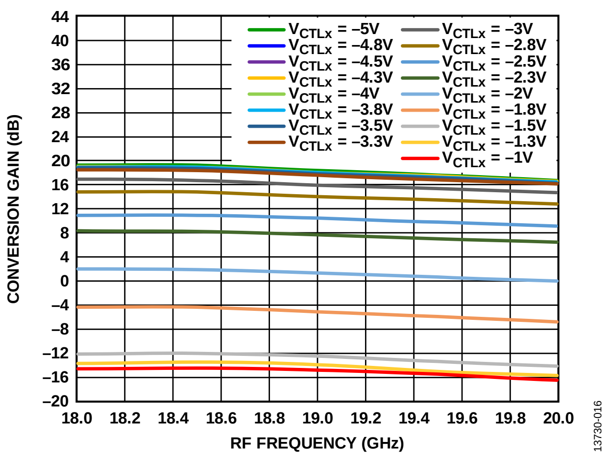

Figure 16. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 4 dBm

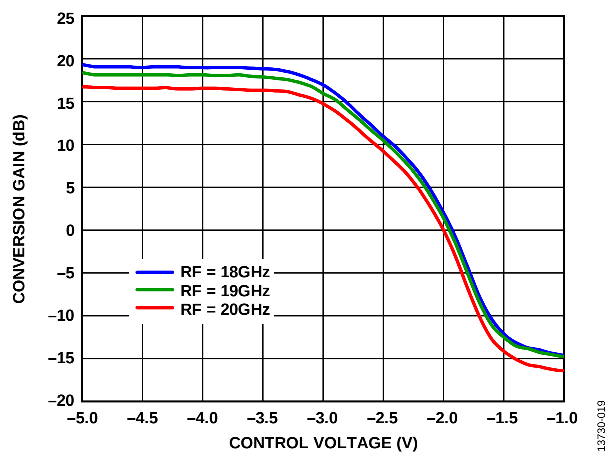

Figure 19. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

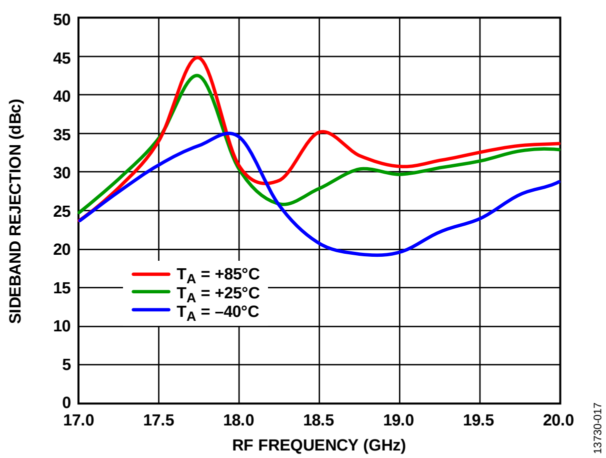

Figure 17. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 4 dBm

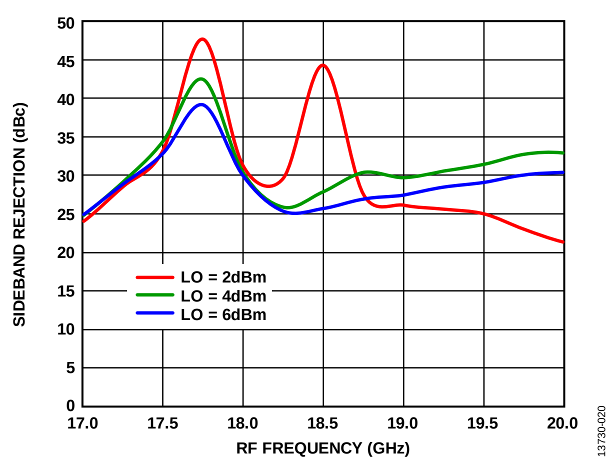

Figure 20. Sideband Rejection vs. RF Frequency at Various LO Powers

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

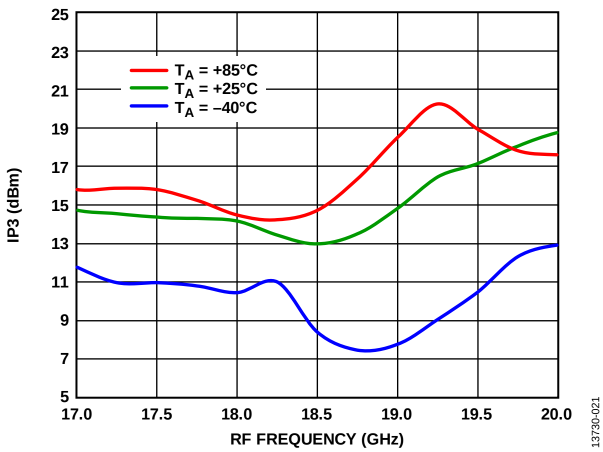

Figure 21. Input IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

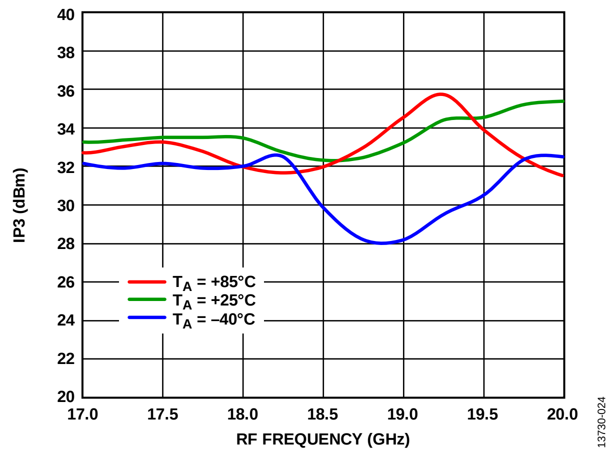

Figure 24. Output IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

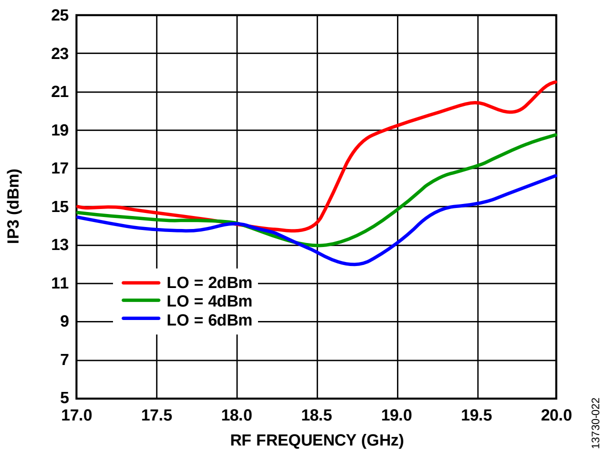

Figure 22. Input IP3 vs. RF Frequency at Various LO Powers

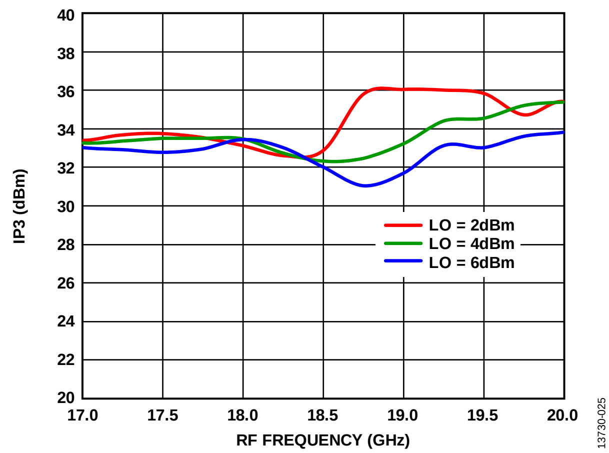

Figure 25. Output IP3 vs. RF Frequency at Various LO Powers

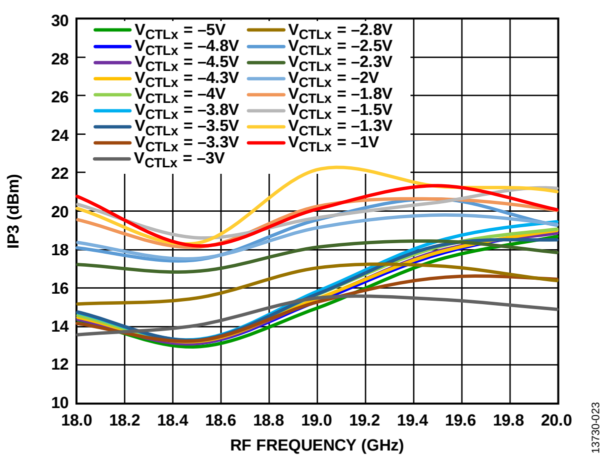

Figure 23. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

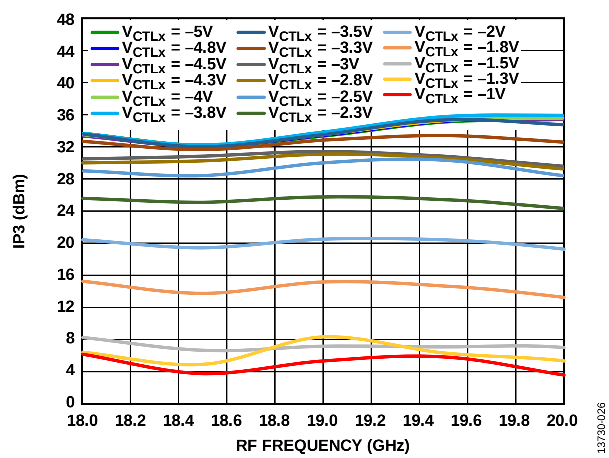

Figure 26. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

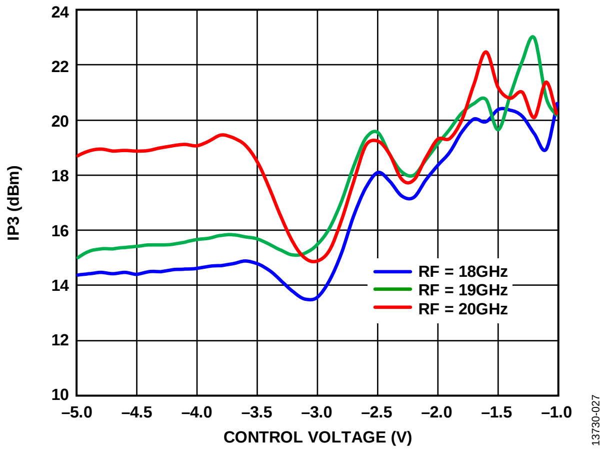

Figure 27. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

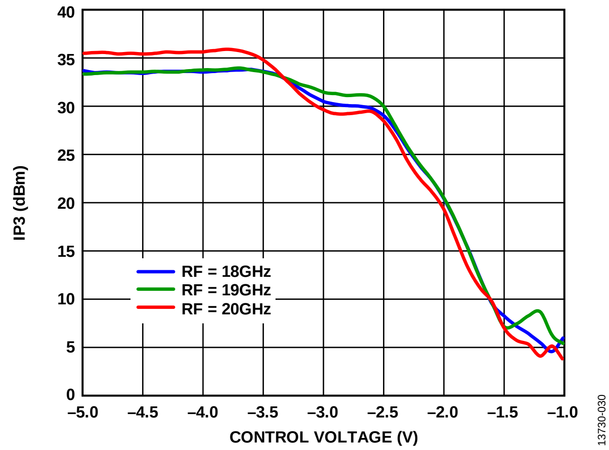

Figure 30. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

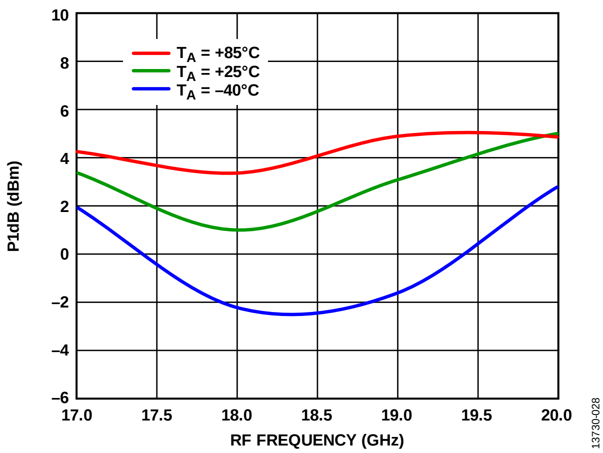

Figure 28. Input P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

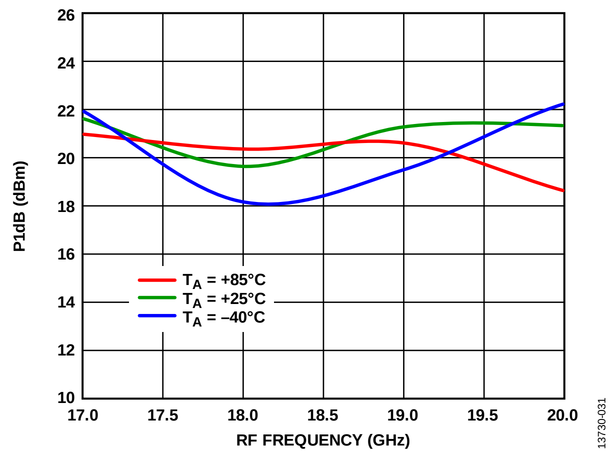

Figure 31. Output P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

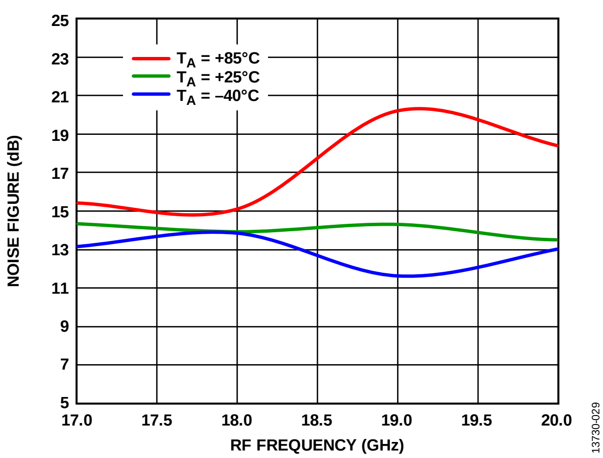

Figure 29. Noise Figure vs. RF Frequency at Various Temperatures, LO = 6 dBm

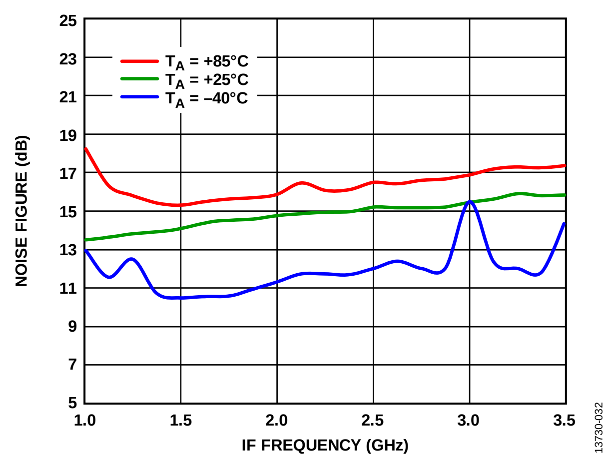

Figure 32. Noise Figure vs. IF Frequency at Various Temperatures, LO = 6 dBm, LO Frequency = 21 GHz

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

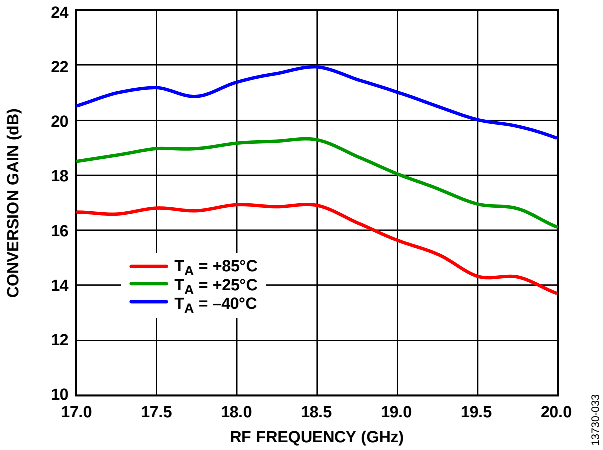

Figure 33. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 4 dBm

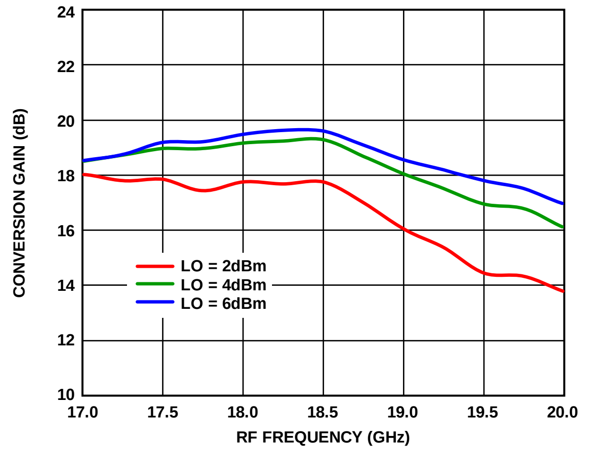

Figure 36. Conversion Gain vs. RF Frequency at Various LO Powers

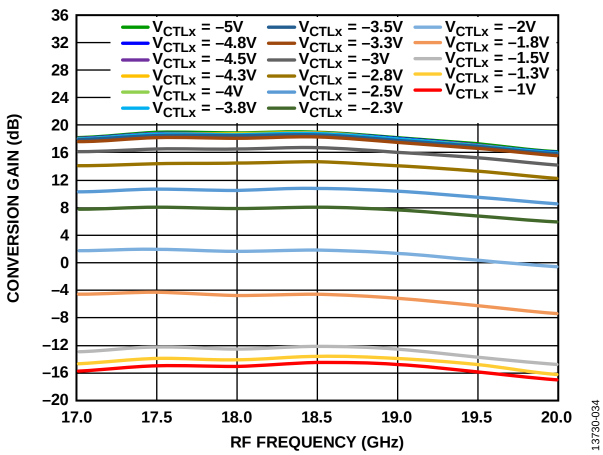

Figure 34. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 4 dBm

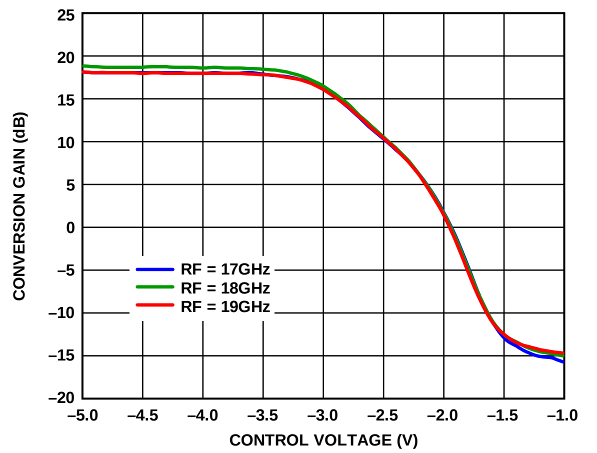

Figure 37. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 4 dBm,

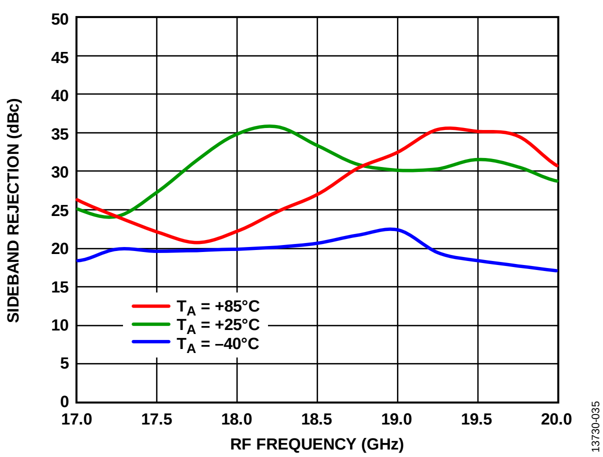

Figure 35. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 4 dBm

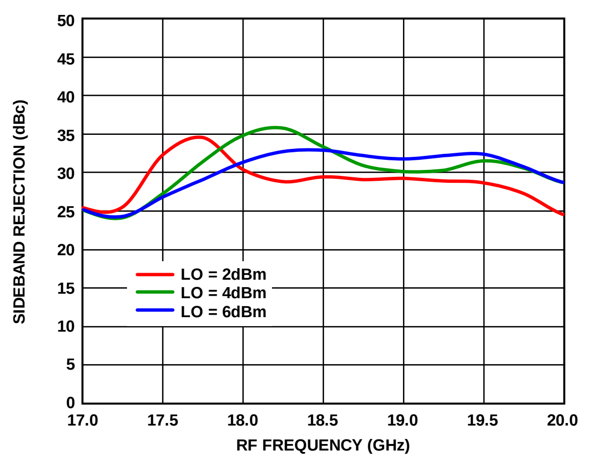

Figure 38. Sideband Rejection vs. RF Frequency at Various LO Powers

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

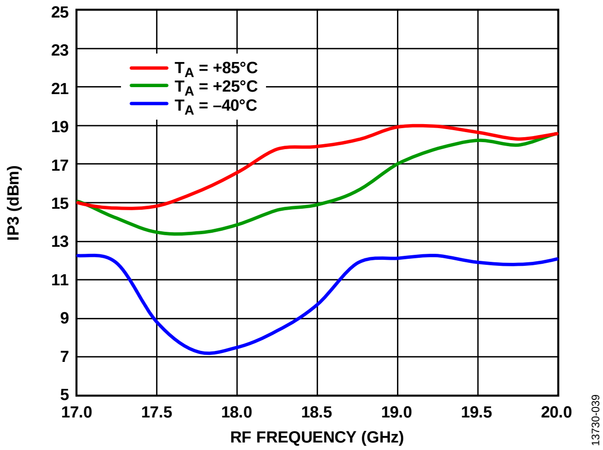

Figure 39. Input IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

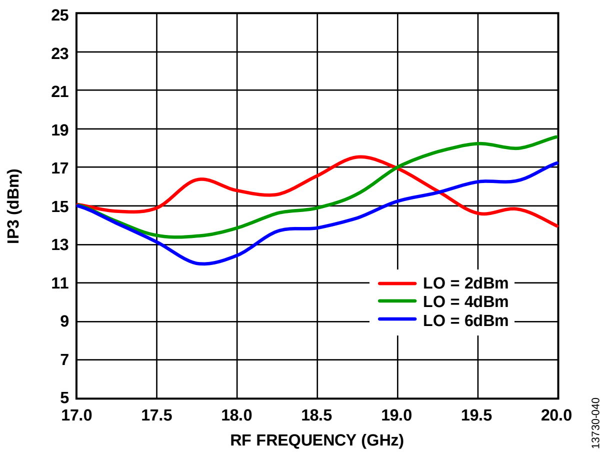

Figure 40. Input IP3 vs. RF Frequency at Various LO Powers

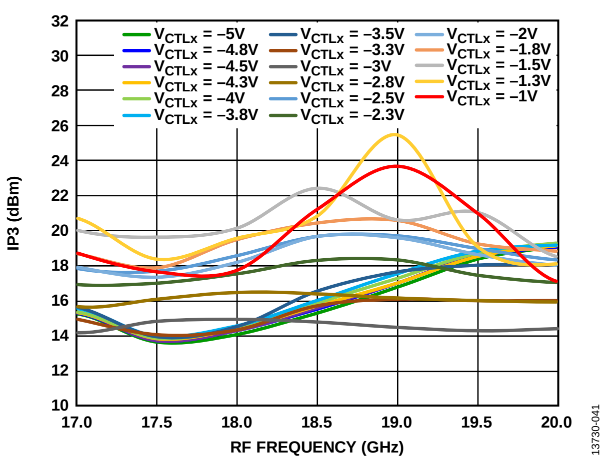

Figure 41. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

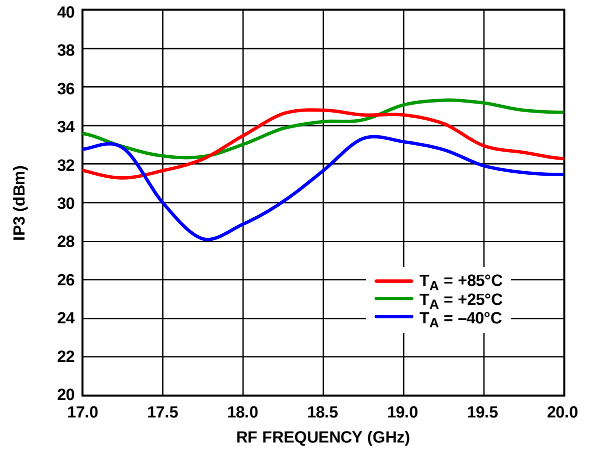

Figure 42. Output IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

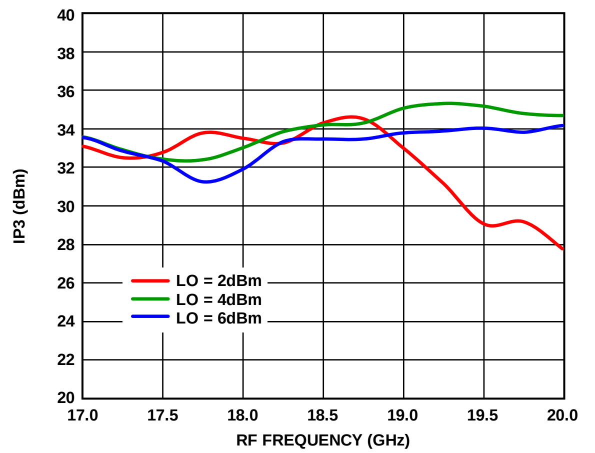

Figure 43. Output IP3 vs. RF Frequency at Various LO Powers

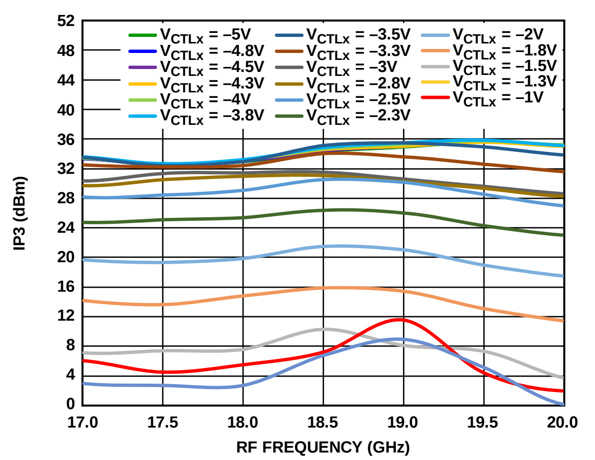

Figure 44. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

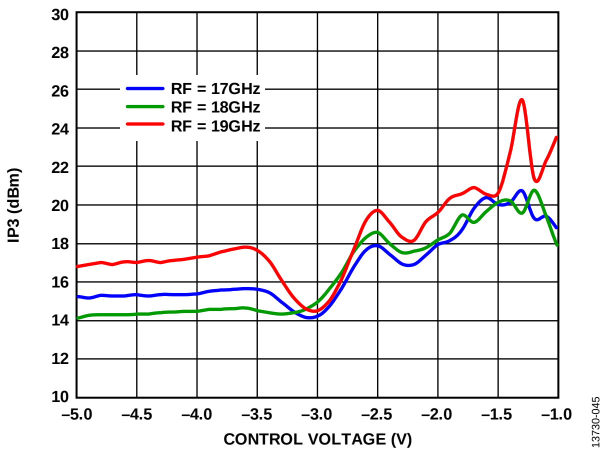

Figure 45. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

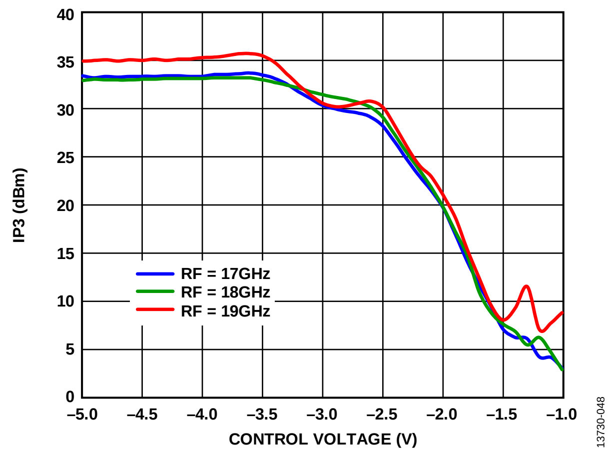

Figure 48. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

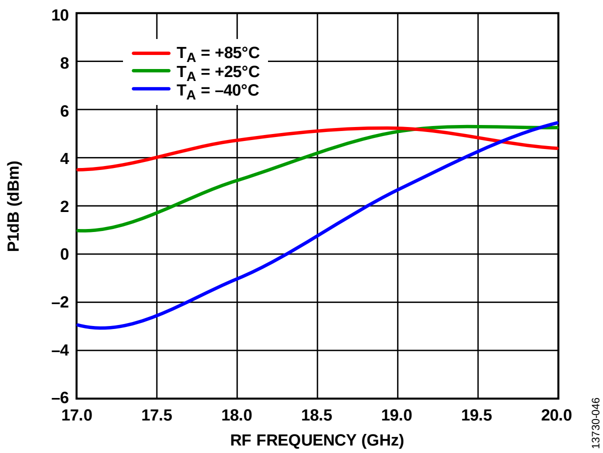

Figure 46. Input P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

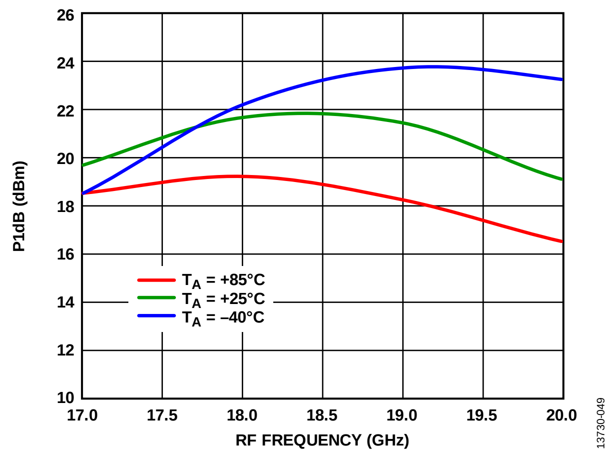

Figure 49. Output P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

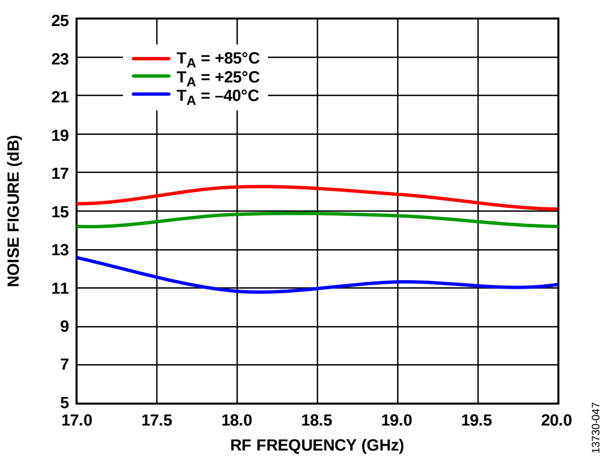

Figure 47. Noise Figure vs. RF Frequency at Various Temperatures, LO = 6 dBm

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

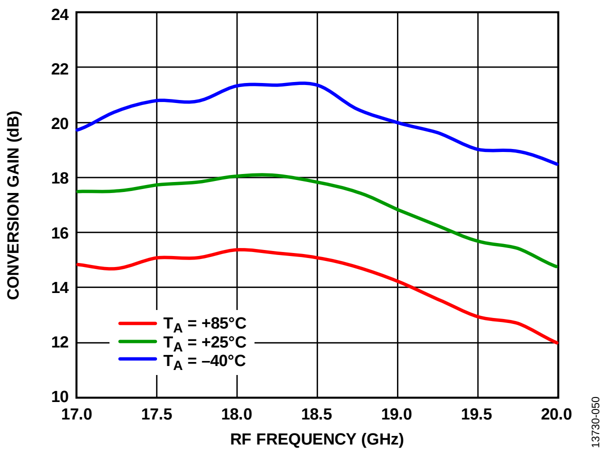

Figure 50. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 4 dBm

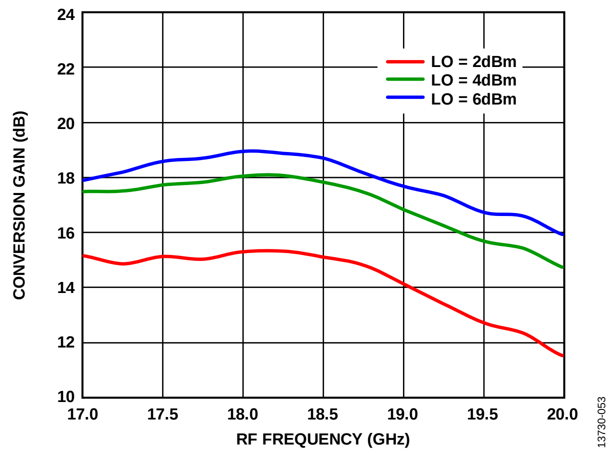

Figure 53. Conversion Gain vs. RF Frequency at Various LO Powers

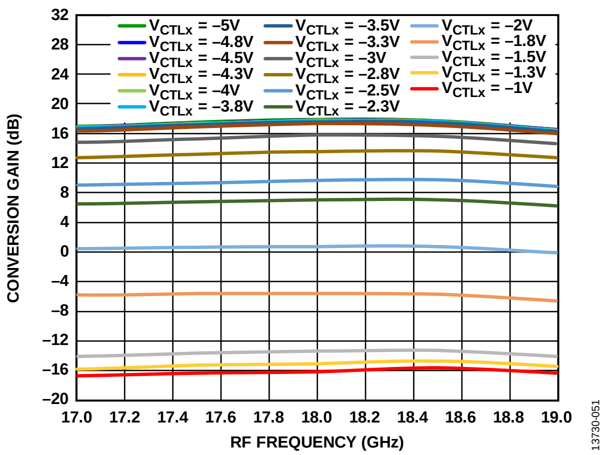

Figure 51. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 4 dBm

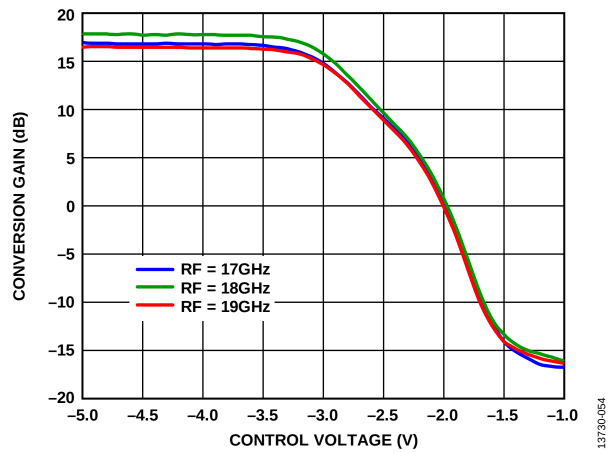

Figure 54. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

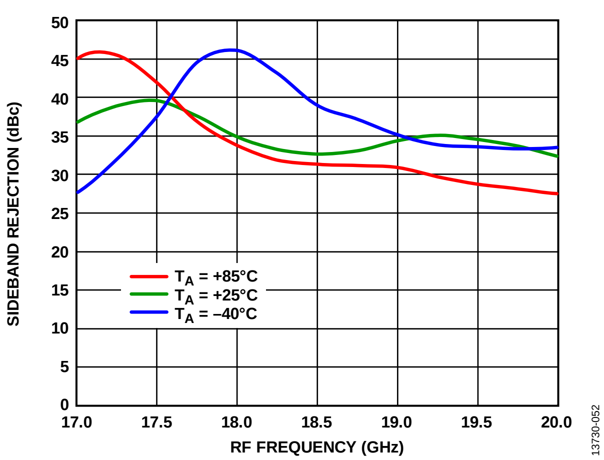

Figure 52. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 4 dBm

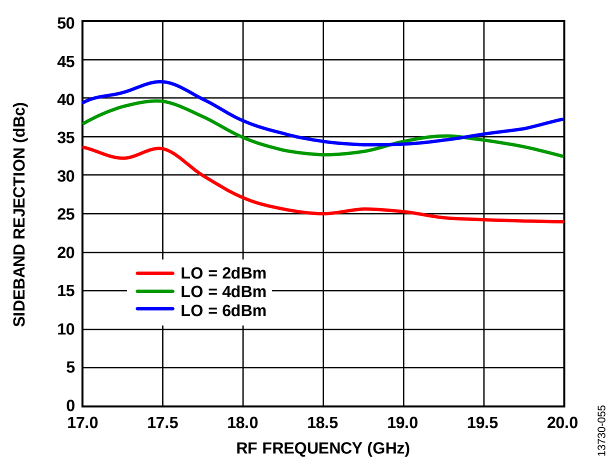

Figure 55. Sideband Rejection vs. RF Frequency at Various LO Powers

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

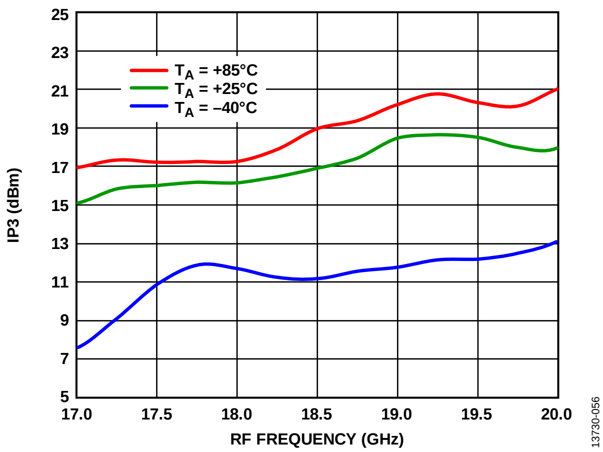

Figure 56. Input IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

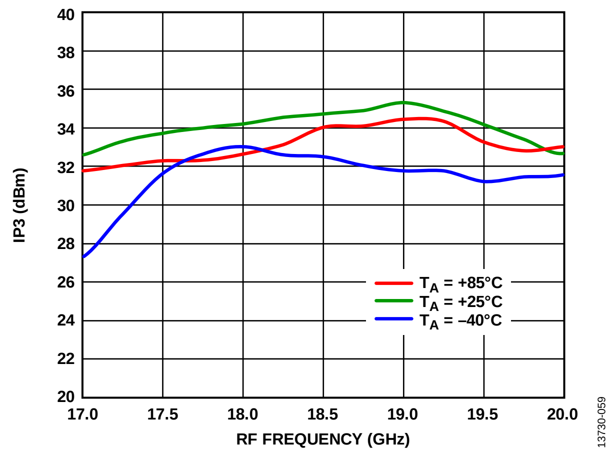

Figure 59. Output IP3 vs. RF Frequency at Various Temperatures, LO = 4 dBm

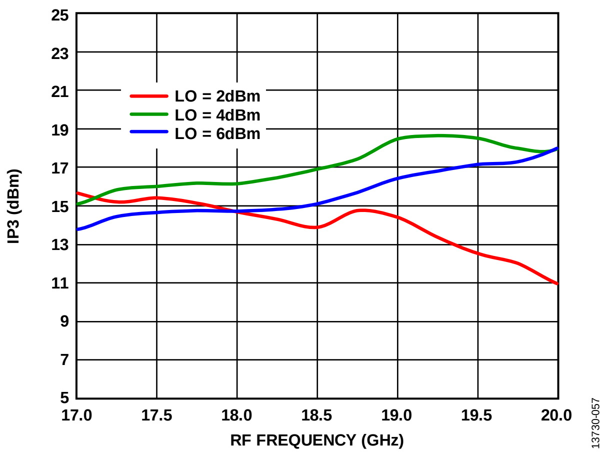

Figure 57. Input IP3 vs. RF Frequency at Various LO Powers

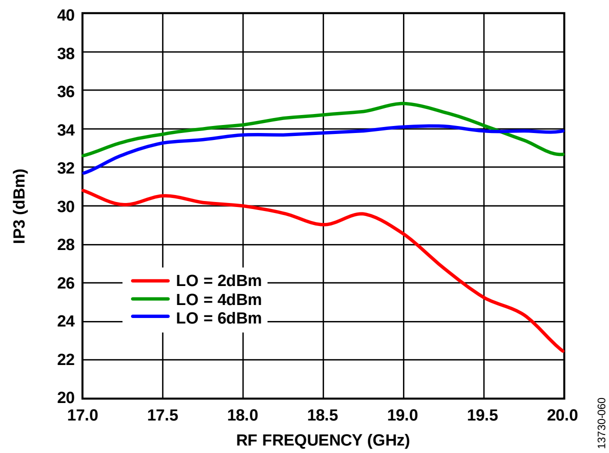

Figure 60. Output IP3 vs. RF Frequency at Various LO Powers

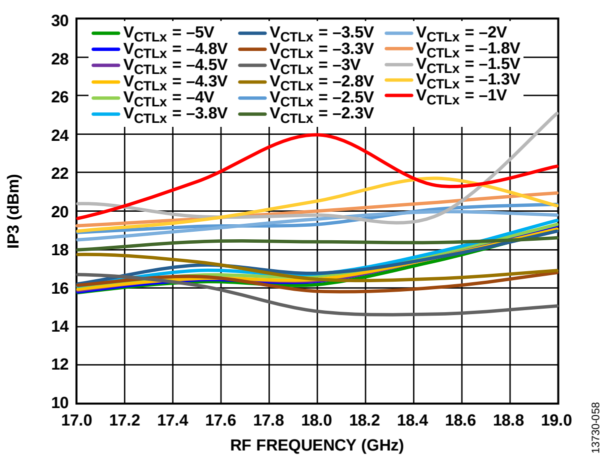

Figure 58. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

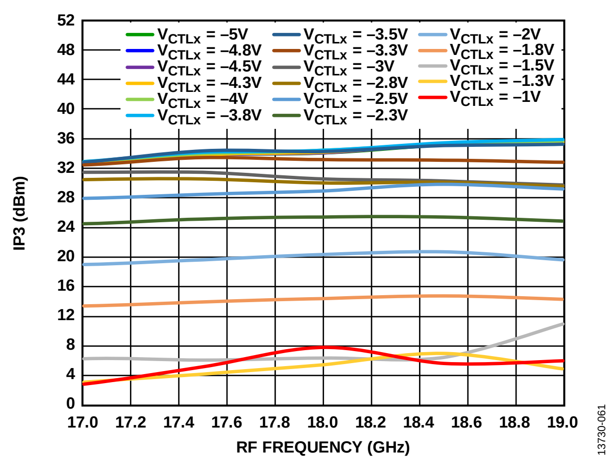

Figure 61. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 4 dBm

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

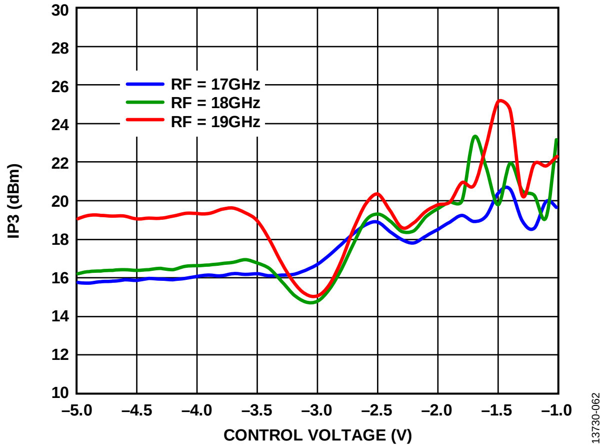

Figure 62. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

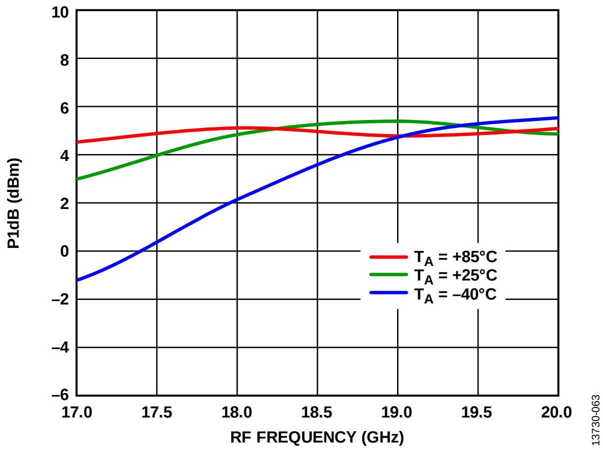

Figure 63. Input P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

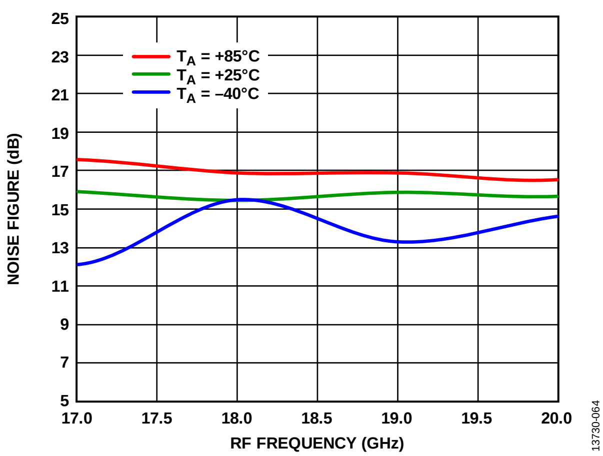

Figure 64. Noise Figure vs. RF Frequency at Various Temperatures, LO = 6 dBm

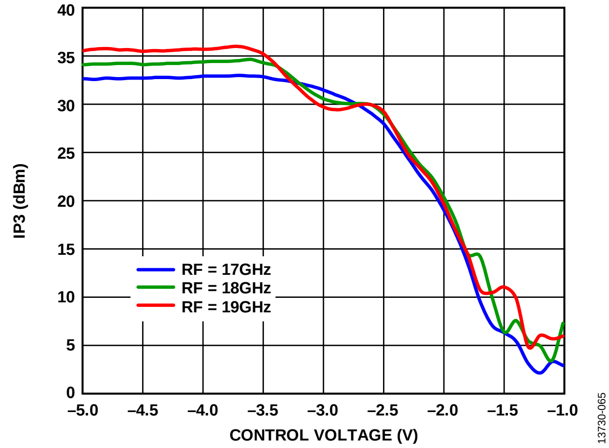

Figure 65. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 4 dBm

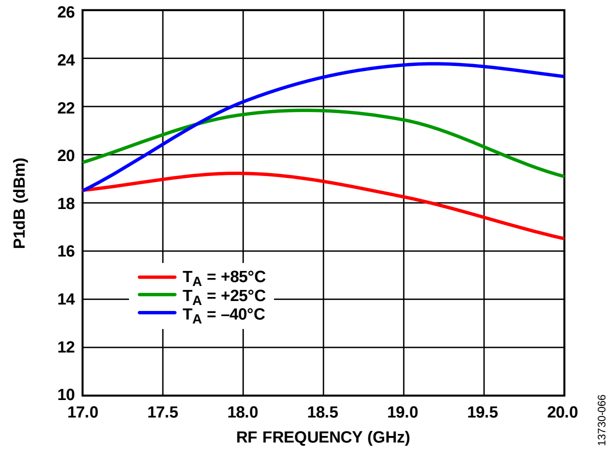

Figure 66. Output P1dB vs. RF Frequency at Various Temperatures, LO = 4 dBm

LEAKAGE PERFORMANCE

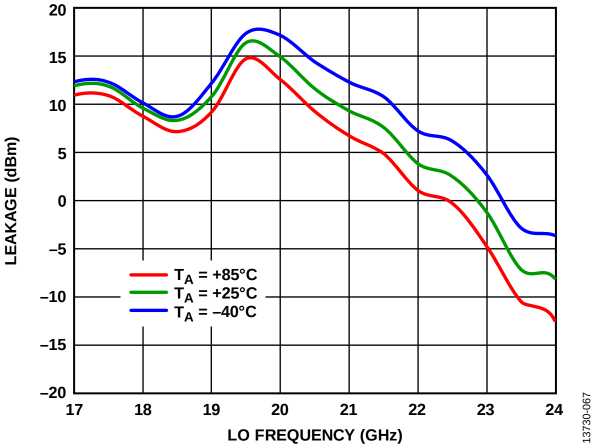

Figure 67. 2× LO Leakage at RFOUT vs. LO Frequency at Various Temperatures, LO = 4 dBm

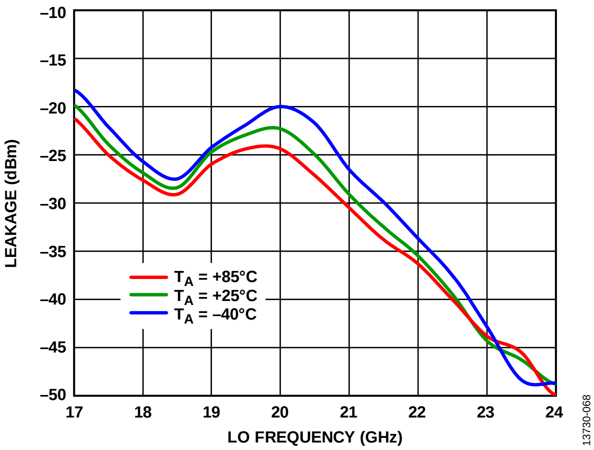

Figure 68. 2× LO Leakage at IF2 vs. LO Frequency at Various Temperatures, LO = 4 dBm

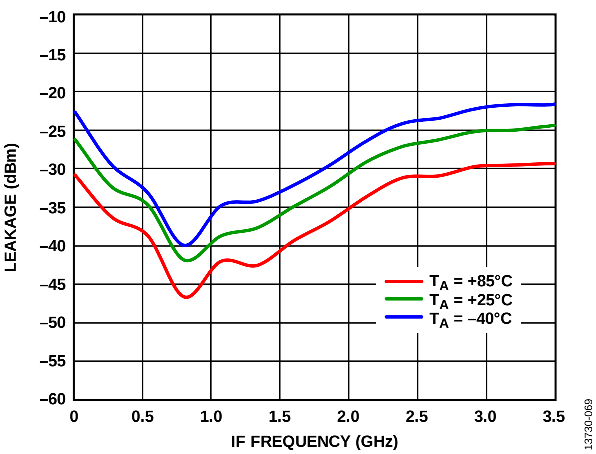

Figure 69. IF2 Leakage at RFOUT vs. IF Frequency at Various Temperatures

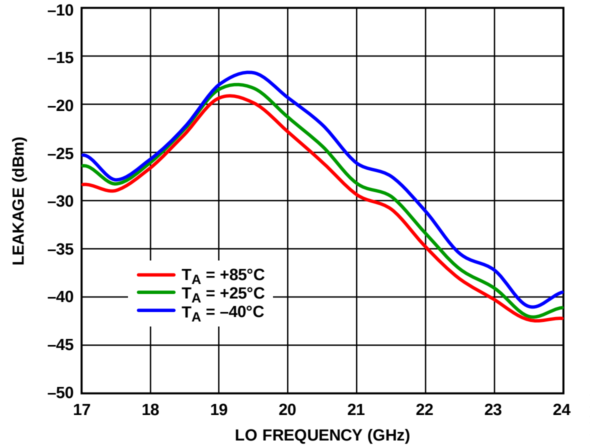

Figure 70. 2× LO Leakage at IF1 vs. LO Frequency at Various Temperatures, LO = 4 dBm

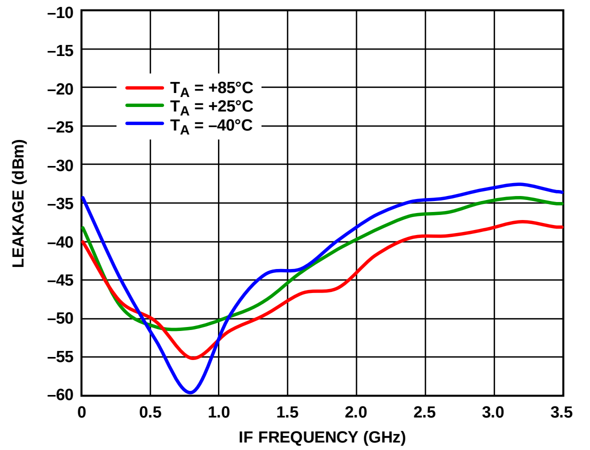

Figure 71. IF1 Leakage at RFOUT vs. IF Frequency at Various Temperatures

RETURN LOSS PERFORMANCE

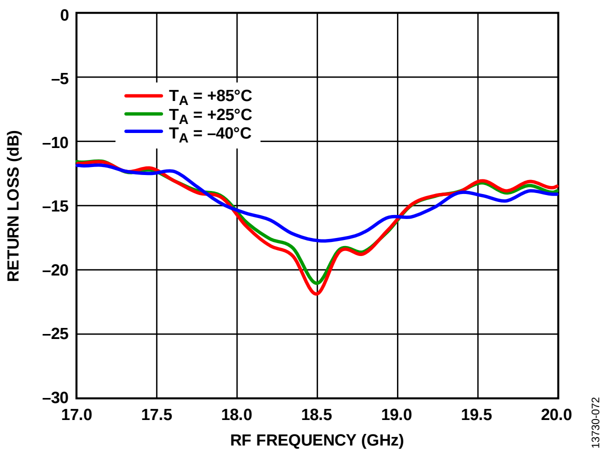

Figure 72. RF Return Loss vs. RF Frequency at Various Temperatures, LO = 4 dBm at LO Frequency = 21 GHz

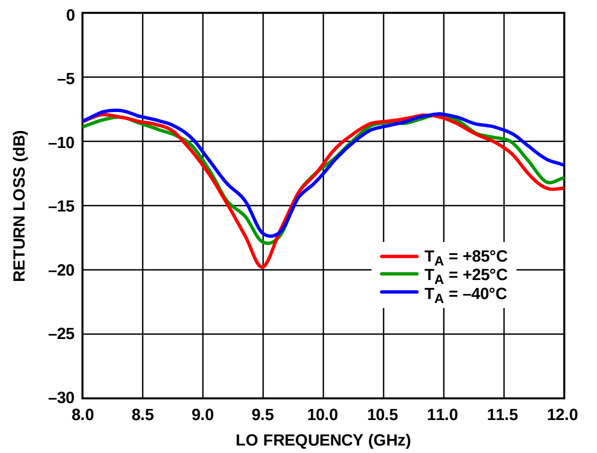

Figure 74. LO Return Loss vs. LO Frequency at Various Temperatures, LO = 4 dBm

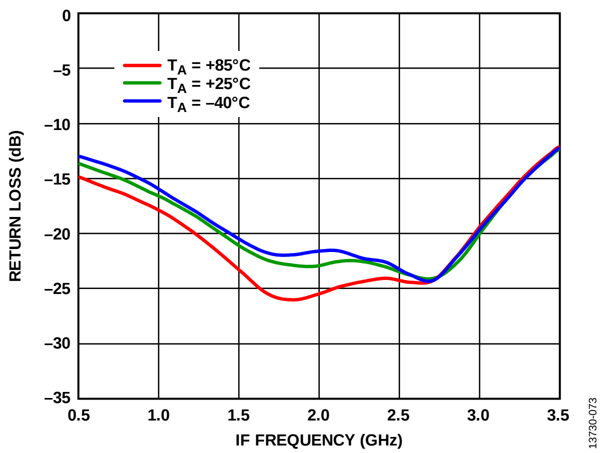

Figure 73. IF1 Return Loss vs. IF Frequency at Various Temperatures, LO = 4 dBm at LO Frequency = 21 GHz

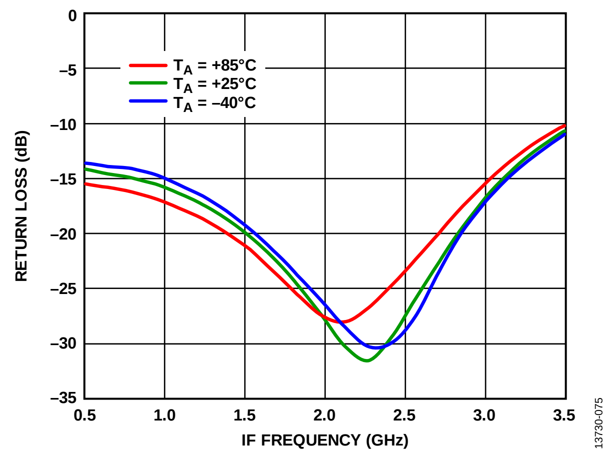

Figure 75. IF2 Return Loss vs. IF Frequency at Various Temperatures, LO = 4 dBm at LO Frequency = 21 GHz

POWER DETECTOR PERFORMANCE

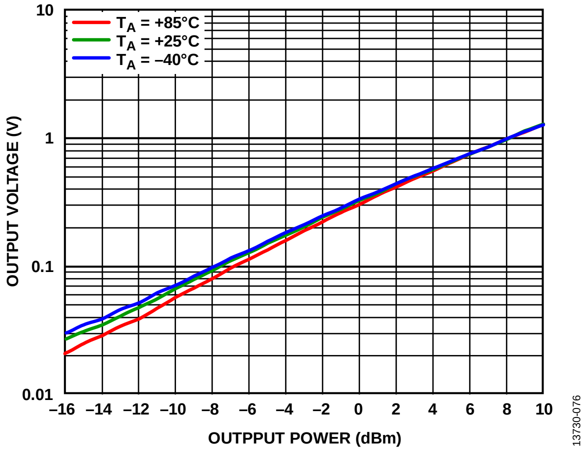

Figure 76. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, LO = 20.5 GHz

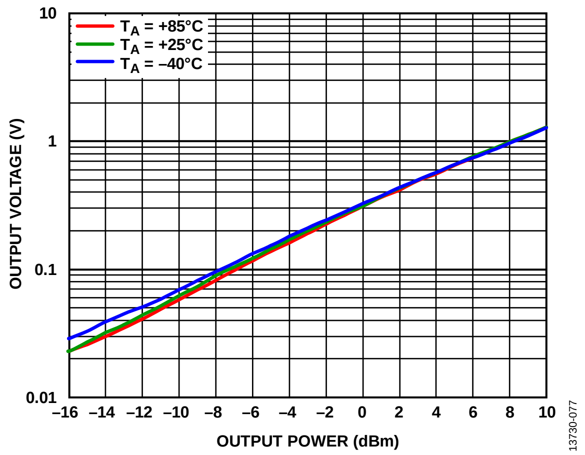

Figure 77. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, LO = 22 GHz

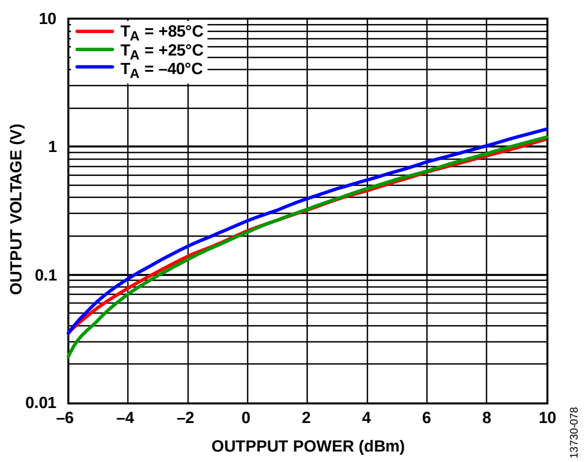

Figure 78. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, LO = 23.5 GHz

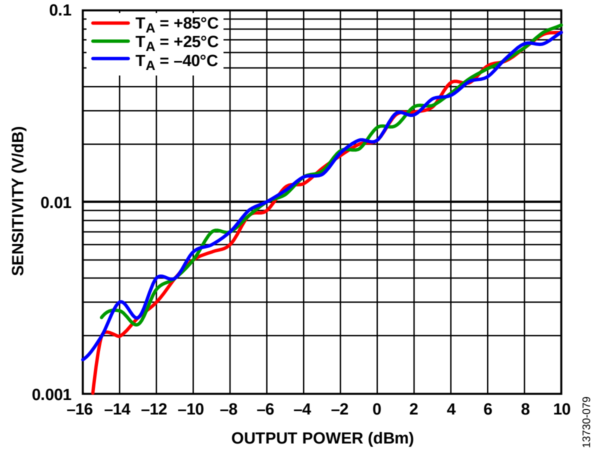

Figure 79. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 20.5 GHz

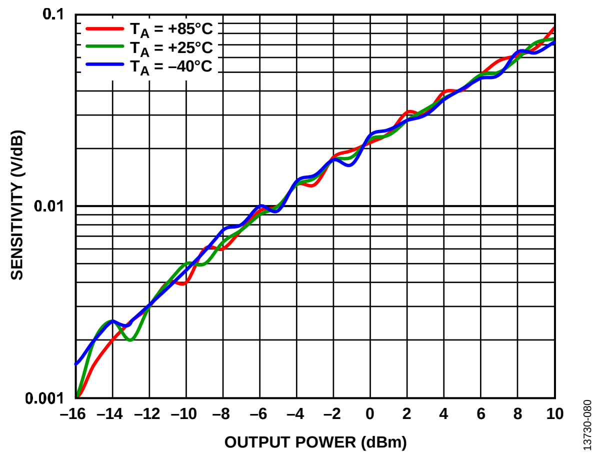

Figure 80. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 22 GHz

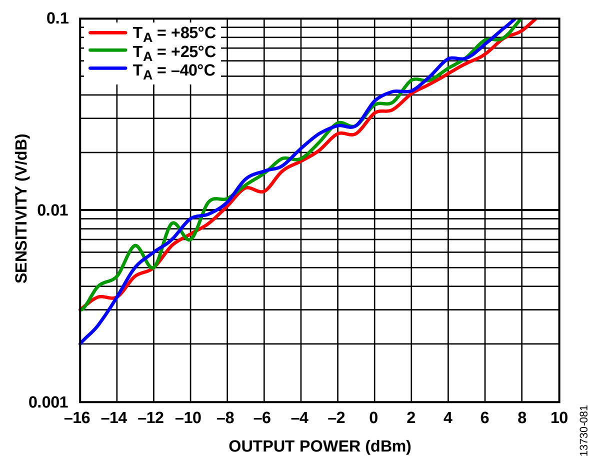

Figure 81. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 23.5 GHz

SPURIOUS PERFORMANCE

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 5 V, V_{DRFx} = 5 V, V_{CTLx} = −5 V, V_{ESD} = −5 V, V_{GMIX} = −0.5 V.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 17 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 18 GHz at LO input power = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	6	58	N/A	N/A	N/A
	1	52	0	45	N/A	N/A	N/A
	2	72	50	42	N/A	N/A	N/A
	3	91	69	71	N/A	N/A	N/A
	4	98	80	79	N/A	N/A	N/A
	5	108	93	87	N/A	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 19 GHz at LO input power = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	7	66	N/A	N/A	N/A
	1	53	0	48	N/A	N/A	N/A
	2	66	48	41	N/A	N/A	N/A
	3	74	78	69	N/A	N/A	N/A
	4	99	88	82	N/A	N/A	N/A
	5	117	102	91	N/A	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 20 GHz at LO input = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	4.8	54	N/A	N/A	N/A
	1	50	0	48	N/A	N/A	N/A
	2	59	45	44	N/A	N/A	N/A
	3	82	77	66	N/A	N/A	N/A
	4	101	95	77	N/A	N/A	N/A
	5	98	103	94	N/A	N/A	N/A

M × N Spurious Output, RF = 19 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 20 GHz at LO input = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	6	56	N/A	N/A	N/A
	1	52	0	50	N/A	N/A	N/A
	2	79	43	52	N/A	N/A	N/A
	3	90	64	69	N/A	N/A	N/A
	4	98	77	79	N/A	N/A	N/A
	5	115	93	85	N/A	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 21 GHz at LO input power = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	4	60	N/A	N/A	N/A
	1	50	0	46	N/A	N/A	N/A
	2	69	45	52	N/A	N/A	N/A
	3	78	68	71	N/A	N/A	N/A
	4	99	79	77	N/A	N/A	N/A
	5	106	90	83	N/A	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 22 GHz at LO input power = 4 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	3	71	N/A	N/A	N/A
	1	51	0	47	N/A	N/A	N/A
	2	66.3	39	53	N/A	N/A	N/A
	3	92	73	71	N/A	N/A	N/A
	4	104	86	81	N/A	N/A	N/A
	5	95	103	88	N/A	N/A	N/A

THEORY OF OPERATION

The HMC7911 is a GaAs, pHEMT, MMIC I/Q upconverter with an integrated LO buffer that upconverts intermediate frequencies between dc to 3.5 GHz to RF between 17 GHz and 20 GHz. LO buffer amplifiers are included on chip to allow a minimum LO drive level of 4 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q singly balanced cores of the passive mixers. The RF output of the I and Q mixers are then summed through an on-chip Wilkinson power combiner and relatively matched to provide a single-ended 50 Ω output signal that is amplified by the RF amplifiers to produce a dc-coupled and 50 Ω matched RF output signal at the RFOUT port. A voltage attenuator precedes the RF amplifiers for desired gain control.

The power detector feature provides a LO cancellation capability to the level of −10 dBm. See Figure 82 for a functional block diagram of the upconverter circuit architecture.

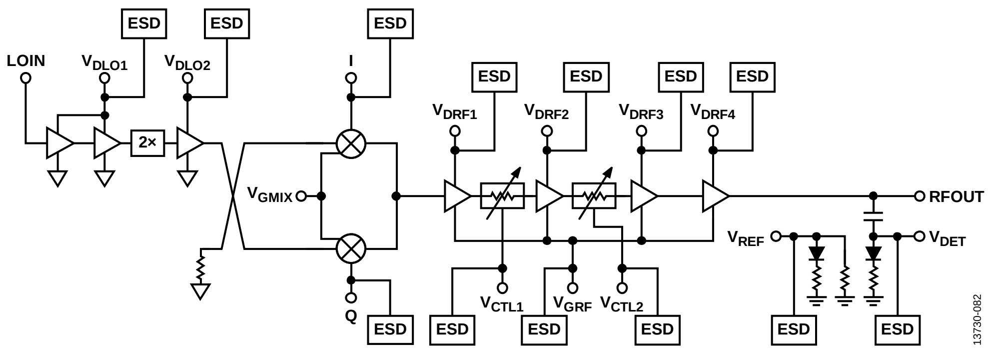

Figure 82. Upconverter Circuit Architecture

APPLICATIONS INFORMATION

A typical lower sideband upconversion circuit is shown in Figure 83. The lower sideband input signal is connected to the input port of the 90° hybrid coupler. The isolated port is loaded to 50 Ω. The external 90° hybrid splits the IF signal into I and Q phase terms. The I and Q input signals enter the HMC7911 on the IF1 and IF2 inputs. IF1 of the device is connected to the 90° port of the hybrid coupler. IF2 is connected to the 0° port of the hybrid coupler. The LO to RF leakage can be improved by applying small dc offsets to the I/Q mixer cores via the V_{DC_IF1} and V_{DC_IF2} inputs. However, it is important to limit the applied dc bias to avoid sourcing or sinking more than ±3 mA of bias current. Depending on the bias sources used, it may be prudent to add series resistance to ensure that the applied bias current does not exceed ±3 mA.

BIASING SEQUENCE

The HMC7911 uses buffer amplifiers in the LO and RF paths. These active stages all use depletion mode pHEMTs. To ensure transistor damage does not occur, use the following power-up bias sequence:

1. Apply a −5 V bias to Pin 27 (V_{ESD}).
2. Apply a −2 V bias to Pin 26 (V_{GRF}), which is a pinched off state.
3. Apply a −0.5 V bias to Pin 1 (V_{GMIX}). This bias can be adjusted from 0.5 V to −1 V depending on the LO power used to provide the optimum IP3 response of the mixer.
4. Apply 5 V to Pin 9 (V_{DLO1}) and Pin 10 (V_{DLO2}).
5. Apply −5 V to Pin 20 (V_{CTL2}) and Pin 21 (V_{CTL1}). Adjust V_{CTL1} and V_{CTL2} between −5 V and 0 V depending on the amount of attenuation desired.
6. Apply 5 V to Pin 18, Pin 19, Pin 22, and Pin 25 (V_{DRF4}, V_{DRF3}, V_{DRF2}, and V_{DRF1}).
7. Adjust Pin 26 (V_{GRF}) between −2 V and 0 V to achieve a total amplifier quiescent drain current of 220 mA.

LOCAL OSCILLATOR NULLING

Broad LO nulling may be required to achieve optimum IP3 and LO to RF isolation performance. This nulling is achieved by applying dc voltages between −0.2 V and +0.2 V to the I and Q ports to suppress the LO signal across the RF frequency band by approximately 5 dBc to 10 dBc. To suppress the LO signal at the RF port, use the following nulling sequence:

1. Adjust V_{DC_IF1} between −0.2 V and +0.2 V and monitor the LO leakage on the RF port. When the desired or maximum level of suppression is achieved, proceed to Step 2.
2. Adjust V_{DC_IF2} between −0.2 V and +0.2 V and monitor the LO leakage on the RF port until either the desired or the maximum level of suppression is achieved.
3. If the desired level of the LO signal on the RF port has still not been achieved, further tune each V_{DC_IF1} and V_{DC_IF2} independently to achieve the desired LO leakage. The resolution of the voltage changed on the voltage of the V_{DC_IF1} and V_{DC_IF2} inputs must be in the millivolt range.

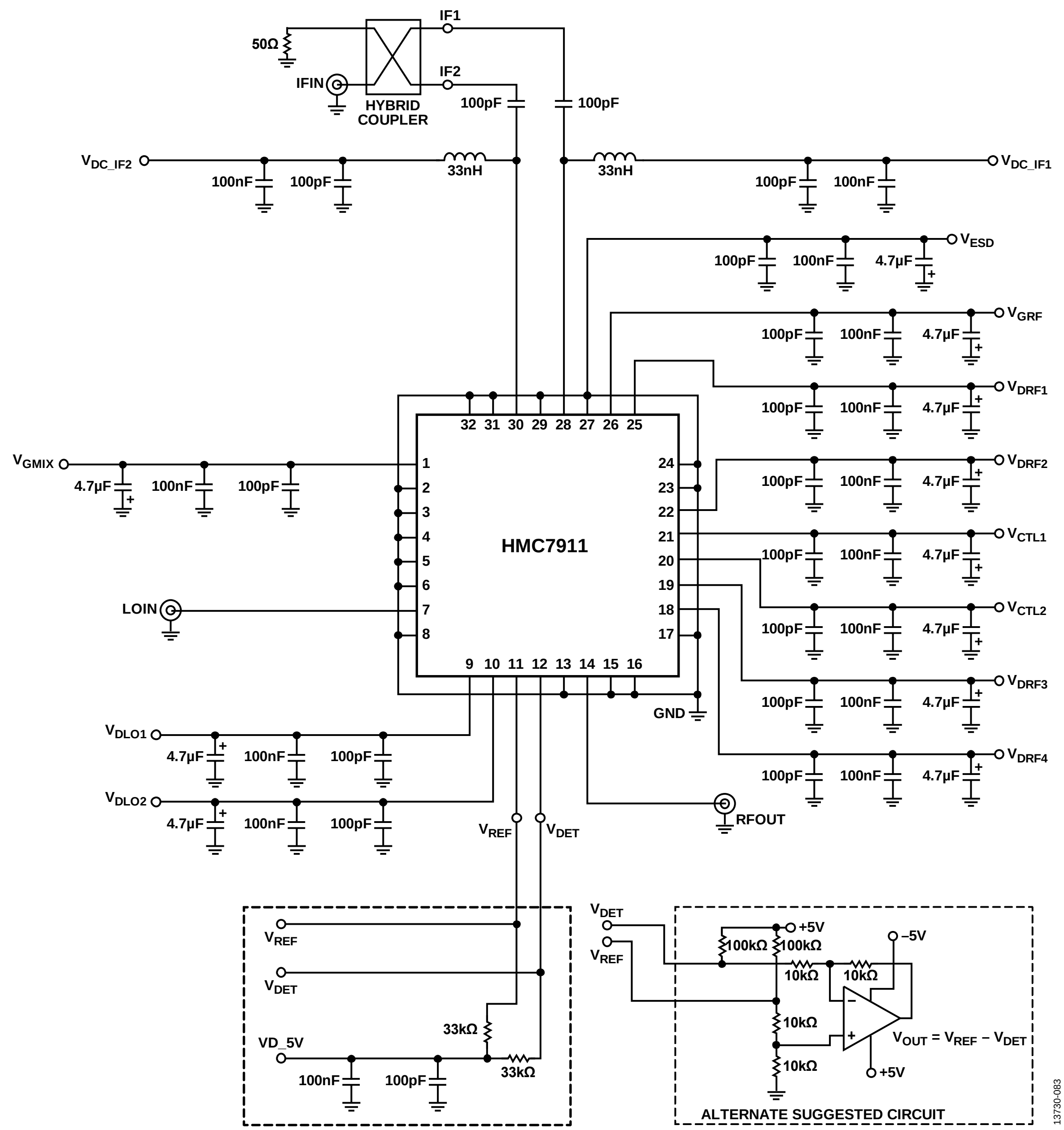

Figure 83. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD

The circuit board used in this application must use RF circuit design techniques. Signal lines must have 50 Ω impedance and the package ground leads and exposed pad must be connected directly to the ground plane similar to that shown in Figure 84.

Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 84 is available from Analog Devices, Inc., upon request.

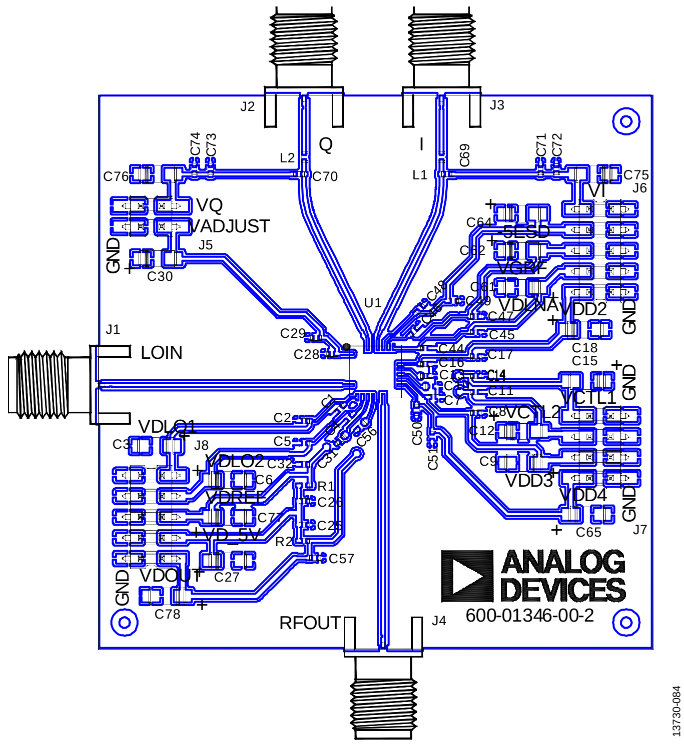

Figure 84. Evaluation Board Top Layer

OUTLINE DIMENSIONS

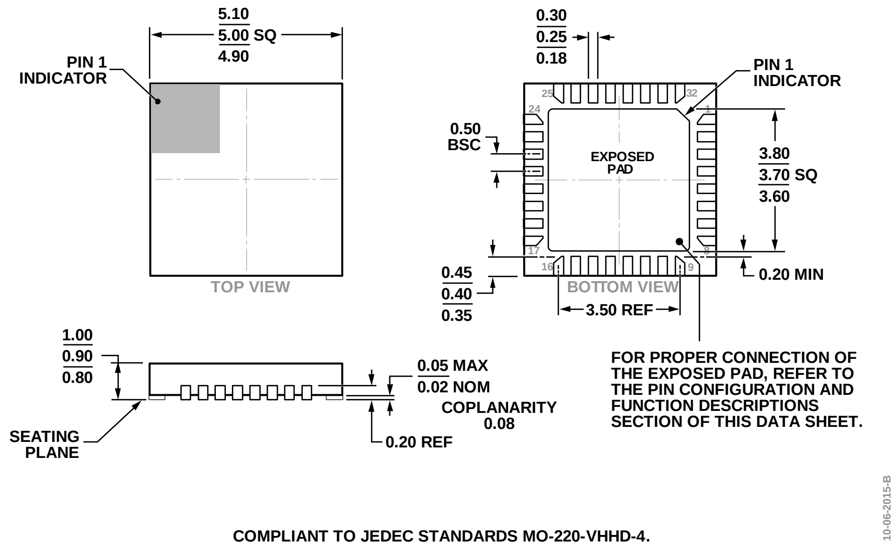

Figure 85. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.90 mm Package Height
(HCP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC7911LP5E	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-32-3
HMC7911LP5ETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-32-3
EV1HMC7911LP5			Evaluation Assembly Board	

[1] HMC7911LP5E and HMC7911LP5ETR are RoHS Compliant Parts.
[2] The peak reflow temperature is 260°C. See the Absolute Maximum Ratings section, Table 2.

D13730-0-6/16(A)