Terminal Voltage 0V to 13.2V, 128 Taps Up/Down Interface

The Intersil ISL95310 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by an Up/Down interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The wiper of each potentiometer has an associated volatile Wiper Counter Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper on the resistor array through the switches. At power-up, the device recalls the contents of the default data registers to the corresponding WR. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- LCD contrast control
- Parameter and bias adjustments
- Mechanical potentiometer replacement
- Industrial and automotive control

Ordering Information

PART NUMBER	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
ISL95310WIU10Z (See Note) **(No longer available, recommended replacement: ISL95310UIU10Z-TK)**	10K	-40 to +85	10 Ld MSOP
ISL95310UIU10Z (See Note)	50K	-40 to +85	10 Ld MSOP

Add “-TK” suffix for tape and reel.

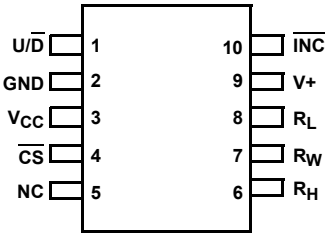
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

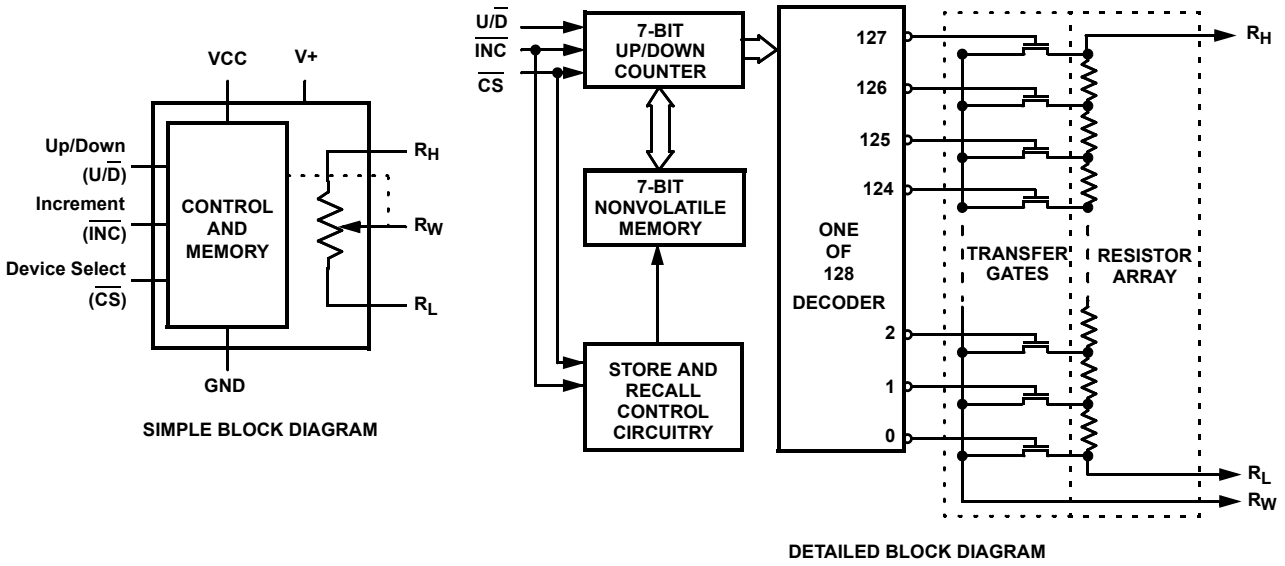
- Non-volatile solid-state potentiometer
- Up/down interface with chip select enable
- DCP terminal voltage, 0 to +13.2V
- 128 wiper tap points - 0.8% resolution
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 127 resistive elements
  - Temperature compensated
  - Low wiper resistance 70Ω typical @ 3.3V
- Low power CMOS
  - Standby current, 2µA at V_{CC} = +3.6V
- High reliability
  - Endurance, 200,000 data changes per bit
  - Register data retention 50 years @ T ≤ 75°C
- R_{TOTAL} values = 10kΩ, 50kΩ
- 10-lead MSOP package
  - Pb-free plus anneal available (RoHS compliant)

Pinout

ISL95310
(10 LD MSOP)
TOP VIEW



Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	$U/\overline{D}$	Controls the direction of wiper movement and whether the counter is incremented or decremented
2	GND	Ground
3	V_{CC}	Positive logic supply voltage
4	$\overline{CS}$	Chip select; the device is selected when the $\overline{CS}$ input is LOW; also used to initiate a nonvolatile store
5	NC	No connect; pin is to be left unconnected
6	R_H	A fixed terminal for one end of the potentiometer resistor
7	R_W	The wiper terminal which is equivalent to the movable terminal of a potentiometer
8	R_L	A fixed terminal for one end of the potentiometer resistor
9	V+	Positive bias voltage for the potentiometer wiper control
10	$\overline{INC}$	Increment input; negative edge triggered

Absolute Maximum Ratings

Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$
with respect to GND . . . . . -0.3V to V_{CC} +0.3V
Voltage on V+ (referenced to GND) . . . . . +13.2V
$\Delta V = |V_{(RH)}-V_{(RL)}|$ . . . . . V+
R_H, R_L, R_W . . . . . V+
Lead temperature (soldering 10s) . . . . . +300°C
I_W (10s) . . . . . ±6mA
V_{CC} . . . . . -0.3V to +6V
Power rating of each DCP 20mW

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
V+ . . . . . 8.0V to 13.2V
Wiper current of each DCP . . . . . ±3.0mA

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog Specifications Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L resistance tolerance		-20		+20	%
V_{RH}	R_H terminal voltage	V_{RL} = 0V	0		V+	V
R_W	Wiper resistance	V+ = 12V, wiper current = V+ / R_{TOTAL}		70	200	Ω
$C_H/C_L/C_W$	Potentiometer Capacitance (Note 13)			10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins	Voltage at pin from GND to V+		0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ R_L; V+ @ R_H; measured at R_W, unloaded)						
INL (Note 6)	Integral non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential non-linearity	W option	-0.75		0.75	LSB (Note 2)
		U option	-0.5		0.5	
ZSerror (Note 3)	Zero-scale error	U option	0	1	7	LSB (Note 2)
		W option	0	0.5	2	
FSerror (Note 4)	Full-scale error	U option	-7	-1	0	LSB (Note 2)
		W option	-2	-1	0	
TC_V (Note 7)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 11)	Integral non-linearity	DCP register set between 20 hex and 7F hex; monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential non-linearity	W option	-0.75		0.75	MI (Note 8)
		U option	-0.5		0.5	
Roffset (Note 9)	Offset	DCP Register set to 00 hex, W option	0	1	7	MI (Note 8)
		DCP Register set to 00 hex, U option	0	0.5	2	MI (Note 8)
TC_R (Note 12)	Resistance Temperature Coefficient	DCP register set between 20 hex and 7F hex		±45		ppm/°C

Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
I_{CC1}	V_{CC} supply current, volatile write/read	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and INC = 0.4V/2.4V min; t_{CYC} R_L, R_H, R_W not connected			1	mA
I_{CC2}	V_{CC} supply current, nonvolatile write	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and INC = 0.4V/2.4V min; t_{CYC} R_L, R_H, R_W not connected			3	mA
I_{SB}	V_{CC} current, standby	V_{CC} = +5.5V, 2-wire interface in standby state			5	µA
		V_{CC} = +3.6V, 2-wire interface in standby state			2	µA
I_{V+}	V+ bias current	V+ = 13.2V; V_{CC} = +5.5V			1	µA
I_{LkgDig}	Leakage current, at pins $\overline{INC}$, $\overline{CS}$, U/$\overline{D}$, A0, and A1 pins	Voltage at pin from GND to V_{CC}	-10		10	µA
I_{LI}	CS input leakage current	V_{IN} = V_{CC}			±1	µA
		V_{CC} = 3V, $\overline{CS}$ = 0	60	100	150	µA
		V_{CC} = 5V, $\overline{CS}$ = 0	120	200	250	µA
I_{V+}	V+ bias current	V+ = 13.2V; V_{CC} = +5.5V			1	µA
t_{DCP} (Note 13)	DCP wiper response time	$\overline{INC}$ falling edge of last bit of DCP data byte to wiper change			1	µs
Vpor (Note 13)	Power-on recall voltage	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V
V_{CC} Ramp (Note 13)	V_{CC} ramp rate		0.2			V/ms
t_D (Note 13)	Power up delay	V_{CC} above Vpor, to DCP initial value register recall completed, and 2-wire Interface in standby state			3	ms
EEPROM SPECS						
	EEPROM endurance		150,000			Cycles
	EEPROM retention	Temperature ≤ 75°C	50			Years
SERIAL INTERFACE SPECS						
V_{IL}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$		-0.3		0.3* V_{CC}	V
V_{IH}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$		0.7* V_{CC}		V_{CC}+ 0.3	V
Hysteresis (Note 13)	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ input buffer hysteresis		0.05* V_{CC}			V
Cpin (Note 13)	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ pin capacitance				10	pF

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID} (Note 13)	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI} (Note 13)	U/$\overline{D}$ to $\overline{INC}$ setup	1			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs

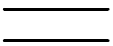
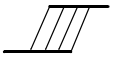
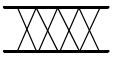
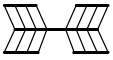
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated **(Continued)**

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNIT
t_{CPHS}	$\overline{CS}$ deselect time (STORE)	20			ms
t_{CPHNS} (Note 13)	$\overline{CS}$ deselect time (NO STORE)	1			µs
t_{IW} (Note 13)	$\overline{INC}$ to R_W change		100	500	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F (Note 13)	$\overline{INC}$ input rise and fall time			500	µs

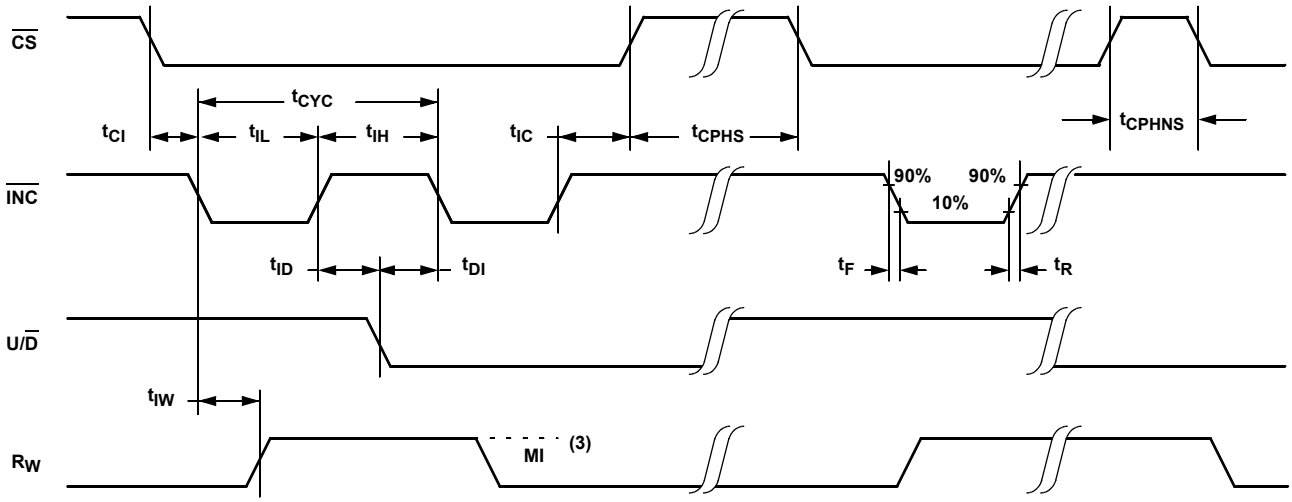
NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(R_W)_0$/LSB.
4. FS error = $[V(R_W)_{127} – V+]$/LSB.
5. DNL = $[V(R_W)_i – V(R_W)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(R_W)_i – (i • LSB – V(R_W)_0)$ for i = 1 to 127.
7. $$TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)] \S 2} x \frac{10^6}{125°C}$$
   for i = 16 to 120 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0|$ /127. R_{127} and R_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
9. Roffset = R_0/MI, when measuring between R_W and R_L.
   Roffset = R_{127}/MI, when measuring between R_W and R_H.
10. RDNL = $(R_i – R_{i-1})$/MI, for i = 16 to 127.
11. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 16 to 127.
12. $$TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)] \S 2} \times \frac{10^6}{125°C}$$
    for i = 16 to 127, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.
14. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a 3-wire serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. Timing



Power Up and Down Requirements

In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up. The potentiometer voltages must be applied after this sequence is completed. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect.

Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the ISL95310 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the ISL95310 will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the ISL95310: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 127 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

On applying power to the ISL95310, the V_{CC} supply should have a monotonic ramp to the specified operating voltage. It is important that once V_{CC} reaches 1V that it increases to at least 2.5V in less than 7.5ms (0.2V/ms). The ramp rate before and after these thresholds is not important.

V_{CC} must be applied prior to, or simultaneously, with V+. Under no condition should V+ be applied without V_{CC}. While the sequence of applying V+ and V_{CC} to the ISL95310 does not affect the proper recall of the wiper position, applying V+ before V_{CC} powers the electronic switches of the DCP before the electronic switch control signals are applied. This can result in multiple electronic switches being turned on, which could load the power supply and cause brief, unexpected potentiometer wiper settings.

To prevent unknown wiper positions on the ISL95310 on power down, it is recommended that V+ turn off before or simultaneously with V_{CC}. If V+ remains on after V_{CC} turns off, the wiper position can remain unchanged from its previous setting or it can go to an undefined state.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the ISL95310, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained. During initial power-up $\overline{CS}$ must go high along with or before V_{CC} to avoid an accidental store generation.

TABLE 1. MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down
↗	H	X	Store wiper position
H	X	X	Standby current
↗	L	X	No store, return to standby
H	H	X	Standby
↘	L	H	Wiper up one position (not recommended)
↘	L	L	Wiper down one position (not recommended)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 27, 2015	FN8083.1	- Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. -Updated POD M10.118 to most current version change is as follows: Added land pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

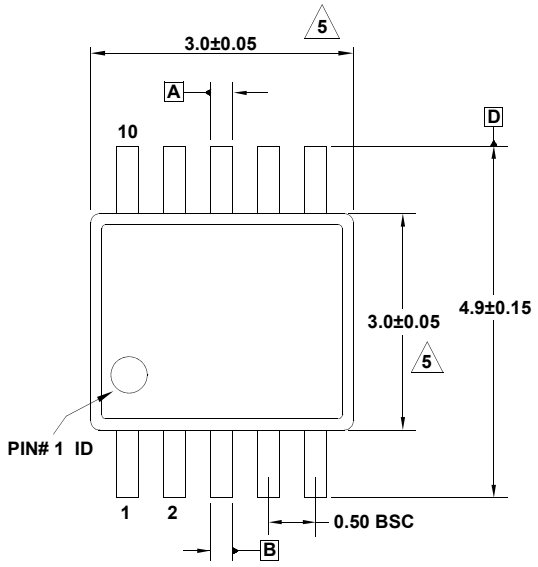
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

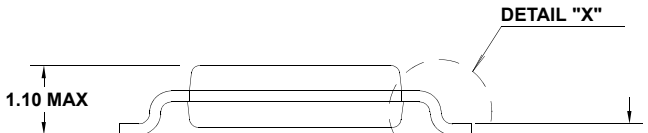
M10.118

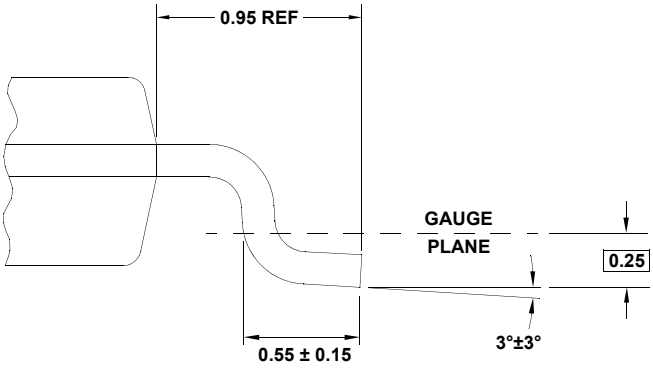
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 4/12

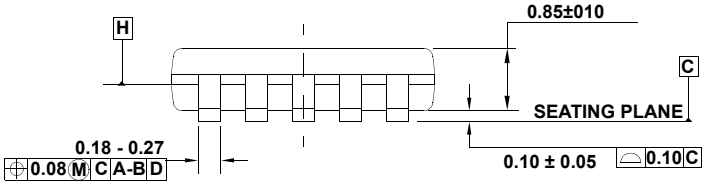


TOP VIEW

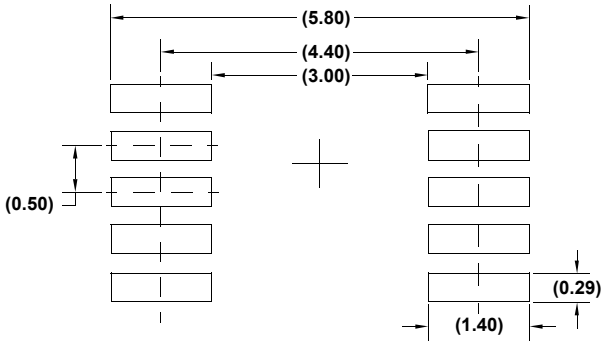




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.