



### FEATURES

- 40 MHz correlated double sampler (CDS)
- 0 dB to 18 dB, 9-bit variable gain amplifier (VGA)
- 40 MSPS analog-to-digital converter (ADC)
- Optical black clamp (CLPOB) with variable level control
- Complete on-chip timing driver
- Precision Timing core with <550 ps resolution
- On-chip 3 V horizontal and RG drivers
- 4-phase H-clock mode
- 100-lead, 9 mm × 9 mm, CSP\_BGA package

### APPLICATIONS

- Signal processor for dual-channel CCD outputs
- Digital still cameras
- Digital video cameras
- High speed digital imaging applications

### GENERAL DESCRIPTION

The AD9942 is a highly integrated dual-channel CCD signal processor for digital still camera applications. Each channel is specified at pixel rates of up to 40 MHz. The AD9942 consists of a complete analog front end with analog-to-digital conversion, combined with a programmable timing driver. The Precision Timing core allows high speed clocks to be adjusted with 550 ps resolution.

The analog front end uses black level clamping and includes a VGA, a 40 MSPS ADC, and a CDS. The timing driver provides the high speed CCD clock drivers for RG\_A and RG\_B, as well as the H1A to H4A and H1B to H4B outputs. The 6-wire serial interface is used to program the AD9942.

Available in a space-saving, 9 mm × 9 mm, CSP\_BGA package, the AD9942 is specified over an operating temperature range of -25°C to +85°C.

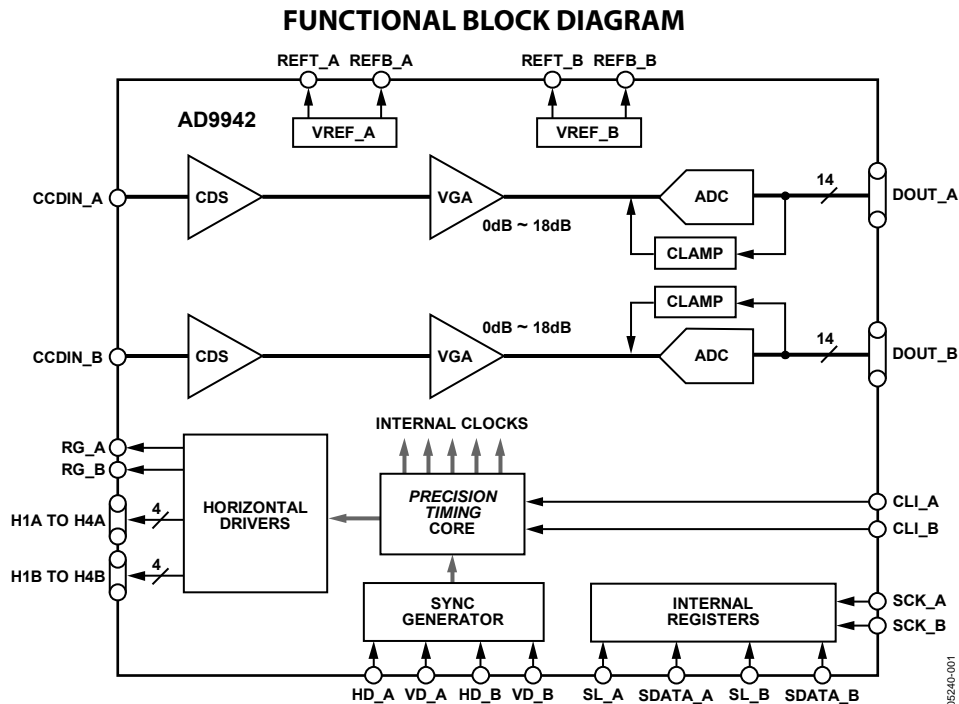


Figure 1.

#### Rev. A

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## DOCUMENTATION

### Data Sheet

- AD9942: Dual-Channel, 14-Bit, CCD Signal Processor with *Precision Timing™* Core Data Sheet

## DESIGN RESOURCES

- AD9942 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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## REVISION HISTORY

### 8/06—Rev. 0 to Rev. A

Changes to Table 3.....	5
Changes to Table 13.....	17
Change to Channel A and Channel B Variable Gain Amplifier Section.....	28
Updated Outline Dimensions .....	33

### 1/05—Revision 0: Initial Version

## SPECIFICATIONS

### GENERAL SPECIFICATIONS

X = A, B.

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	-25		+85	°C
Storage	-65		+150	°C
MAXIMUM CLOCK RATE	40			MHz
POWER SUPPLY VOLTAGE				
AVDD_X, TCVDD_X (AFE, Timing Core)	2.7	3.0	3.6	V
HVDD_X (H1X to H4X Drivers)	2.7	3.0	3.6	V
RGVDD_X (RG_X Driver)	2.7	3.0	3.6	V
DRVDD_X (D0 to D13 Drivers)	2.7	3.0	3.6	V
DVDD_X (Digital)	2.7	3.0	3.6	V
POWER DISSIPATION FOR EACH CHANNEL (40 MHz, 3 V Supplies, 100 pF H1X to H4X Loading, 10 pF RG_X Loading)				
Power from AVDD_X		110		mW
Power from TCVDD_X		33		mW
Power from HVDD_X <sup>1</sup>		160		mW
Power from RGVDD_X		13		mW
Power from DRVDD_X		15		mW
Power from DVDD_X		40		mW
Total Shutdown Mode		2		mW

<sup>1</sup> Total HVDD\_X Power =  $[(C_{LOAD}) \times (HVDD\_X) \times (\text{Pixel Frequency})] \times (HVDD\_X) \times (\text{Number of Horizontal Outputs Used})$ .

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## DIGITAL SPECIFICATIONS

$T_{MIN}$  to  $T_{MAX}$ ,  $AVDD\_X = DVDD\_X = DRVDD\_X = HVDD\_X = RGVDD\_X = 2.7$  V,  $C_L = 20$  pF, unless otherwise noted.  
X = A, B.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	$V_{IH}$	2.1			V
Low Level Input Voltage	$V_{IL}$			0.6	V
High Level Input Current	$I_{IH}$		10		$\mu$ A
Low Level Input Current	$I_{IL}$		10		$\mu$ A
Input Capacitance	$C_{IN}$		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, $I_{OH} = 2$ mA	$V_{OH}$	2.2			V
Low Level Output Voltage, $I_{OL} = 2$ mA	$V_{OL}$			0.5	V
CLI INPUT					
High Level Input Voltage ( $TCVDD\_X/2 + 0.5$ V)	$V_{IH-CLI}$	1.85			V
Low Level Input Voltage	$V_{IL-CLI}$			0.85	V
RG_X AND H1X TO H4X DRIVER OUTPUTS					
High Level Output Voltage ( $RGVDD\_X - 0.5$ V and $HVDD\_X - 0.5$ V)	$V_{OH}$	2.2			V
Low Level Output Voltage	$V_{OL}$			0.5	V
Maximum Output Current (Programmable)			30		mA
Maximum Load Capacitance		100			pF

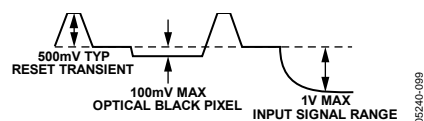
## ANALOG SPECIFICATIONS

$T_{MIN}$  to  $T_{MAX}$ ,  $AVDD\_X = DVDD\_X = 3.0$  V,  $f_{CL1} = 40$  MHz, typical timing specifications, unless otherwise noted. X = A, B.

Table 3.

Parameter	Min	Typ	Max	Unit	Notes
CDS					
Gain		0		dB	
Allowable CCD Reset Transient <sup>1</sup>		500		mV	
Max Input Range Before Saturation	1.0			V p-p	
Max CCD Black Pixel Amplitude		±100		mV	Measured at 12 dB VGA gain (Typ = 70 mV at 15 dB and 50 mV at 18 dB)
VARIABLE GAIN AMPLIFIER (VGA_X)					
Max Input Range	1.0			V p-p	
Max Output Range	2.0			V p-p	
Gain Control Resolution		512		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Min Gain (Code 0)		0		dB	
Max Gain (Code 511)		18		dB	
CLPOB					
Clamp Level Resolution		256		Steps	4 LSB/step
Clamp Level					Measured at ADC output
Min Clamp Level		0		LSB	
Max Clamp Level		1023		LSB	
CHN_A AND CHN_B ADC					
Differential Nonlinearity (DNL)	-1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT_X)		2.0		V	
Reference Bottom Voltage (REFB_X)		1.0		V	
SYSTEM PERFORMANCE					
VGA Gain Accuracy					Specifications include entire signal chain
Min Gain (Code 0)	-0.5	0	+0.5	dB	
Max Gain (Code 511)	17.5	18	18.5	dB	
Peak Nonlinearity, 500 mV Input Signal		0.15		%	12 dB gain applied
Total Output Noise		3		LSB rms	AC grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply

<sup>1</sup> Input signal characteristics defined as follows:



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## CHANNEL-TO-CHANNEL SPECIFICATIONS

T<sub>MIN</sub> to T<sub>MAX</sub>, AVDD\_X = DVDD\_X = 3.0 V, f<sub>CL1</sub> = 40 MHz, typical timing specifications, unless otherwise noted. X = A, B.

Table 4.

Parameter	Min	Typ	Max	Unit	Notes
CHANNEL A/CHANNEL B OUTPUT CODE MATCHING ERROR <sup>1</sup>		<1.0%			VGA = 6 dB, 12 dB, and 18 dB conditions.
CROSSTALK ERROR					VGA = 6 dB, 12 dB, and 18 dB conditions.
Channel A to Channel B		-84		dB	Full-scale step applied to Channel A while measuring response on Channel B.
Channel B to Channel A		-84		dB	Full-scale step applied to Channel B while measuring response on Channel A.

<sup>1</sup> Matching error calculated using a ramp input applied to Channel A and Channel B simultaneously. Typical Channel A/Channel B error is <1.0% at each output code.

**TIMING SPECIFICATIONS**

$C_L = 20$  pF,  $f_{CLI} = 40$  MHz, serial timing in Figure 14 and Figure 15, unless otherwise noted. X = A, B.

**Table 5.**

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK (CLI_X) (See Figure 16)					
CLI_X Clock Period		25.0			ns
CLI_X High/Low Pulse Width	$t_{ADC}$	10.0	12.5	15.0	ns
Delay from CLI_X to Internal Pixel Period Position (See Figure 16)	$t_{CLIDLY}$		6		ns
CLPOB_X PULSE WIDTH (Programmable) <sup>1</sup>	$t_{COB}$	2	20		Pixels
SAMPLE CLOCKS (See Figure 17)					
SHP_X Rising Edge to SHD_X Rising Edge	$t_{S1}$	11.2	12.5		ns
DATA OUTPUTS (See Figure 19 and Figure 20)					
Output Delay from Programmed Edge	$t_{OD}$		6		ns
Pipeline Delay			11		Cycles
SERIAL INTERFACE					
Maximum SCK_X Frequency	$f_{SCLK}$	10			MHz
SL_X to SCK_X Setup Time	$t_{LS}$	10			ns
SCK to SL_X Hold Time	$t_{LH}$	10			ns
SDATA_X Valid to SCK_X Rising Edge Setup	$t_{DS}$	10			ns
SCK_X Falling Edge to SDATA_X Valid Hold	$t_{DH}$	10			ns
SCK_X Falling Edge to SDATA_X Valid Read	$t_{DV}$	10			ns

<sup>1</sup> Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp reference.



## ABSOLUTE MAXIMUM RATINGS

Table 6. Ratings (X = A, B)

Parameter	Rating
AVDD_X and TCVDD_X to AVSS_X	-0.3 V to +3.9 V
HVDD_X and RGVDD_X to HVSS_X and RGVSS_X	-0.3 V to +3.9 V
DVDD_X and DRVDD_X to DVSS_X and DRVSS_X	-0.3 V to +3.9 V
Any VSS_X to Any VSS_X	-0.3 V to +0.3 V
Digital Outputs to DRVSS_X	-0.3 V to DRVDD + 0.3 V
SCK_X, SL_X, and SDATA_X to DVSS_X	-0.3 V to DVDD + 0.3 V
RG_X to RGVSS_X	-0.3 V to RGVDD + 0.3 V
H1X to H4X to HVSS_X	-0.3 V to HVDD + 0.3 V
REFT_X, REFB_X, and CCDIN_X to AVSS_X	-0.3 V to AVDD + 0.3 V
Junction Temperature	150°C
Lead Temperature (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

100-lead, 9 mm × 9 mm, CSP\_BGA package:  $\theta_{JA} = 38.3^{\circ}\text{C}/\text{W}^1$

<sup>1</sup>  $\theta_{JA}$  is measured using a 4-layer PCB with the exposed paddle soldered to the board.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

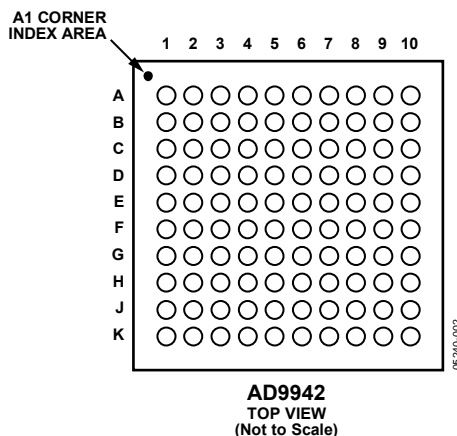


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Ball Location	Mnemonic	Type <sup>1</sup>	Description
B2	SL_A	DI	6-Wire Serial Load for Channel A
C2	SDATA_A	DI	6-Wire Serial Data for Channel A
D2	SCK_A	DI	6-Wire Serial Clock for Channel A
C1	REFT_A	AO	Reference Top Decoupling for Channel A (decouple with 1.0 $\mu$ F to AVSS_A)
D1	REFB_A	AO	Reference Bottom Decoupling for Channel A (decouple with 1.0 $\mu$ F to AVSS_A)
A1	CCDIN_A	AI	Analog Input for Channel A CCD Signal (connect through series 0.1 $\mu$ F capacitor)
F4	H1A	DO	CCD Horizontal Clock 1 for Channel A
F3	H2A	DO	CCD Horizontal Clock 2 for Channel A
D4	H3A	DO	CCD Horizontal Clock 3 for Channel A
D3	H4A	DO	CCD Horizontal Clock 4 for Channel A
B4	RG_A	DO	CCD Reset Gate Clock for Channel A
J2	DRVSS_A	P	Digital Driver Ground for Channel A
K3	DRVDD_A	P	Digital Driver Supply for Channel A
E3	HVSS_A	P	H1A to H4A Driver Ground for Channel A
E4	HVDD_A	P	H1A to H4A Driver Supply for Channel A
C3	RGVSS_A	P	RG_A Driver Ground for Channel A
C4	RGVDD_A	P	RG_A Driver Supply for Channel A
B3	TCVSS_A	P	Analog Ground for Channel A Timing Core
A4	TCVDD_A	P	Analog Supply for Channel A Timing Core
B1	AVSS_A	P	Analog Ground for Channel A
A2	AVDD_A	P	Analog Ground for Channel A
F2	DVSS_A	P	Digital Ground for Channel A
F1	DVDD_A	P	Digital Supply for Channel A
E2	VD_A	DI	Vertical Sync Pulse for Channel A
E1	HD_A	DI	Horizontal Sync Pulse for Channel A
B8	SL_B	DI	6-Wire Serial Load for Channel B
C8	SDATA_B	DI	6-Wire Serial Data for Channel B
D8	SCK_B	DI	6-Wire Serial Clock for Channel B
C7	REFT_B	AO	Reference Top Decoupling for Channel B (decouple with 1.0 $\mu$ F to AVSS_B)
D7	REFB_B	AO	Reference Bottom Decoupling for Channel B (decouple with 1.0 $\mu$ F to AVSS_B)
A7	CCDIN_B	AI	Analog Input for Channel B CCD Signal (connect through series 0.1 $\mu$ F capacitor)
F10	H1B	DO	CCD Horizontal Clock 1 for Channel B
F9	H2B	DO	CCD Horizontal Clock 2 for Channel B
D10	H3B	DO	CCD Horizontal Clock 3 for Channel B

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Ball Location	Mnemonic	Type <sup>1</sup>	Description
D9	H4B	DO	CCD Horizontal Clock 4 for Channel B
B10	RG_B	DO	CCD Reset Gate Clock for Channel B
J8	DRVSS_B	P	Digital Driver Ground for Channel B
K9	DRVDD_B	P	Digital Driver Supply for Channel B
E9	HVSS_B	P	H1B to H4B Driver Ground for Channel B
E10	HVDD_B	P	H1B to H4B Driver Supply for Channel B
C9	RGVSS_B	P	RG_B Driver Ground for Channel B
C10	RGVDD_B	P	RG_B Driver Supply for Channel B
B9	TCVSS_B	P	Analog Ground for Channel B Timing Core
A10	TCVDD_B	P	Analog Supply for Channel B Timing Core
B7	AVSS_B	P	Analog Ground for Channel B
A8	AVDD_B	P	Analog Ground for Channel B
F8	DVSS_B	P	Digital Ground for Channel B
F7	DVDD_B	P	Digital Supply for Channel B
E8	VD_B	DI	Vertical Sync Pulse for Channel B
E7	HD_B	DI	Horizontal Sync Pulse for Channel B
A3	CLI_A	DI	Master Clock Input for Channel A
G1	D0_A	DO	Data Output Channel A
H1	D1_A	DO	Data Output Channel A
J1	D2_A	DO	Data Output Channel A
K1	D3_A	DO	Data Output Channel A
G2	D4_A	DO	Data Output Channel A
H2	D5_A	DO	Data Output Channel A
K2	D6_A	DO	Data Output Channel A
G3	D7_A	DO	Data Output Channel A
H3	D8_A	DO	Data Output Channel A
J3	D9_A	DO	Data Output Channel A
K4	D10_A	DO	Data Output Channel A
J4	D11_A	DO	Data Output Channel A
H4	D12_A	DO	Data Output Channel A
G4	D13_A	DO	Data Output Channel A
A5, B5, C5, D5, E5, F5, G5, H5, J5, K5, A6, B6, C6, D6, E6, F6, G6, H6, J6, K6	GND	P	Ground Connection
A9	CLI_B	DI	Master Clock Input for Channel B
G7	D0_B	DO	Data Output Channel B
H7	D1_B	DO	Data Output Channel B
J7	D2_B	DO	Data Output Channel B
K7	D3_B	DO	Data Output Channel B
G8	D4_B	DO	Data Output Channel B
H8	D5_B	DO	Data Output Channel B
K8	D6_B	DO	Data Output Channel B
G9	D7_B	DO	Data Output Channel B
H9	D8_B	DO	Data Output Channel B
J9	D9_B	DO	Data Output Channel B
K10	D10_B	DO	Data Output Channel B
J10	D11_B	DO	Data Output Channel B
H10	D12_B	DO	Data Output Channel B
G10	D13_B	DO	Data Output Channel B

<sup>1</sup> AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power.

## TERMINOLOGY

### Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes must be present over all operating conditions.

### Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9942 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

### Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1 \text{ LSB} = (\text{ADC full scale} / 2^n \text{ codes})$$

where  $n$  is the bit resolution of the ADC. For the AD9942, 1 LSB is approximately 122.0  $\mu\text{V}$ .

### Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

### Matching Error

The matching error refers to the Channel A to Channel B mismatch after post-ADC correction calibration has been applied to remove gain error between Channel A and Channel B.

### Crosstalk

The crosstalk is measured while applying a full-scale step to one channel and measuring the interference on the opposite channel.

$$\text{Crosstalk (dB)} = 20 \times \log \left( \frac{\text{Interference (LSB)}}{16,384} \right)$$

## EQUIVALENT INPUT/OUTPUT CIRCUITS

X = A, B.

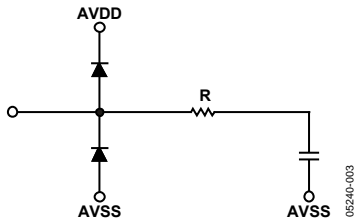


Figure 3. CCDIN\_X

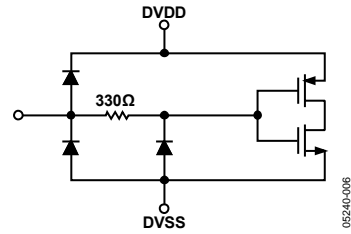


Figure 6. Digital Inputs

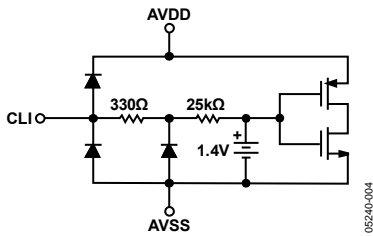


Figure 4. CLI\_X

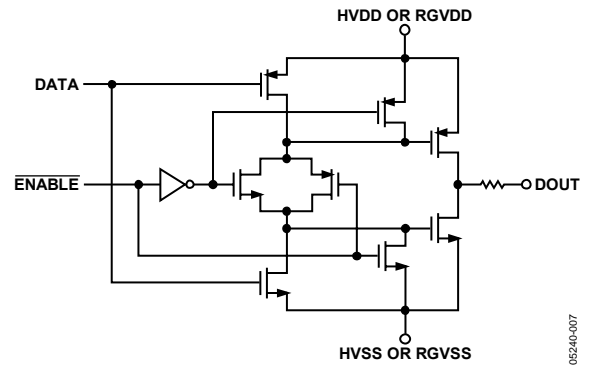


Figure 7. H1X to H4X and RG\_X

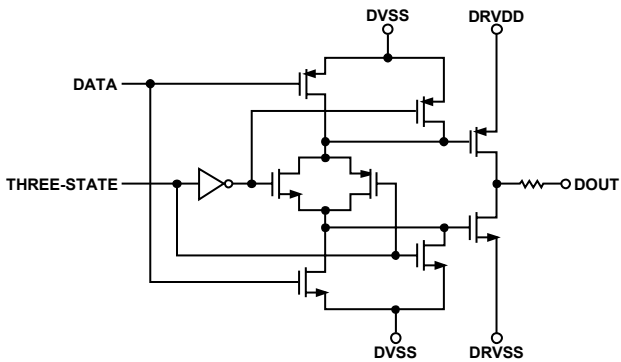


Figure 5. Data Outputs D0\_X to D13\_X

# TYPICAL PERFORMANCE CHARACTERISTICS

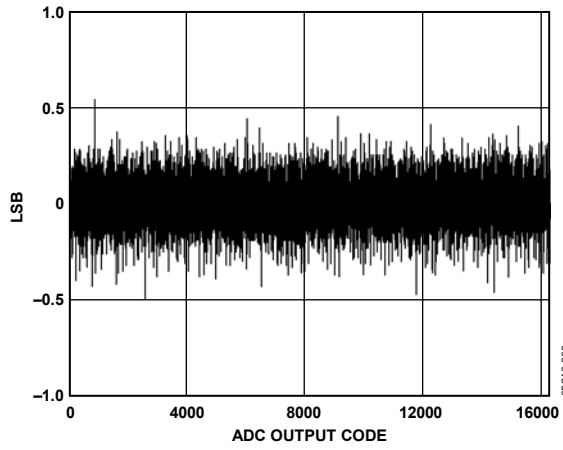


Figure 8. DNL for Channel A and Channel B

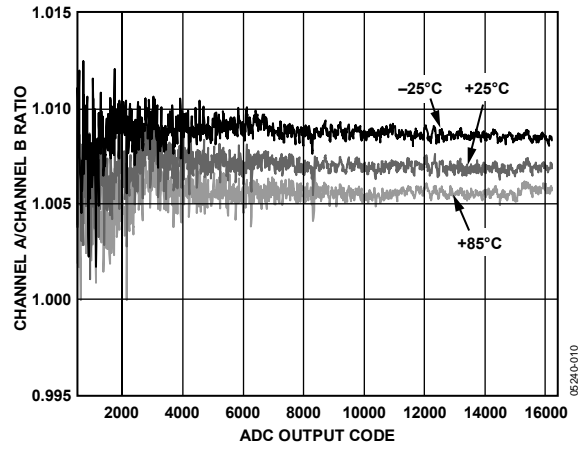


Figure 10. Noncalibrated Channel A/Channel B Ratio

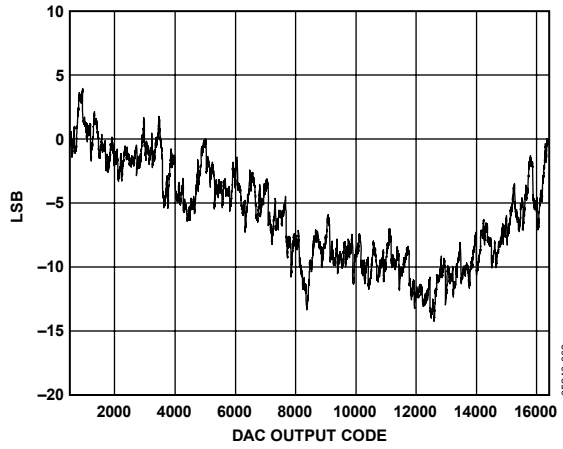


Figure 9. INL Performance for Channel A and Channel B

## SYSTEM OVERVIEW

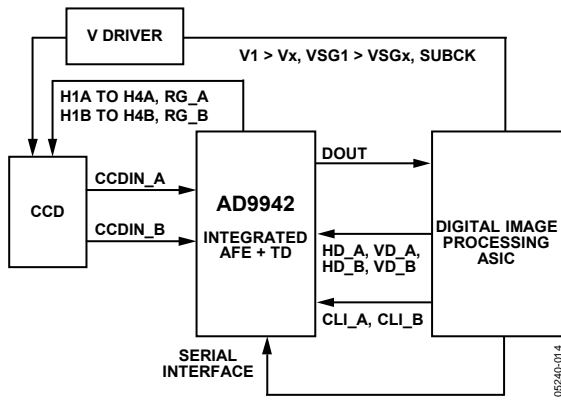


Figure 11. Typical Application

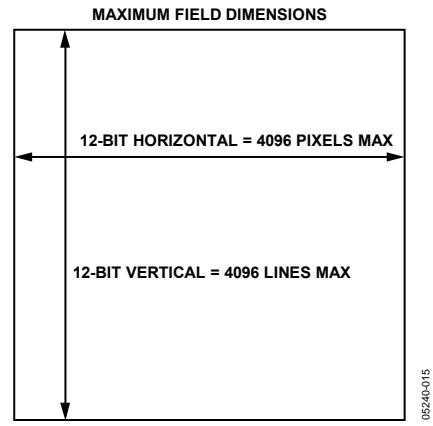


Figure 12. Vertical and Horizontal Counters

Figure 11 shows the typical system application diagram for the AD9942. The CCD output is processed by the AD9942 AFE circuitry, which consists of a CDS, a VGA, a CLPOB, and an ADC. The digitized pixel information is sent to the digital image processor chip, where all postprocessing and compression occurs. To operate the CCD, CCD timing parameters are programmed from the image processor to the AD9942 through the 6-wire serial interface. From the system master clock, CLI, which is provided by the image processor, the device generates the high speed CCD clocks and internal AFE clocks. All AD9942 clocks are synchronized with VD\_X and HD\_X. The CLPOB is programmed and generated internally.

The H drivers for H1A to H4A, H1B to H4B, RG\_A, and RG\_B are included in the AD9942, allowing these clocks to be directly connected to the CCD. An H driver voltage of 3 V is supported in the AD9942.

Figure 12 shows the horizontal and vertical counter dimensions for the device. All internal horizontal clocking is programmed using these dimensions to specify line and pixel locations.

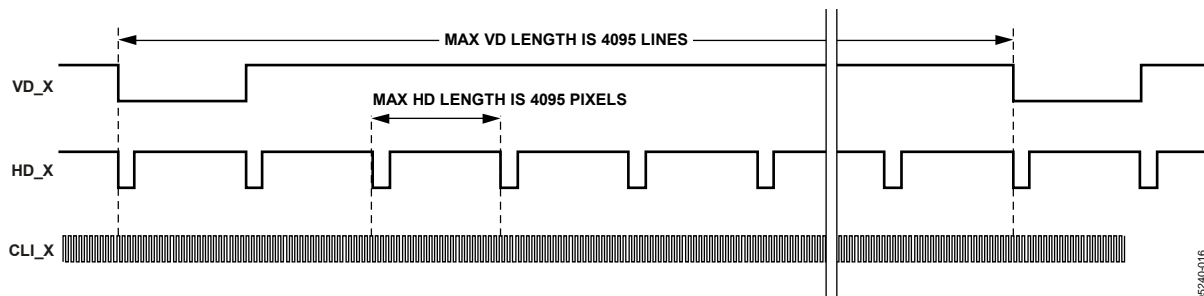


Figure 13. Maximum VD\_X/HD\_X Dimensions

## SERIAL INTERFACE TIMING

All of the AD9942 internal registers are accessed through a 6-wire serial interface. Each register consists of an 8-bit address and a 24-bit data-word. Both the 8-bit address and the 24-bit data-word are written starting with the LSB. To write to each register, a 32-bit operation is required, as shown in Figure 14. Although many registers are less than 24 bits wide, all 24 bits must be written for each register. If the register is only 16 bits wide, then the upper 8 bits can be filled with 0s during the serial write operation. If fewer than 24 bits are written, the register is not updated with new data.

Figure 15 shows a more efficient way to write to the registers by using the AD9942 address auto-increment capability. In this method, the lowest desired address is written first, followed by multiple 24-bit data-words. Each new 24-bit data-word is written automatically to the next highest register address. By eliminating the need to write each 8-bit address, faster register loading is achieved. The address auto-increment function can be used, starting with any register location, to write to as few as two registers or to as many as the entire register space.

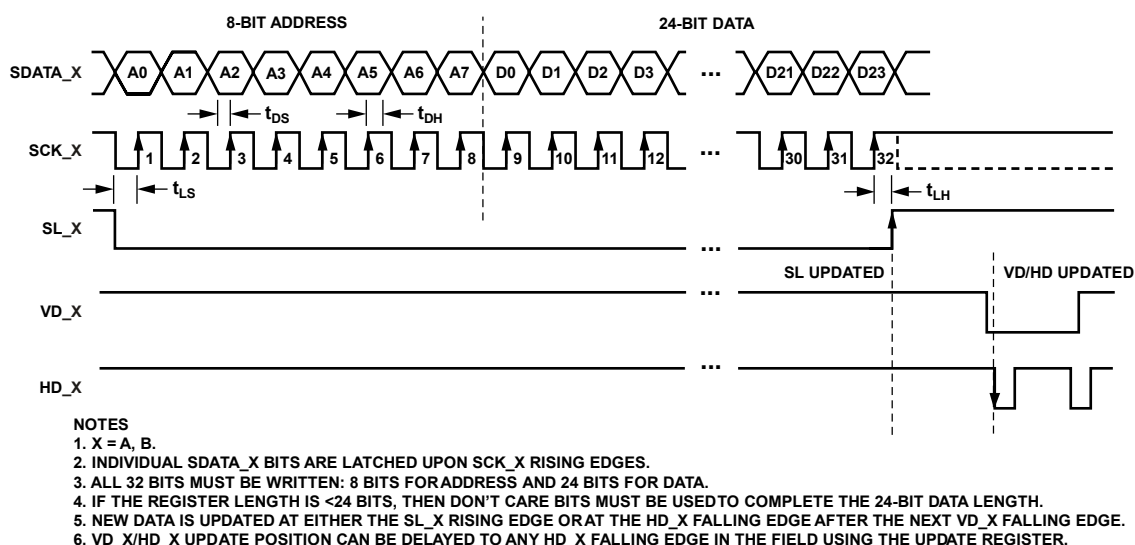


Figure 14. Serial Write Operation

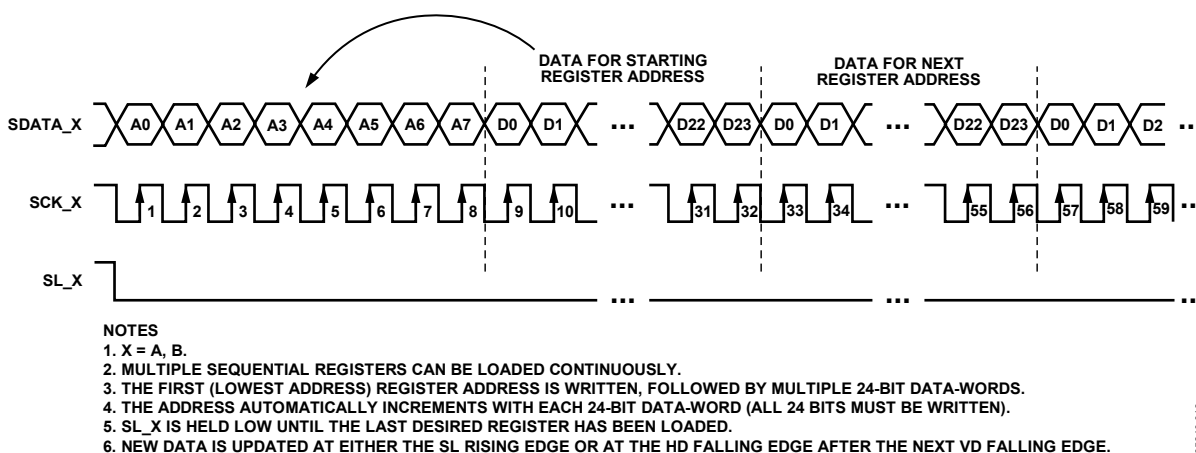


Figure 15. Continuous Serial Write Operation



## COMPLETE REGISTER LISTING

In Table 8 through Table 16, note the following:

- All addresses and default values are expressed in hexadecimal format.
- All registers are VD\_X/HD\_X updated as shown in Figure 14, except for the registers indicated in Table 8, which are SL\_X updated.
- Each channel is programmed independently using the 5-wire serial interface. Both channels can be programmed with the same register values by tying the SL\_A and SL\_B signals together and the SDATA\_A and SDATA\_B signals together.

**Table 8. Updated Registers upon Rising Edge of SL\_X**

Register	Description
OPRMODE	AFE operation modes
CTLMODE	AFE control modes
SW_RESET	Software reset bit
TGCORE_RSTB	Reset bar signal for internal TG core
PREVENTUPDATE	Prevents update of registers
VDHDEDGE	VD/HD active edge
FIELDVAL	Resets internal field pulse
HBLKRETIME	Retimes the HBLK to internal clock
H1CONTROL	H1 polarity control
RGCONTROL	RG signal control polarity
DRVCONTROL	Drive-strength control
SAMPCONTROL	SHP/SHD sample control
DOUPHASE	DOU phase control

**Table 9. CHN\_A and CHN\_B AFE Register Map**

Address	Data Bit Content	Default (Hex)	Name	Description
00	[11:0]	4	OPRMODE	AFE operation modes (see Table 15).
01	[9:0]	0	TESTMODE	Internal test mode. Should always be set = 0.
02	[7:0]	80	CLAMP LEVEL	CLPOB level.
03	[11:0]	4	CTLMODE	AFE control modes (see Table 16).
04	[17:0]	0	TESTMODE	Test operation only. Set = 0.
05	[17:0]	0	TESTMODE	Test operation only. Set = 0.

**Table 10. CHN\_A and CHN\_B Miscellaneous Register Map**

Address	Data Bit Content	Default (Hex)	Name	Description
10	[0]	0	SW_RST	Software reset. 1 = reset all registers to default, then self-clear back to 0.
11	[0]	0	OUT_CONTROL	Output control. 0 = make all dc outputs inactive.
12	[0]	0	TGCORE_RSTB	Timing core reset bar. 0 = reset TG core; 1 = resume operation.
13	[11:0]	0	UPDATE	Serial update. Sets the line (HD) within the field to update serial data.
14	[0]	0	PREVENTUPDATE	Prevents the update of the VD-updated registers. 1 = prevent update.
15	[0]	0	VDHDEDGE	VD/HD active edge. 0 = falling edge triggered; 1 = rising edge triggered.
16	[1:0]	0	FIELDVAL	Field value sync. 0 = next field 0; 1 = next field 1; 2/3 = next field 2.
17	[0]	0	HBLKRETIME	Retime HBLK to internal H1 clock. Preferred setting is 1. Setting to 1 adds one cycle delay to HBLK toggle positions.
18	[1:0]	0	TEST MODE	Internal test mode. Should always be set = 0.
19	[0]	0	TEST MODE	Internal test mode. Should always be set = 0.
1A	[0]	0	TEST MODE	Internal test mode. Should always be set = 0.
E8	[2:0]		TEST MODE	Internal test mode. Should always be set = 0.
	[11:3]	0	VGAGAIN	VGA gain control.

Table 11. CHN\_A and CHN\_B CLPOB Register Map

Address	Data Bit Content	Default (Hex)	Name	Description (the CLPOBSCP0 Always Starts at Line 0)
20	[3:0]	F	CLPOBPOL	Start polarities for CLPOB Sequences 0, 1, 2, and 3.
21	[23:0]	FFFFFF	CLPOBTOG_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
22	[23:0]	FFFFFF	CLPOBTOG_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
23	[23:0]	FFFFFF	CLPOBTOG_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
24	[23:0]	FFFFFF	CLPOBTOG_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
25	[7:0]	00	CLPOBSPTR	CLPOB sequence pointers for Region 0 [1:0], 1 [3:2], 2 [5:4], and 3 [7:6].
26	[11:0]	FFF	CLPOBSCP1	CLPOB sequence—Change Position 1.
27	[11:0]	FFF	CLPOBSCP2	CLPOB sequence—Change Position 2.
28	[11:0]	FFF	CLPOBSCP3	CLPOB sequence—Change Position 3.

Table 12. PBLK Register Map

Address	Data Bit Content	Default (Hex)	Name	Description (the PBLKSCP0 Always Starts at Line 0)
30	[3:0]	F	PBLKPOL	Start polarities for PBLK Sequences 0, 1, 2, and 3.
31	[23:0]	FFFFFF	PBLKTOG_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
32	[23:0]	FFFFFF	PBLKTOG_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
33	[23:0]	FFFFFF	PBLKTOG_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
34	[23:0]	FFFFFF	PBLKTOG_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
35	[7:0]	00	PBLKSPTR	PBLK Sequence Pointers for Region 0 [1:0], 1 [3:2], 2 [5:4], and 3 [7:6].
36	[11:0]	FFF	PBLKSCP1	PBLK sequence—Change Position 1.
37	[11:0]	FFF	PBLKSCP2	PBLK sequence—Change Position 2.
38	[11:0]	FFF	PBLKSCP3	PBLK sequence—Change Position 3.

Table 13. HBLK Register Map

Address	Data Bit Content	Default (Hex)	Name	Description (the HBLKSCP0 Always Starts at Line 0)
40	[0]	0	TESTMODE	Test mode. Always set = 0 if accessed.
41	[0]	0	TESTMODE	Test mode. Always set = 0 if accessed.
42	[0]	1	TESTMODE	Test mode. Always set = 1 if accessed.
43	[3:0]	F	HBLKMASK	HBLK internal masking polarity. 0 = mask H1 low; 1 = mask H1 high.
44	[23:0]	FFFFFF	HBLKTOG12_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
45	[23:0]	FFFFFF	HBLKTOG34_0	Sequence 0. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
46	[23:0]	FFFFFF	HBLKTOG56_0	Sequence 0. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
47	[23:0]	FFFFFF	HBLKTOG12_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
48	[23:0]	FFFFFF	HBLKTOG34_1	Sequence 1. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
49	[23:0]	FFFFFF	HBLKTOG56_1	Sequence 1. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
4A	[23:0]	FFFFFF	HBLKTOG12_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
4B	[23:0]	FFFFFF	HBLKTOG34_2	Sequence 2. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
4C	[23:0]	FFFFFF	HBLKTOG56_2	Sequence 2. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
4D	[23:0]	FFFFFF	HBLKTOG12_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
4E	[23:0]	FFFFFF	HBLKTOG34_3	Sequence 3. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
4F	[23:0]	FFFFFF	HBLKTOG56_3	Sequence 3. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
50	[7:0]	00	HBLKSPTR	HBLK sequence pointers for Region 0 [1:0], 1 [3:2], 2 [5:4], and 3 [7:6].
51	[11:0]	FFF	HBLKSCP1	HBLK sequence—Change Position 1.
52	[11:0]	FFF	HBLKSCP2	HBLK sequence—Change Position 2.
53	[11:0]	FFF	HBLKSCP3	HBLK sequence—Change Position 3.

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**Table 14. CHN\_A and CHN\_B H1 to H4, RG, SHP, SHD Register Map**

Address	Data Bit Content	Default (Hex)	Name	Description
60	[12:0]	01001	H1CONTROL	H1 signal control. Polarity [0] (0 = inversion; 1 = no inversion). H1 positive edge location [6:1]. H1 negative edge location [12:7].
61	[12:0]	00801	RGCONTROL	RG signal control. Polarity [0] (0 = inversion; 1 = no inversion). RG positive-edge location [6:1]. RG negative-edge location [12:7].
62	[14:0]	0	DRVCONTROL	Drive-strength control for H1X [2:0], H2X [5:3], H3X [8:6], H4X [11:9], and RG_X [14:12]. Drive-current values: 0 = off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.2 mA, 5 = 21.5 mA, 6 = 25.8 mA, 7 = 30.1 mA.
63	[11:0]	00024	SAMPCONTROL	SHP/SHD sample control. SHP sampling location [5:0]. SHD sampling location [11:6].
64	[5:0]	0	DOUTPHASE	DOUT phase control.

**Table 15. CHN\_A and CHN\_B AFE Operation Register Detail**

Address	Data Bit Content	Default (Hex)	Name	Description
00	[1:0]	0	PWRDOWN	0 = normal operation; 1 = reference standby; 2/3 = total power-down.
	[2]	1	CLPENABLE	0 = disable CLPOB; 1 = enable CLPOB.
	[3]	0	CLPSPEED	0 = select normal CLPOB settling; 1 = select fast CLPOB settling.
	[4]	0	FASTUPDATE	0 = ignore VGA update; 1 = very fast clamping when VGA is updated.
	[5]	0	PBLK_LVL	DOUT value during PBLK; 0 = blank to zero; 1 = blank to clamp level.
	[7:6]	0	TEST MODE	Internal test mode. Should always be set = 3.
	[8]	0	DCBYP	0 = enable dc restore circuit; 1 = bypass dc restore circuit during PBLK.
	[9]	0	TESTMODE	Test operation only. Set = 0.
	[11:10]	0	TESTMODE	Test operation only. Set = 0.

**Table 16. CHN\_A and CHN\_B AFE Control Register Detail**

Address	Data Bit Content	Default (Hex)	Name	Description
03	[1:0]	0	TESTMODE	Test operation only. Set = 0.
	[2]	1	TESTMODE	Test operation only. Set = 0.
	[3]	0	DOUTDISABLE	0 = data outputs are driven; 1 = data outputs are three-stated.
	[4]	0	DOUTLATCH	0 = latch data outputs with DOUT phase; 1 = output latch transparent.
	[5]	0	GRAYENCODE	0 = binary encode data outputs; 1 = gray encode data outputs.

## CHANNEL A AND CHANNEL B *PRECISION TIMING*

### HIGH SPEED TIMING GENERATION

The AD9942 generates flexible, high speed timing signals using the *Precision Timing* core for both channels. This core is the foundation for generating the timing used for both the CCD and the AFE, the reset gate RG\_X, the horizontal drivers H1X to H4X, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

### TIMING RESOLUTION

The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 16 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Therefore, the edge resolution of the *Precision Timing* core is ( $t_{CLI}/48$ ). For more information on using the CLI input, see the Applications Information section.

### HIGH SPEED CLOCK PROGRAMMABILITY

Figure 17 shows how the high speed clocks, RG\_X, H1X to H4X, SHP, and SHD, are generated. The RG\_X pulse has programmable rising and falling edges and can be inverted using the polarity control. The horizontal clock, H1, has programmable rising and falling edges and polarity control. The H2 clock is always the inverse of the H1 clock. Table 17 summarizes the high speed timing registers and their parameters.

Each edge location setting is six bits wide, but only 48 valid edge locations are available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table 18 shows the correct register values for the corresponding edge locations.

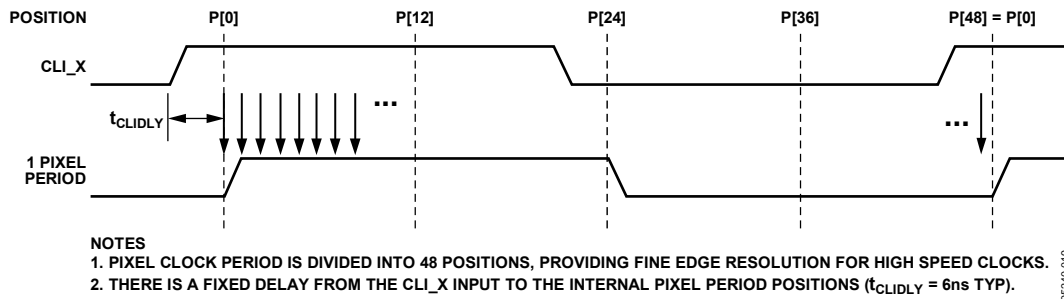


Figure 16. High Speed Clock Resolution from CLI

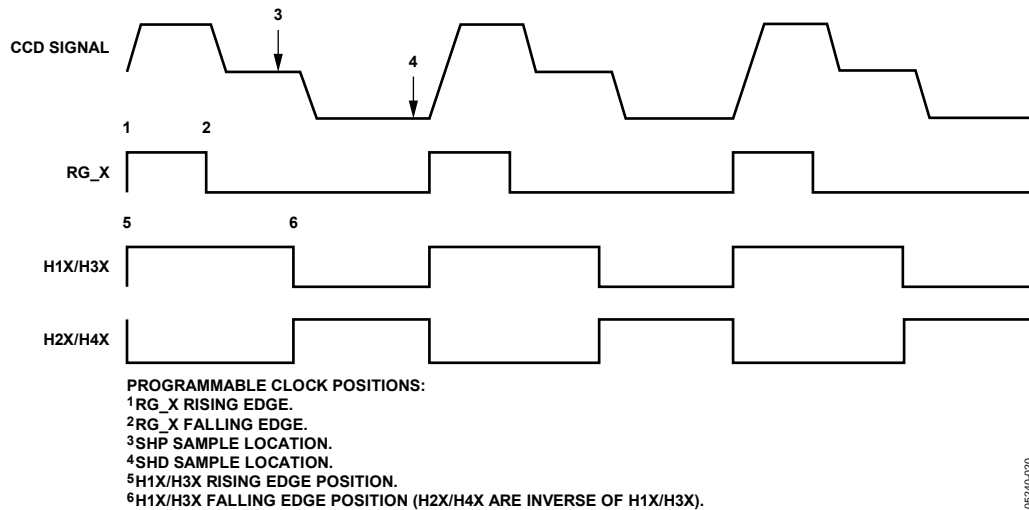


Figure 17. High Speed Clock Programmable Locations

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**Table 17. Channel A and Channel B H1X to H4X CONTROL, RG\_X CONTROL, DRVCONTROL, and SAMPCONTROL Register Parameters**

Parameter	Length (Bit)	Range	Description
Polarity	1	High/low	Polarity control for H1X and RG_X (0 = no inversion; 1 = inversion).
Positive Edge	6	0 to 47 edge locations	Positive-edge location for H1X, H3X, and RG_X.
Negative Edge	6	0 to 47 edge locations	Negative-edge location for H1X and RG_X.
Sample Location	6	0 to 47 sample locations	Sampling location for SHP and SHD.
Drive Control	3	0 to 7 current steps	Drive current for H1X to H4X and RG_X outputs, 0 to 7 steps of 4.1 mA each.
DOUT Phase	6	0 to 47 edge locations	Phase location of data outputs with respect to pixel period.

**Table 18. Channel A and Channel B Precision Timing Edge Locations**

Quadrant	Edge Location (Decimal)	Register Value (Decimal)	Register Value (Binary)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011

### H DRIVER AND RG OUTPUTS

In addition to the programmable timing positions, the AD9942 features on-chip output drivers for the RG\_X and H1X to H4X outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG-driver currents can be adjusted for optimum rise and fall time into a particular load by using the DRVCONTROL register (Address 0x62). The DRVCONTROL register is divided into five 3-bit values, each adjustable in 4.1 mA increments. The minimum setting of 0 is equal to off, or three-state, and the maximum setting of 7 is equal to 30.1 mA.

As shown in Figure 18, the H2X/H4X outputs are inverses of H1X. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results in a H1X/H2X crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

### DIGITAL DATA OUTPUTS

The AD9942 data output phase is programmable using the DOUTPHASE register (Address 0x64). Any edge from 0 to 47 can be programmed, as shown in Figure 19. The pipeline delay for the digital data output is shown in Figure 20.

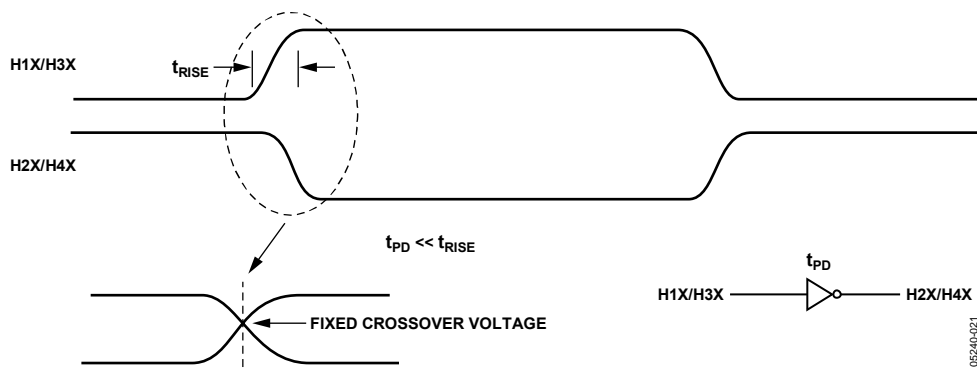
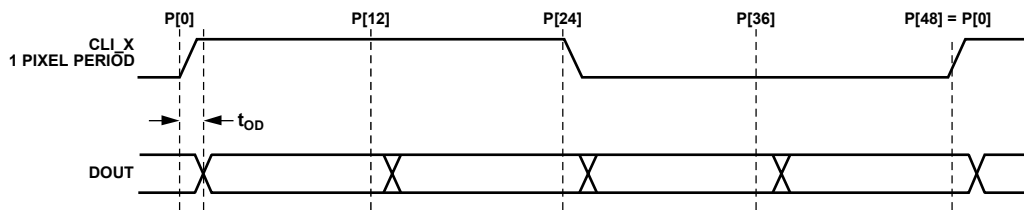
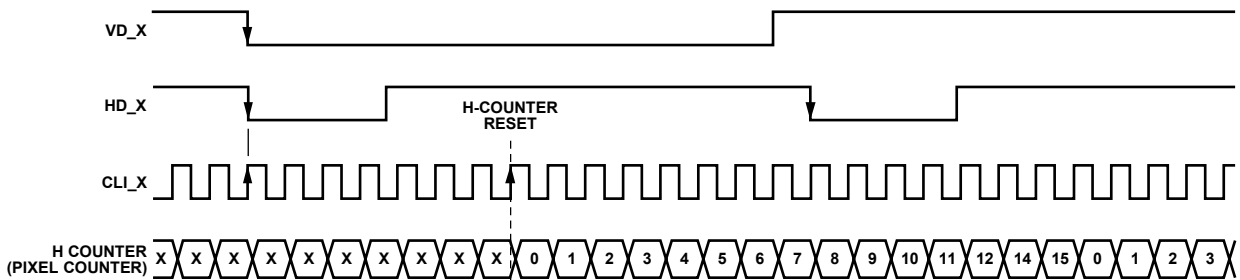


Figure 18. H-Clock Inverse Phase Relationship



- NOTES
1. DIGITAL OUTPUT DATA (DOUT) PHASE IS ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
  2. WITHIN ONE CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO ANY OF THE 48 LOCATIONS.

Figure 19. Digital Output Phase Adjustment



- NOTES
1. INTERNAL H COUNTER IS RESET SEVEN CLI\_X CYCLES AFTER THE HD\_X FALLING EDGE (WHEN USING VDHEDGE = 0).
  2. TYPICAL TIMING RELATIONSHIP: CLI\_X RISING EDGE IS COINCIDENT WITH HD\_X FALLING EDGE.

Figure 20. Pipeline Delay for Channel A and Channel B Digital Data Output

## CHANNEL A AND CHANNEL B HORIZONTAL CLAMPING AND BLANKING

The AD9942 horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual sequences are defined for each signal, which are then organized into multiple regions during image readout. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

### INDIVIDUAL CLPOB AND PBLK SEQUENCES

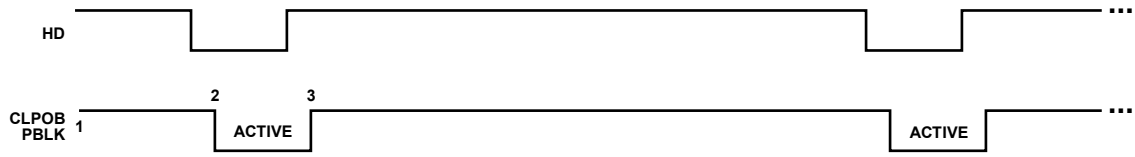
The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 21. These two signals are independently programmed using the parameters shown in Table 19. The start polarity, first toggle position, and second toggle position are fully programmable for each signal. The CLPOB and PBLK signals are active low and should be programmed accordingly. Up to four individual sequences can be created for each signal.

### INDIVIDUAL HBLK SEQUENCES

The HBLK programmable timing, shown in Figure 22, is similar to CLPOB and PBLK. However, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, there is a polarity control, HBLKMASK, which designates the polarity of the horizontal clock signal H1 during the blanking period. Setting HBLKMASK high sets H1 low and H2 high during the blanking, as shown in Figure 23. Up to four individual sequences are available for HBLK.

**Table 19. Channel A and Channel B CLPOB and PBLK Individual Sequence Parameters**

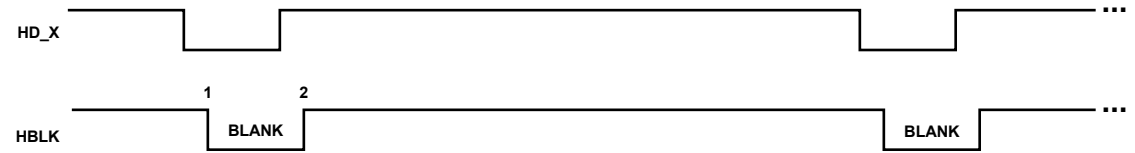
Parameter	Length (Bit)	Range	Description
Polarity	1	High/low	Starting polarity of CLPOB and PBLK pulses for Sequences 0 to 3.
Toggle Position 1	12	0 to 4095 pixel locations	First toggle position within the line for Sequences 0 to 3.
Toggle Position 2	12	0 to 4095 pixel locations	Second toggle position within the line for Sequences 0 to 3.



PROGRAMMABLE SETTINGS:  
 1 START POLARITY (CLAMP AND BLANK REGION ARE ACTIVE LOW).  
 2 FIRST TOGGLE POSITION.  
 3 SECOND TOGGLE POSITION.

05240-024

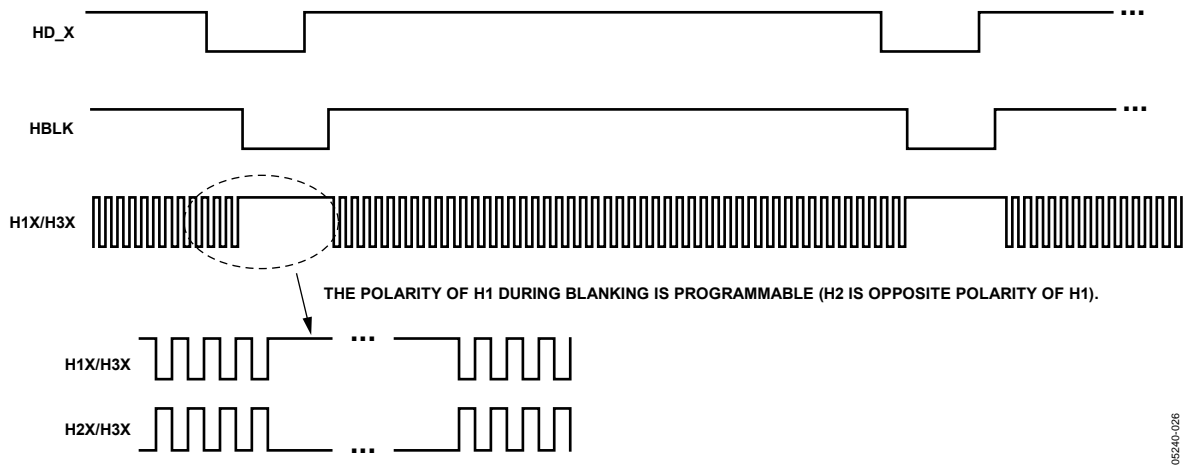
Figure 21. CLPOB and PBLK Pulse Placement



PROGRAMMABLE SETTINGS:  
 1 FIRST TOGGLE POSITION = START OF BLANKING.  
 2 SECOND TOGGLE POSITION = END OF BLANKING.

05240-025

Figure 22. HBLK Pulse Placement



05240-026

Figure 23. HBLK Masking Control



## CHANNEL A AND CHANNEL B SPECIAL HBLK PATTERNS

Six toggle positions are available for HBLK. Typically, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 24. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

### HORIZONTAL SEQUENCE CONTROL

The AD9942 uses sequence change positions (SCPs) and sequence pointers (SPTRs) to organize the individual horizontal sequences. Up to four SCPs are available to divide the readout

into four separate regions, as shown in Figure 25. The SCP0 is always hard-coded to Line 0, and SCP1 to SCP3 are register programmable. During each region bounded by the SCP, the SPTR registers designate which sequence is used by each signal. CLPOB, PBLK, and HBLK each have a separate set of SCPs. For example, CLPOBSCP1 defines Region 0 for CLPOB, and in that region any of the four CLPOB sequences can be selected with the CLPOBSPTR register. The next SCP defines a new region, in which each signal can be assigned to a different individual sequence. The sequence control registers are detailed in Table 21.

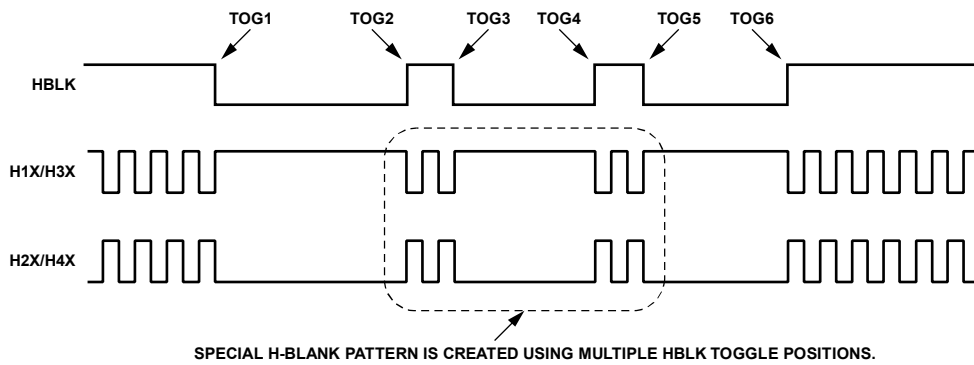


Figure 24. Generating Special HBLK Patterns

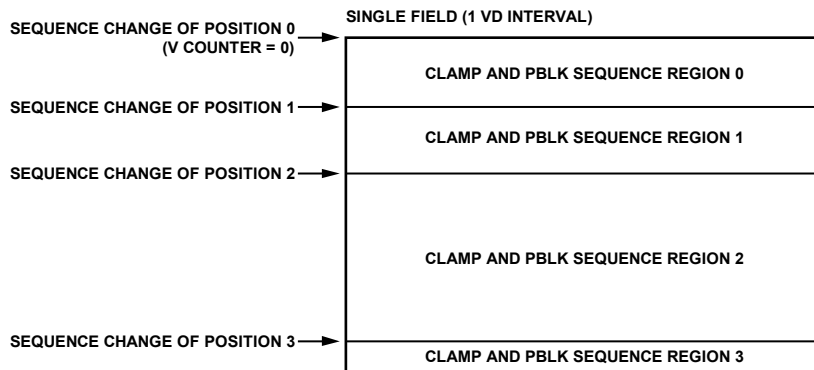


Figure 25. CLPOB and PBLK Sequence Flexibility

Table 20. Channel A and Channel B HBLK Individual Sequence Parameters

Parameter	Length (Bit)	Range	Description
HBLKMASK	1	High/low	Masking polarity for H1 for Sequences 0 to 3 (0 = low; 1 = high).
Toggle Position 1	12	0 to 4095 pixel locations	First toggle position within the line for Sequences 0 to 3.
Toggle Position 2	12	0 to 4095 pixel locations	Second toggle position within the line for Sequences 0 to 3.
Toggle Position 3	12	0 to 4095 pixel locations	Third toggle position within the line for Sequences 0 to 3.
Toggle Position 4	12	0 to 4095 pixel locations	Fourth toggle position within the line for Sequences 0 to 3.
Toggle Position 5	12	0 to 4095 pixel locations	Fifth toggle position within the line for Sequences 0 to 3.
Toggle Position 6	12	0 to 4095 pixel locations	Sixth toggle position within the line for Sequences 0 to 3.

Table 21. Channel A and Channel B Horizontal Sequence Control Registers for CLPOB, PBLK, and HBLK

Register	Length (Bit)	Range	Description
SCP	12	0 to 4095 line numbers	CLPOB/PBLK/HBLK SCP to define Horizontal Regions 0 to 3.
SPTR	2	0 to 3 sequence numbers	Sequence pointer for Horizontal Regions 0 to 3.

Table 22. Channel A and Channel B External HBLK Register Parameters

Register	Length (Bit)	Range	Description
HBLKDIR	1	High/low	Specifies HBLK internally generated or externally supplied. 0 = internal; 1 = external.
HBLKPOL	1	High/low	External HBLK active polarity. 0 = active low; 1 = active high.
HBLKEXTMASK	1	High/low	External HBLK masking polarity. 0 = mask H1 low; 1 = mask H1 high.

## H-COUNTER SYNCHRONIZATION

The H-counter reset occurs seven CLI cycles after the HD falling edge.

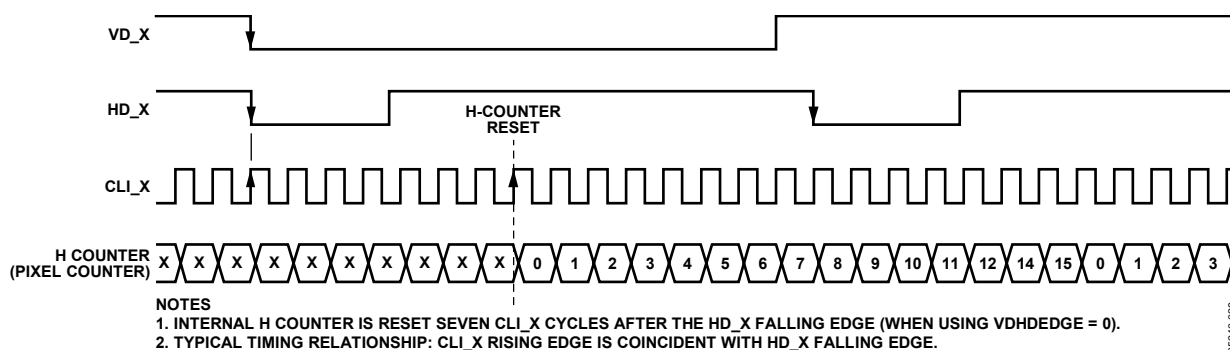


Figure 26. H-Counter Synchronization

## CHANNEL A AND CHANNEL B POWER-UP PROCEDURE

When the AD9942 is powered up, the following sequence is recommended for Channel A and Channel B (see Figure 27 for each step).

1. Turn on the power supplies for the AD9942.
2. Apply the master clock input, CLI\_X, VD\_X, and HD\_X.
3. Although the AD9942 contains an on-chip power-on reset, a software reset of the internal registers is recommended. Write a 1 to the SW\_RST register (Address 0x10), which resets all the internal registers to their default values. This bit is self-clearing and is automatically reset to 0.
4. Reset the *Precision Timing* core by writing a 0 to the TGCORE\_RSTB register (Address 0x12), then write a 1 to the TGCORE\_RSTB register. This starts the internal timing core operation.
5. Write a 1 to the PREVENTUPDATE register (Address 0x14). This prevents an update of the serial register data.
6. Write to the desired registers to configure high speed timing and horizontal timing.
7. Write a 3 to the [7:6] TESTMODE register (Address 0x00). See Table 15.
8. Write a 1 to the OUT\_CONTROL register (Address 0x11). This allows the outputs to become active after the next VD\_X/HD\_X rising edge.
9. Write a 0 to the PREVENTUPDATE register (Address 0x14). This allows the serial information to be updated at the next VD\_X/HD\_X falling edge. The next VD\_X/HD\_X falling edge allows register updates, including updates of OUT\_CONTROL, to occur which enables all clock outputs.

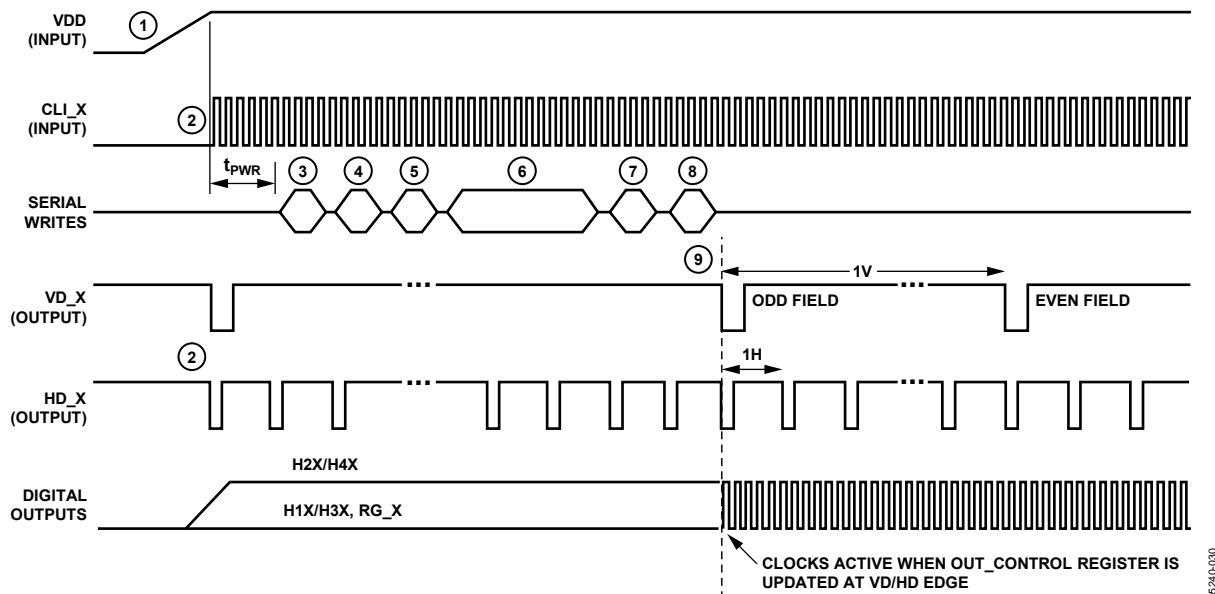


Figure 27. Recommended Power-Up Sequence

06240-030

## CHANNEL A AND CHANNEL B ANALOG FRONT END OPERATION

The AD9942 signal processing chain is shown in Figure 28. Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

### DC RESTORE

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external  $0.1 \mu\text{F}$  series coupling capacitor. This restores the dc level of the CCDIN\_X signal to approximately 1.5 V to be compatible with the 3 V supply voltage of the AD9942.

### CORRELATED DOUBLE SAMPLER

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 17 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and the CCD signal level, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SAMPCONTROL register located at Address 0x63. Placement of these two clock signals is critical for achieving the best performance from the CCD.

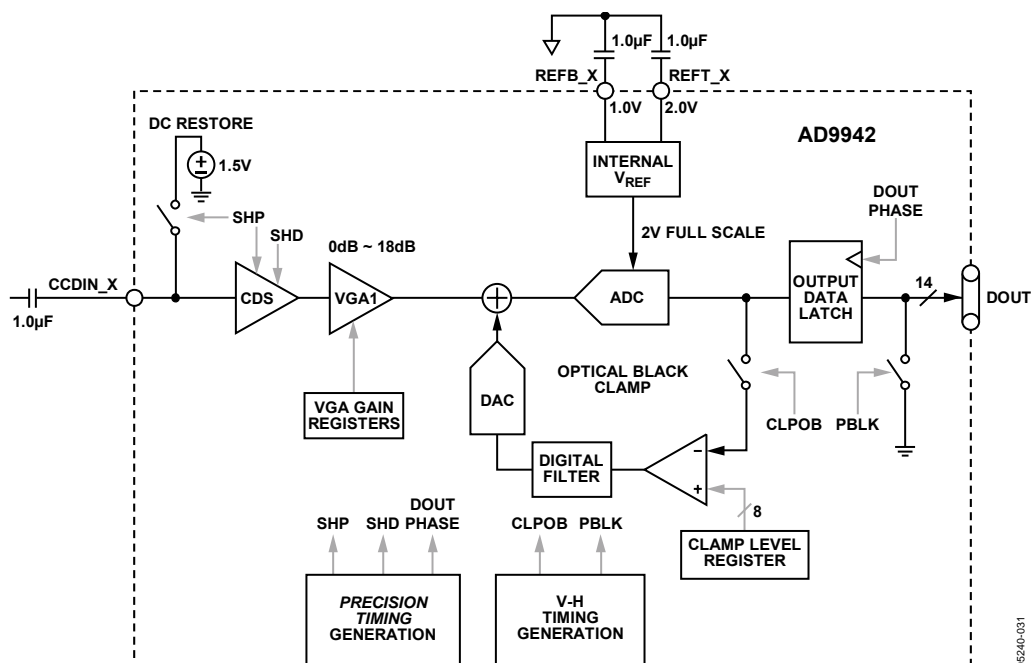


Figure 28. Channel A and Channel B Analog Front End Functional Block Diagram

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## CHANNEL A AND CHANNEL B VARIABLE GAIN AMPLIFIER

The VGA stage provides a gain range of 0 dB to 18 dB, programmable with 9-bit resolution through the serial digital interface. A minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain can be calculated for any gain register value by using the equation

$$\text{Gain (dB)} = (0.035 \times \text{VGAGAIN Code})$$

where the code range is 0 to 511.

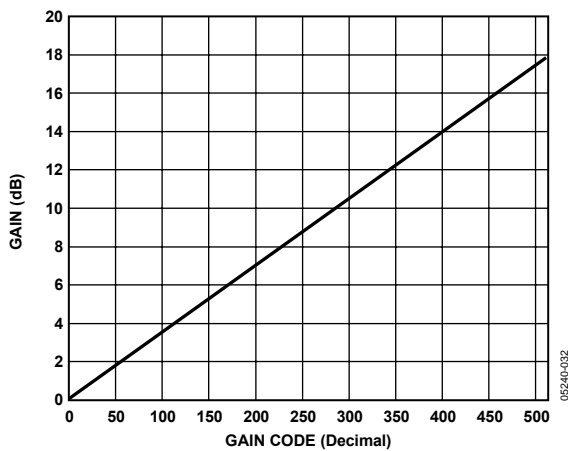


Figure 29. VGA Gain Curve

## CHANNEL A AND CHANNEL B ADC

The AD9942 uses a high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. See Figure 8 and Figure 9 for typical linearity and noise performance plots for the AD9942.

## CHANNEL A AND CHANNEL B CLPOB

The CLPOB loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD black level. During the optical black (OB), or shielded, pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the CLAMP LEVEL register. The value can be programmed between 0 LSB and 255 LSB in 256 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a digital-to-analog converter. Typically, the CLPOB loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during postprocessing, the AD9942 CLPOB can be disabled using Bit D2 in the OPRMODE register. The CLAMP LEVEL register can be used to provide programmable offset adjustment even when the loop is disabled.

The CLPOB pulse should be placed during the CCD's OB pixel region. It is recommended that the CLPOB pulse duration be at least 20 pixels wide to minimize clamp noise. Shorter pulse widths can be used, but clamp noise might increase and the ability to track low frequency variations in the black level is reduced. See the Channel A and Channel B Horizontal Clamping and Blanking section and the Applications Information section for timing examples.

## CHANNEL A AND CHANNEL B DIGITAL DATA OUTPUTS

The AD9942 digital output data is latched using the DOUTPHASE register value, as shown in Figure 28. (Output data timing is shown in Figure 19 and Figure 20.) It is also possible to leave the output latches transparent, so that the data outputs are valid immediately from the ADC. Programming the AFE Control Register Bit D4 to 1 sets the output latches transparent. The data outputs can also be disabled (three-stated) by setting the AFE Control Register Bit D3 to 1.

The data output coding is typically straight binary, but the coding can be changed to gray coding by setting the AFE Control Register Bit D5 to 1.

## APPLICATIONS INFORMATION

### CIRCUIT CONFIGURATION

The AD9942 recommended circuit configuration is shown in Figure 30. Achieving good image quality from the AD9942 requires careful attention to the printed circuit board (PCB) layout. All signals should be routed to maintain low noise performance. The CCD\_A and CCD\_B output signals should be directly routed to Pins A1 and A7, respectively, through a 0.1  $\mu\text{F}$  capacitor. The master clock, CLI\_X, should be carefully routed to Pins A3 and A9 to minimize interference with the CCDIN\_X, REFT\_X, and REFB\_X signals.

The digital outputs and clock inputs should be connected to the digital ASIC away from the analog and CCD clock signals. Placing series resistors close to the digital output pins may help to reduce digital code transition noise. If the digital outputs must drive a load larger than 20 pF, buffering is recommended to minimize additional noise. If the digital ASIC can accept gray code, the AD9942 outputs can be selected to output data in gray code format using the Control Register Bit D5. Gray coding helps reduce potential digital transition noise compared with binary coding.

The H1X to H4X and RG\_X traces should have low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demand on H1X to H4X from the capacitive load of the CCD. If possible, physically locate the AD9942 closer to the CCD to reduce the inductance on these lines. As always, the routing path should be as direct as possible from the AD9942 to the CCD.

The CLI\_X and CCDIN\_X PCB traces should be carefully matched in length and impedance to achieve optimal channel-to-channel matching performance.

### GROUNDING/DECOUPLING RECOMMENDATIONS

As Figure 30 shows, a single ground plane is recommended for the AD9942. This ground plane should be as continuous as possible, particularly around the P-, AI-, and A-type pins, to ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All high frequency decoupling capacitors should be located as close as possible to the package pins.

All the supply pins must be decoupled to ground with good quality, high frequency chip capacitors. There should also be a 4.7  $\mu\text{F}$  or larger bypass capacitor for each main supply—that is, the AVDD\_X, RGVDD\_X, HVDD\_X, and DRVDD\_X—although this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD\_X and HVDD\_X, which can be done as long as the individual supply pins are separately bypassed. A separate 3 V supply can be used for DRVDD\_X, but this supply pin should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS\_X is not recommended.

The reference bypass pins (REFT\_X, REFB\_X) should be decoupled to ground as close as possible to their respective pins. The analog input capacitor (CCDIN\_X) should also be located close to the pin.

The GND connections should be tied to the lowest impedance ground plane on the PCB. Performance does not degrade if several of these GND connections are left unconnected for routing purposes.

# AD9942

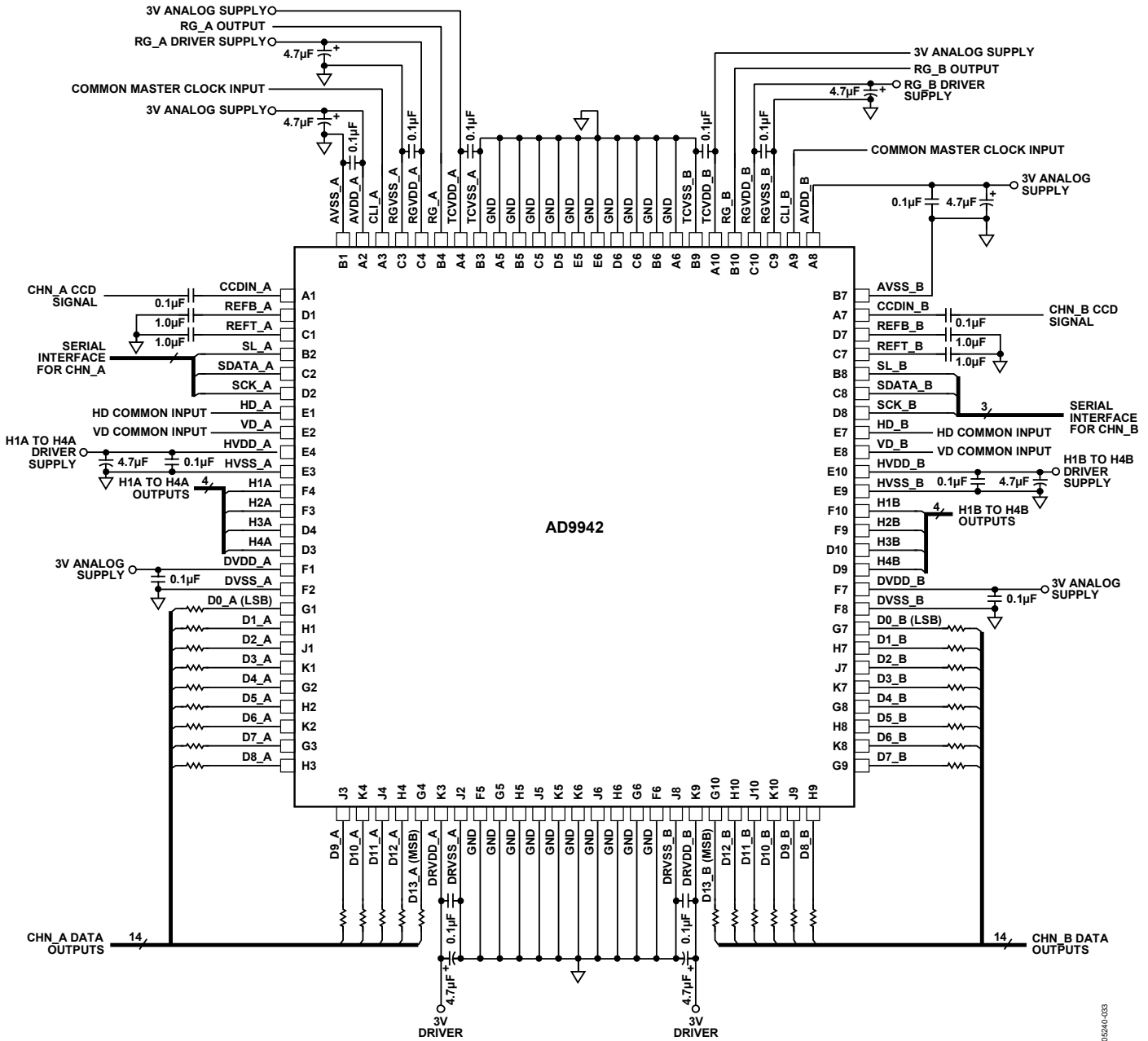


Figure 30. Recommended Circuit Configuration

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**DRIVING THE CLI INPUT**

The AD9942 CLI can be used in two configurations, depending on the application. Figure 31 shows a typical dc-coupled input from the master clock source. When the dc-coupled technique is used, the master clock signal should be at standard 3 V CMOS logic levels. As shown in Figure 32, a 1000 pF ac coupling capacitor can be used between the clock source and the CLI input. In this configuration, the CLI input performs a self-bias to the proper dc voltage level of approximately 1.4 V. When the ac-coupled technique is used, the master clock signal can be as low as  $\pm 500$  mV in amplitude.

**HORIZONTAL TIMING SEQUENCE EXAMPLE**

Figure 33 shows an example CCD configuration. The horizontal register contains 28 dummy pixels, which occur on each line clocked from the CCD. In the vertical direction, there are

10 OB lines at the front of the readout and 2 at the back of the readout. The horizontal direction has 4 OB pixels in the front and 48 in the back.

To configure the AD9942 horizontal signals for this CCD, three sequences can be used. Figure 34 shows the first sequence to be used during vertical blanking. During this time, there are no valid OB pixels from the sensor, so the CLPOB signal is not used. PBLK can be enabled during this time because no valid data is available.

Figure 35 shows the recommended sequence for the vertical OB interval. The clamp signals are used across the whole lines to stabilize the clamp loop of the AD9942.

Figure 36 shows the recommended sequence for the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signal.

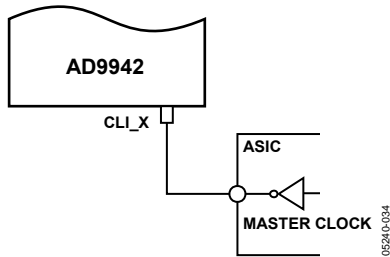


Figure 31. CLI Connection, DC-Coupled

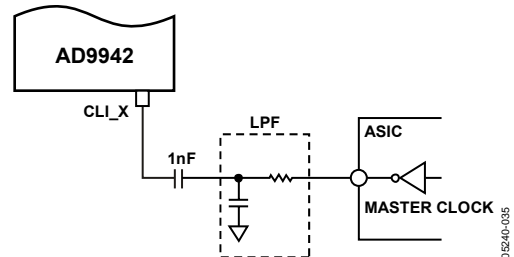


Figure 32. CLI Connection, AC-Coupled

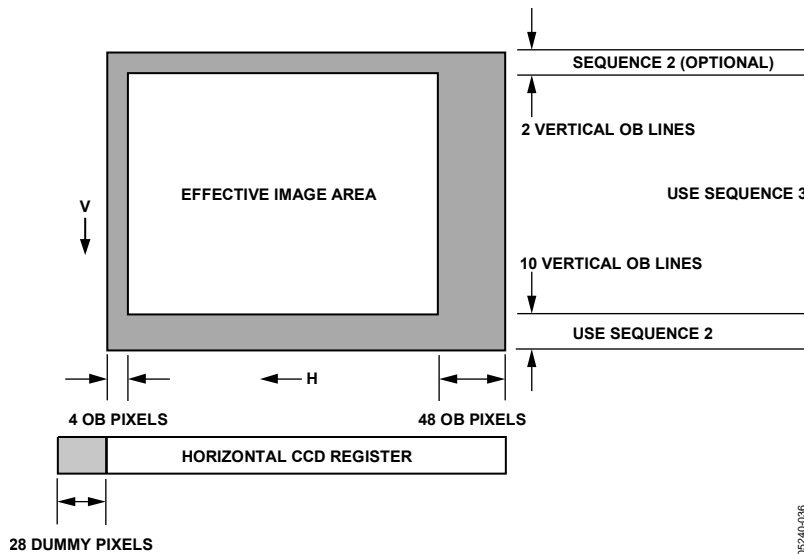


Figure 33. Example CCD Configuration



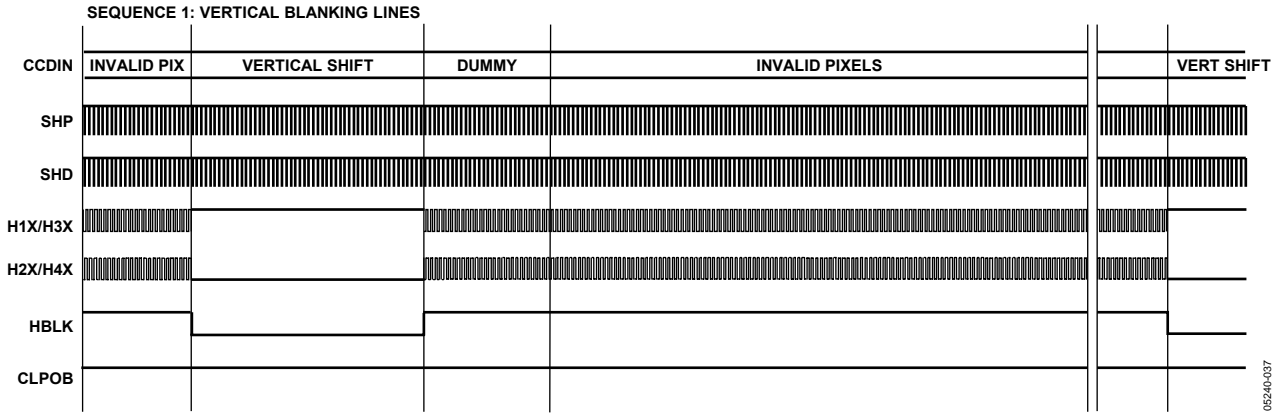


Figure 34. Horizontal Sequence During Vertical Blanking

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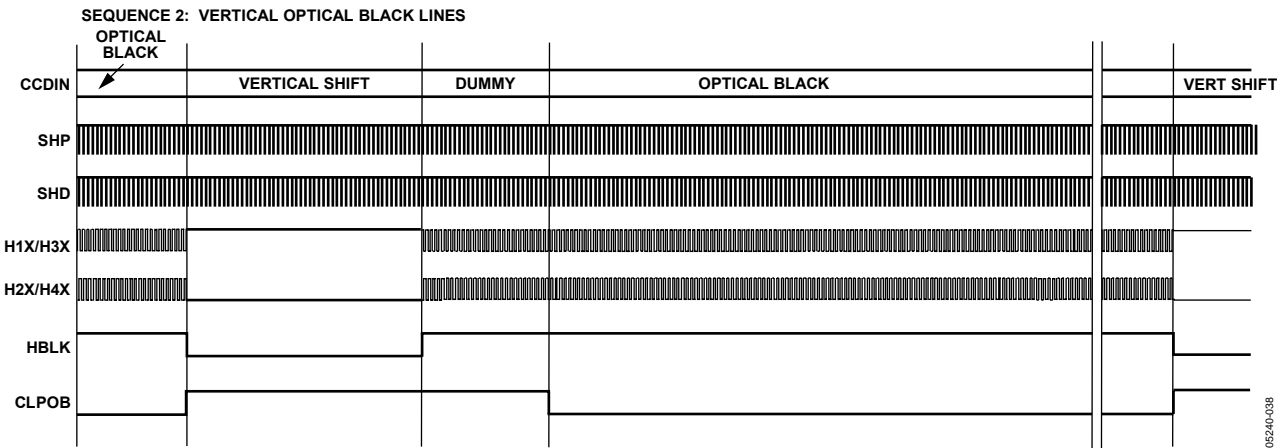


Figure 35. Horizontal Sequences During Vertical OB Pixels

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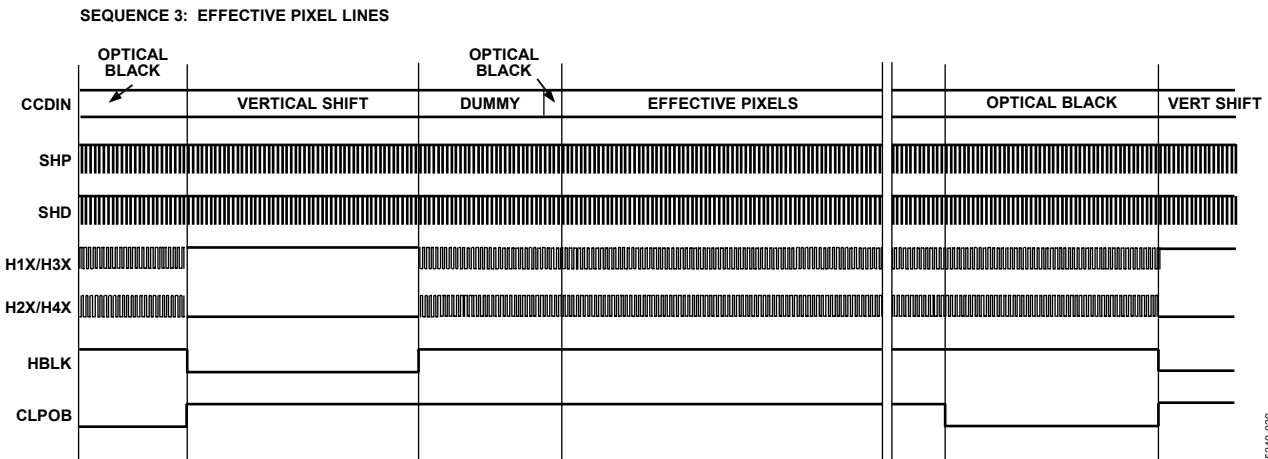


Figure 36. Horizontal Sequences During Effective Pixels

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**AD9942**

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