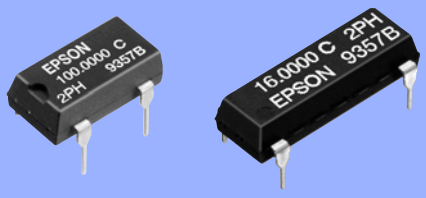
CRYSTAL OSCILLATOR
PROGRAMMABLE

SG-8002DC / DB series

- Frequency range : 1 MHz to 125 MHz
- Supply voltage : 3.3 V / 5.0 V
- Function : Output enable(OE) or Standby($\overline{ST}$)
  Pin compatible with full size and half size.
- Short mass production lead time by PLL technology.
- SG-Writer available to purchase.
  Please contact EPSON TOYOCOM or local sales representative.

RoHS Compliant

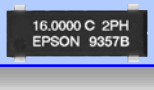
Product Number (please contact us)
SG-8002DC: Q3204DCx1xxxx00
SG-8002DB: Q3203DBx1xxxx00



Actual size

SG-8002DC

SG-8002DB



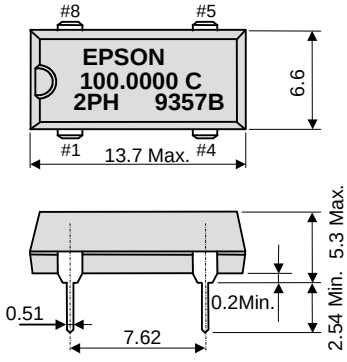
Specifications (characteristics)

Item		Symbol	Specifications *2 PT / ST	PH / SH	PC / SC	Remarks
Output frequency range		f_0	1 MHz to 125 MHz		—	V_{CC}=4.5 V to 5.5 V
			—		1 MHz to 125 MHz	V_{CC}=3.0 V to 3.6 V
			—		1 MHz to 66.7 MHz	V_{CC}=2.7 V to 3.6 V
Supply voltage		V_{CC}	4.5 V to 5.5 V		2.7 V to 3.6 V	
Temperature range	Storage temperature	T_stg	-55 °C to +125 °C			Store as bare product after unpacking
	Operating temperature	T_use	-20 °C to +70 °C (-40 °C to +85 °C)		-40 °C to +85 °C	Refer to “Outline specifications” (Frequency range)
Frequency tolerance		f_tol	B: ±50 × 10^{-6} ,C: ±100 × 10^{-6}			-20 °C to +70 °C
			M: ±100 × 10^{-6}			-40 °C to +85 °C *3
Current consumption		Icc	45 mA Max.		28 mA Max.	No load condition, Max. frequency
Disable current		I_dis	30 mA Max.		16 mA Max.	OE=GND(PT,PH,PC)
Stand-by current		I_std	50 µA Max.			$\overline{ST}$ =GND(ST,SH,SC)
Symmetry *1		SYM	—	40 % to 60 %		CMOS load:50%Vcc level, Max. load condition
			40 % to 60 %	—		TTL load: 1.4 V level, Max. load condition
High output voltage		V_{OH}	V_{CC}-0.4 V Min.			I_{OH}=-16 mA(PT,ST,PH,SH),-8 mA(PC,SC)
Low output voltage		V_{OL}	0.4 V Max.			I_{OL}=16 mA(PT,ST,PH,SH), 8 mA(PC,SC)
Output load condition (TTL) *1		L_TTL	5 TTL Max.	—		Max. frequency and Max. supply voltage
Output load condition (CMOS) *1		L_CMOS	15 pF Max.	25 pF Max.	15 pF Max.	
Output enable / disable input voltage		V_{IH}	2.0 V Min.		70 % V_{CC} Min.	$\overline{ST}$ terminal or OE terminal
		V_{IL}	0.8 V Max.		20 % V_{CC} Max.	
Rise time / Fall time *1		t_r / t_f	—	3 ns Max.		CMOS load: 20 % V_{CC} to 80 % V_{CC} level
			4 ns Max.	—		TTL load: 0.4 V to 2.4 V level
Start-up time		t_str	10 ms Max.			Time at minimum supply voltage to be 0 s
Frequency aging		f_aging	±5 × 10^{-6} / year Max.			+25 °C, V_{CC}=5.0 V/ 3.3 V (PC/SC) First year

*1 Operating temperature (-40 °C to +85 °C), the available frequency, symmetry and output load conditions, please refer to “Outline specifications” page.
*2 PLL-PLL connection & Jitter specification, please refer to “Jitter specifications and characteristics chart” page.
*3 PT / ST and PH / SH for “M” tolerance will be available up to 55 MHz.
Checking possible by the Frequency Checking Program.

External dimensions (Unit:mm)

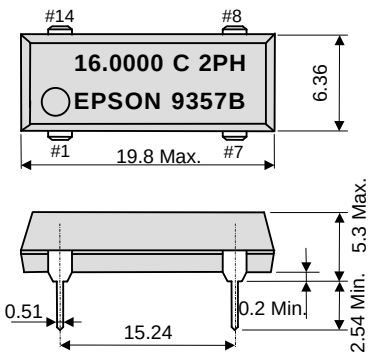
●SG-8002DC



Pin map

Pin	Connection
1	OE or $\overline{ST}$
4	GND
5	OUT
8	V_{CC}

●SG-8002DB



Pin map

Pin	Connection
1	OE or $\overline{ST}$
7	GND
8	OUT
14	V_{CC}

Note.
OE Pin (PT, PH, PC)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

$\overline{ST}$ pin (ST, SH, SC)
$\overline{ST}$ pin = "H" or "open" : Specified frequency output.
$\overline{ST}$ pin = "L" : Output is low level (weak pull - down), oscillation stops.

To maintain stable operation, provide by-pass capacitor with more than 0.1 µF at a location as near as possible to the power source terminal of the crystal products (between V_{CC} - GND).