100MHz Isolated DAC SPI Serial Interface

FEATURES

- **Isolated Interface: 6000V_{RMS} for 1 Minute**
- **UL-CSA-IEC Certification Pending**
- **100MHz SPI-Compatible I/O**
- **Configurable SPI Word-Length: 8 to 32 Bits**
- **Supports Two Isolated Chip Selects**
- **Falling Edge Sensitive Low Jitter $\overline{LOAD}$**
- Three Isolated Control or Multiplexer Signals
- 1.71V to 5.5V I/O Voltages
- 3V to 5.5V Supply Voltages
- High Common Mode Transient Immunity
- 15mm × 6.25mm BGA Package

APPLICATIONS

- Remote Interface Control
- Industrial Process Control and Automation
- Test and Measurement Equipment
- Breaking Ground Loops

DESCRIPTION

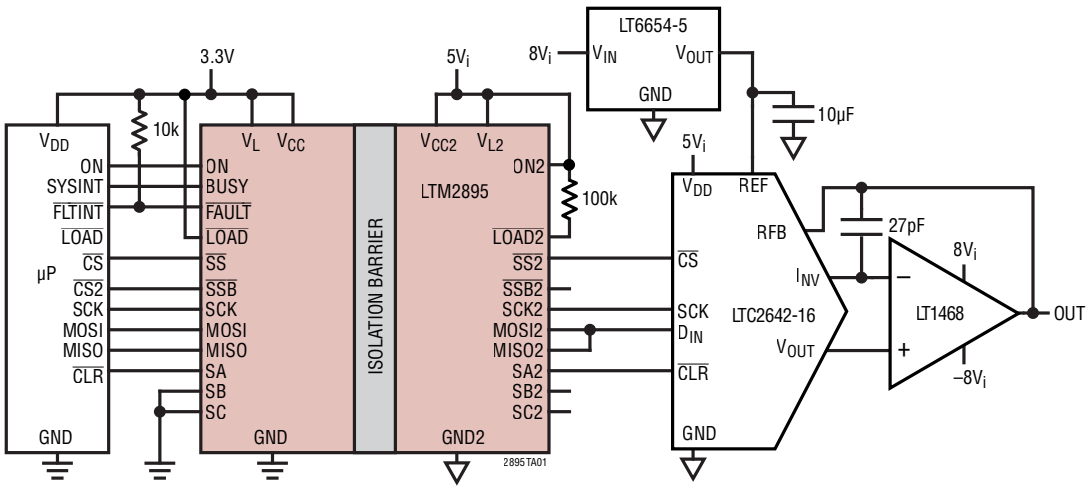
The LTM®2895 is a high speed isolated µModule® (micromodule) SPI interface with DAC control signals designed to isolate LTC's family of general purpose DACs and to isolate general purpose SPI interfaces. The LTM2895 works with DACs and general purpose devices that have a mode (0, 0) SPI interface.

The interface enables fast data throughput, which makes the LTM2895 ideally suited for a wide variety of applications. The high speed SPI-compatible serial port supports 1.71V to 5.5V logic supplies. The LTM2895 is targeted at generic SPI and digital-to-analog converter applications.

The isolation barrier tolerates large voltage ground variations between the logic interface and the isolated side of the LTM2895. Uninterrupted communication is maintained during voltage transients greater than 50kV/µs.

TYPICAL APPLICATION

LTC2642-16 DAC Isolation



CONFIGURATION REGISTERS: WRITE 0x30H AND 0x83H SETS SCK2 TO 33MHz AND WORDLENGTH TO 16-BIT
V_i = ISOLATED VOLTAGE SUPPLY

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages

V_L – GND ..... –0.3V to 6V

V_{CC} – GND ..... –0.3V to 6V

Isolated Supply Voltages

V_{L2} – GND2 ..... –0.3V to 6V

V_{CC2} – GND2 ..... –0.3V to 6V

Logic Signals

ON, $\overline{LOAD}$, BUSY, SA, SB, SC, $\overline{SS}$, $\overline{SSB}$

SCK, MOSI, MISO ..... GND – 0.3V to V_L + 0.3V

$\overline{FAULT}$ ..... GND – 0.3V to 6.3V

Isolated Signals

$\overline{SS2}$, $\overline{SSB2}$, MISO2, ON2, $\overline{LOAD2}$, SCK2

SA2, SB2, SC2, MOSI2 ..... GND2 – 0.3V to V_{L2} + 0.3V

Operating Temperature Range (Note 10)

LTM2895C ..... 0°C to 70°C

LTM2895I ..... –40°C to 85°C

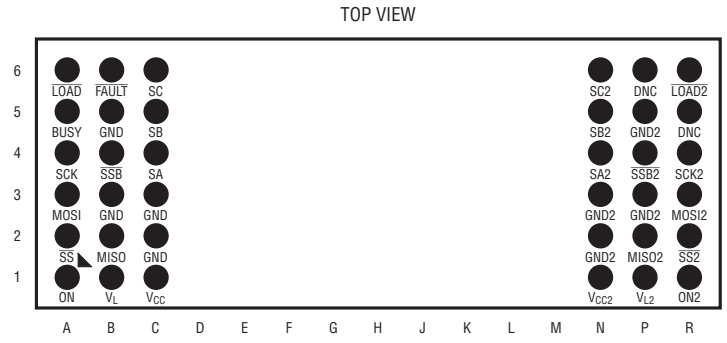
LTM2895H ..... –40°C to 125°C

Storage Temperature Range ..... –55°C to 125°C

Maximum Internal Operating Temperature ..... 125°C

Peak Body Reflow Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
36-LEAD (15mm × 6.25mm × 2.06mm)

T_{JMAX} = 125°C, θ_{JA} = 36°C/W, θ_{JCTOP} = 27.5°C/W, $\theta_{JCBOTTOM}$ = 17.5°C/W
θ_{JB} = 19.1°C/W, WEIGHT = 0.36g

ORDER INFORMATION

http://www.linear.com/product/LTM2895#orderinfo

PART NUMBER	PACKAGE TYPE	BALL FINISH	PART MARKING*		MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE		
LTM2895CY#PBF	BGA	SAC305 (RoHS)	LTM2895Y	e1	3	0°C to 70°C
LTM2895IY#PBF						–40°C to 85°C
LTM2895HY#PBF						–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{CC}	Operating Supply Range		●	3.0		5.5	V
I_{CC}	Operating Supply Current	Idle	●		9	12	mA
	Operating Supply Current, Max DAC Conversion Rate	32-Bit Write/1µs, 20pF Loads, SCK = 50MHz	●		12	15	mA
V_{CC2}	Isolated Operating Supply Range		●	3.0		5.5	V
I_{CC2}	Isolated Operating Supply Current	Idle	●		9	12	mA
	Isolated Operating Supply Current, Max DAC Conversion Rate	32-Bit Write/1µs, 20pF Loads, SCK = 50MHz	●		12	15	mA
V_L	Logic Interface Supply Range		●	1.71	3.3	5.5	V
I_L	Logic Interface Supply Current	Inputs and Outputs Static at GND or V_L	●			±200	µA
	Logic Interface Supply Current, Max Conversion Rate	32-Bit Write/1µs, 20pF Loads, SCK = 50MHz	●		2	5	mA
V_{L2}	Isolated Interface Supply Range		●	1.71	3.3	5.5	V
I_{L2}	Isolated Interface Supply Current	Inputs and Outputs Static at GND2 or V_{L2}	●			±200	µA
	Isolated Interface Supply Current, Max Conversion Rate	32-Bit Write/1µs, 20pF Loads, SCK = 50MHz	●		2	5	mA
Digital Inputs and Digital Outputs (Logic Side)							
V_{IH}	High Level Input Voltage	1.71V ≤ V_L ≤ 5.5V	●	0.8 • V_L			V
V_{IL}	Low Level Input Voltage	1.71V ≤ V_L ≤ 5.5V	●			0.2 • V_L	V
	Digital Input Current (MOSI, SCK, $\overline{LOAD}$)	V_{IN} = 0V to V_L, $\overline{SS}$ = V_L	●			±1	µA
	Digital Input Current ($\overline{SS}$, $\overline{SSB}$, SA, SB, SC, ON)	V_{IN} = 0V to V_L	●			±60	µA
	Digital Input Capacitance	(Note 7)			5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA, 1.71V ≤ V_L ≤ 5.5V	●	V_L – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA, 1.71V ≤ V_L ≤ 5.5V	●			0.2	V
	High-Z Output Leakage Current MISO	$\overline{SS}$ = V_L	●			±1	µA
	Output Source Current (Short-Circuit) MISO, BUSY	V_{OUT} = 0V (Note 7)			–80		mA
	Output Sink Current (Short-Circuit) MISO, BUSY, $\overline{FAULT}$	V_{OUT} = V_L (Note 7)			80		mA
Digital Inputs and Digital Outputs (Isolated Side)							
V_{IH}	High Level Input Voltage	1.71V ≤ V_{L2} ≤ 5.5V	●	0.8 • V_{L2}			V
V_{IL}	Low Level Input Voltage	1.71V ≤ V_{L2} ≤ 5.5V	●			0.2 • V_{L2}	V
	Digital Input Current (ON2)	V_{IN} = 0V to V_{L2}	●			±60	µA
	Digital Input Current (MISO2)	V_{IN} = 0V to V_{L2}	●			±10	µA
	Digital Input Capacitance	(Note 7)			5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA, 1.71V ≤ V_{L2} ≤ 5.5V	●	V_L – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA, 1.71V ≤ V_{L2} ≤ 5.5V	●			0.2	V
	Output Source Current (Short-Circuit)	V_{OUT} = 0V (Note 7)			–80		mA
	Output Sink Current (Short-Circuit)	V_{OUT} = V_{L2} (Note 7)			80		mA

ESD PERFORMANCE (Note 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Isolation Barrier Logic Side I/O Pins Isolated Side I/O Pins	From GND, V_L, or V_{CC} to GND2, V_{L2}, or V_{CC2} GND, V_L, V_{CC} GND2, V_{L2}, V_{CC2}			±15 ±4 ±4		kV kV kV

SWITCHING CHARACTERISTICS

The ● denotes specifications that apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C, C_L = 20pF, V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V; unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{LOADL}	$\overline{LOAD}$ Low Pulse Width		●	20			ns
$t_{DLYLOAD2}$	$\overline{LOAD}$↓ to $\overline{LOAD2}$↓ Delay (Aperture Delay)		●	12	21	33	ns
$t_{PWLOAD2}$	$\overline{LOAD2}$ Low Pulse Width	(SCK2 Frequency ≥ 40MHz)	●	20		52	ns
		(SCK2 Frequency ≤ 33MHz)	●	35		80	ns
	$\overline{LOAD}$ to $\overline{LOAD2}$ Falling Edge Jitter RMS	(Note 7)			30		ps
	$\overline{LOAD}$ High Time		●	100			ns
SPI Timing							
t_{SCK}	SCK Input Period	SCK2 Frequency 50MHz (Note 8)	●	20		2300	ns
t_{SCKH}	SCK Input High Time	SCK2 Frequency 50MHz	●	9			ns
t_{SCKL}	SCK Input Low Time	SCK2 Frequency 50MHz	●	9			ns
t_{SUMOSI}	MOSI Setup Time to SCK↑	(Note 2)	●	1.5			ns
t_{HMOSI}	MOSI Hold Time to SCK↑	(Note 2)	●	1			ns
$t_{DLYSSLOAD}$	$\overline{SS}$ or $\overline{SSB}$ Delay to $\overline{LOAD}$↓ Quiet Time		●	100			ns
t_{DMISO}	MISO Data Valid Delay from SCK↑, SCK2 Selection > 50MHz	V_L = 5.5V (Note 2) V_L = 2.5V (Note 2) V_L = 1.71V (Note 2)	● ● ●		5	7.5 8 9.5	ns ns ns
t_{DMISO}	MISO Data Valid Delay from SCK↓, SCK2 Selection ≤ 50MHz	V_L = 5.5V (Note 2) V_L = 2.5V (Note 2) V_L = 1.71V (Note 2)	● ● ●		5	7.5 8 9.5	ns ns ns
t_{HMISO}	MISO Data Remains Valid Delay from SCK↑	SCK2 ≥ 50MHz (Note 2)	●	1.8			ns
t_{HMISO}	MISO Data Remains Valid Delay from SCK↓	SCK2 < 50MHz (Note 2)	●	1.8			ns
$t_{DMISOSSF}$	MISO Data Valid Delay from $\overline{SS}$↓		●			9.5	ns
t_{SCK2L}	SCK2 Low Time	SCK2 Frequency 50MHz (Notes 2, 8)	●	9.1			ns
$t_{SUMISO2}$	MISO2 Data Setup Time to SCK2↑	(Note 7)	●	1.5			ns
t_{HMISO2}	MISO2 Data Hold Time from SCK2↑	(Note 7)	●	1			ns
t_{HMOSI2}	MOSI2 Data Remains Valid Delay from SCK2↓	(Note 7)	●	1			ns
t_{DMOSI2}	MOSI2 Data Valid Delay from SCK2↓	V_{L2} = 5.5V (Note 2) V_{L2} = 2.5V (Note 2) V_{L2} = 1.71V (Note 2)	● ● ●			1.5 2 3.5	ns ns ns
t_{SSFSCK}	$\overline{SS}$↓ or $\overline{SSB}$↓ Delay to SCK↑	SCK2 Frequency 50MHz (Note 8)	●	25		2300	ns
t_{DIS}	Bus Relinquish Time After $\overline{SS}$↑		●			35	ns
$t_{SCKSSDIS}$	last SCK↑ to $\overline{SS}$↑ or $\overline{SSB}$↑	SCK2 Frequency 50MHz (Note 8)	●	20		2300	ns
t_{DLYSS2}	Delay from $\overline{SS}$ to $\overline{SS2}$ or $\overline{SSB}$ to $\overline{SSB2}$	$\overline{SSB}$ to $\overline{SSB2}$ with DAC 2nd Channel			22		ns
$t_{SCKRSCK2F}$	Delay SCK↑ to SCK2↓	SCK2 Frequency 50MHz			22		ns

SWITCHING CHARACTERISTICS

The ● denotes specifications that apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C, C_L = 20pF, V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V; unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DLYSCKMOSI2}$	Delay SCK↑ to MOSI2 Valid				24		ns
$t_{DLYMOSI2SCK2}$	Setup MOSI2 to SCK2↑	(Note 2)	●	1.5			ns
$t_{SSSPACE}$	$\overline{SS}$↑ or $\overline{SSB}$↑ Space to $\overline{SS}$↓ or $\overline{SSB}$↓		●	60			ns
$t_{SS2FSCK2}$	$\overline{SS2}$↓ or $\overline{SSB2}$↓ Delay to SCK2↑	SCK2 Frequency 50MHz	●	45			ns
$t_{SCK2SS2DIS}$	Last SCK2↑ to $\overline{SS2}$↑ or $\overline{SSB2}$↑	SCK2 Frequency 50MHz	●	32			ns
	MISO Rise/Fall Time	(Note 7)			500		ps
	$\overline{LOAD2}$, $\overline{SS2}$, $\overline{SSB2}$, MOSI2, SCK2 Rise/Fall Time	(Note 7)			500		ps
Select Signals							
	SA, SB, SC Propagation Delay	1.71V ≤ V_L ≤ 5.5V	●	40	80	150	ns
	SA2, SB2, SC2 Rise/Fall Time	1.71V ≤ V_{L2} ≤ 5.5V	●		10	20	ns

ISOLATION CHARACTERISTICS

T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage (Notes 4, 5, 6)	1 Minute, Derived from 1 Second	6000			V_{RMS}
		1 Second	7200			V_{RMS}
	Common Mode Transient Immunity	V_{CC} = V_L = ON = 5V to GND, V_{CC2} = V_{L2} = ON2 = 5V to GND2, 1000V in 20ns Transient Between GND and GND2 (Note 7)	50	100		kV/µs
V_{IORM}	Maximum Working Insulation Voltage	(Note 2)	1000 690			V_{PEAK}, V_{DC} V_{RMS}
	Partial Discharge	V_{PD} = 1830V_{PEAK} (Note 4)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.2		mm
	Input to Output Resistance	(Notes 2, 4)	1	5		TΩ
	Input to Output Capacitance	(Notes 2, 4)		3		pF
	Creepage Distance	(Note 2)		9.2		mm

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. Guaranteed by design, not production tested.

Note 3. Maximum data rate is guaranteed by other measured parameters and is not directly tested.

Note 4. Device considered a 2-terminal device. Measurement between groups of pins A1 through C6 shorted together and pins N1 through R6 shorted together.

Note 5. The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 6. In accordance with UL1577, each device is proof tested for the 6000V_{RMS} rating by applying an RMS voltage multiplied by an acceleration factor of 1.2 for one second.

Note 7. Evaluated by Design, not production tested.

Note 8. See Table 4 and Table 5 for minimum and maximum timing specifications affected by the selection of SCK2 frequencies in the configuration register.

Note 9. All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to their corresponding ground unless otherwise specified.

Note 10. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

TIMING SPECIFICATIONS

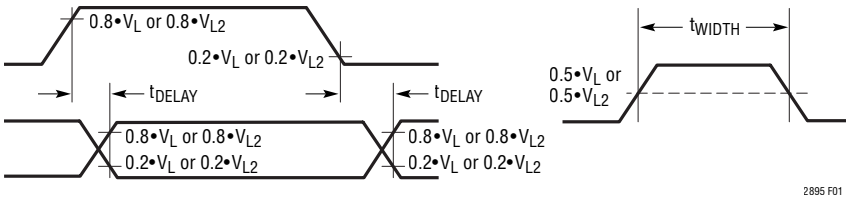
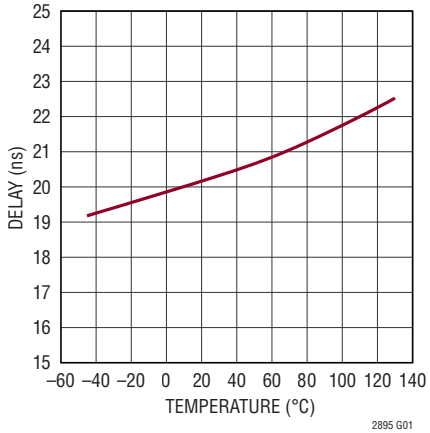


Figure 1. Voltage Levels for Timing Specifications

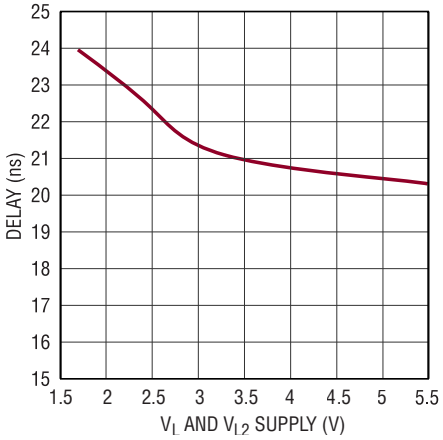
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 5.0V, GND2 = 0V, unless otherwise noted.

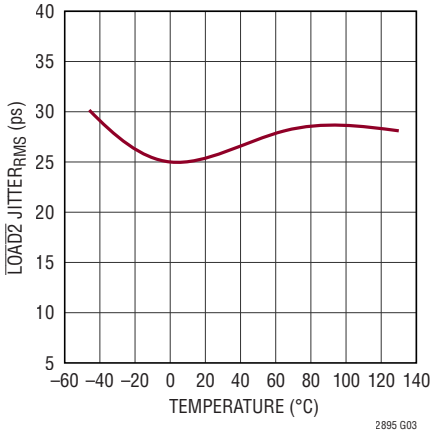
$\overline{LOAD}$ to $\overline{LOAD2}$ Delay vs Temperature



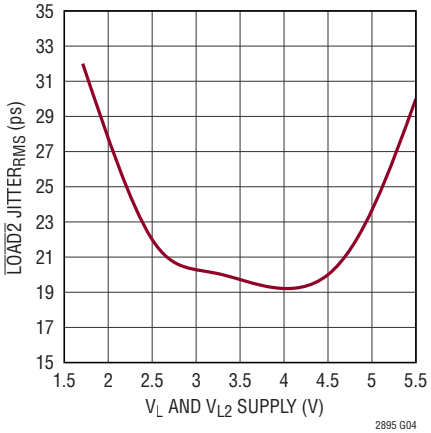
$\overline{LOAD}$ to $\overline{LOAD2}$ Delay vs V_L and V_{L2}



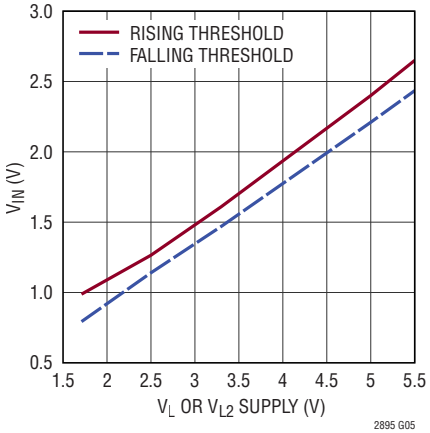
$\overline{LOAD2}$ $Jitter_{RMS}$ vs Temperature



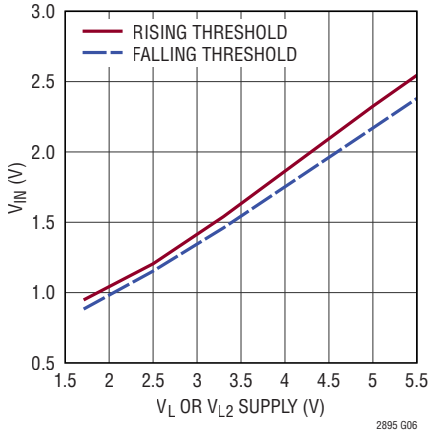
$\overline{LOAD2}$ $Jitter_{RMS}$ vs V_L and V_{L2}



SA, SB, SC, SA2, SB2, or SC2 as Inputs V_{IN} Thresholds vs V_L or V_{L2}



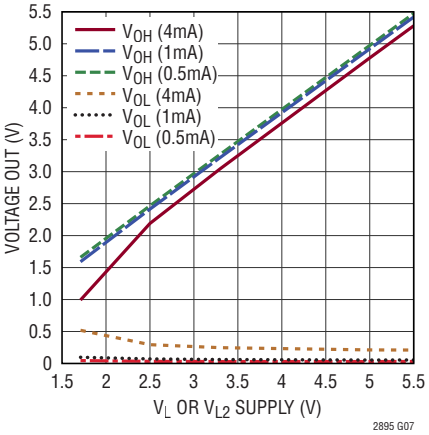
$\overline{LOAD}$ or MOSI, SCK, $\overline{SS}$, $\overline{SSB}$, MISO2 Inputs V_{IN} Thresholds vs V_L or V_{L2}



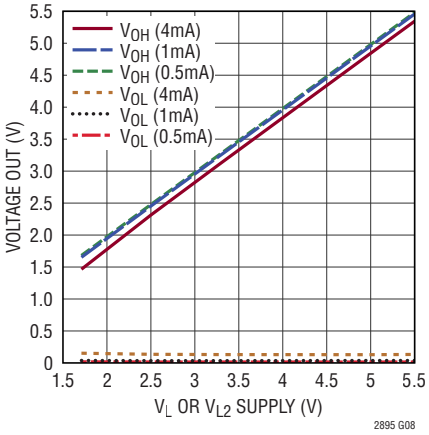
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 5.0V, GND2 = 0V, unless otherwise noted.

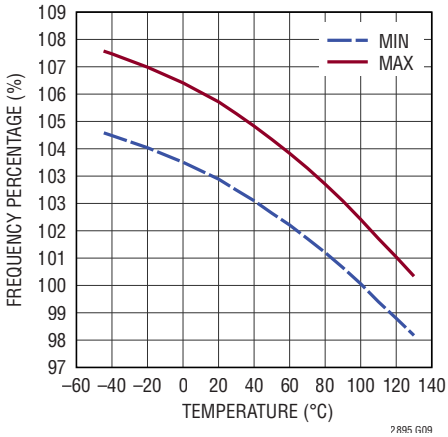
SA, SB, SC, SA2, SB2, or SC2 as Outputs V_{OL}/V_{OH} vs V_L or V_{L2} Voltage



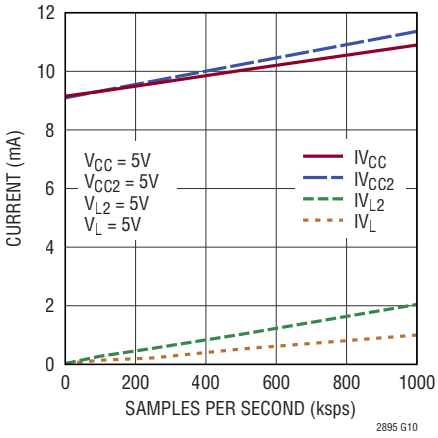
$\overline{LOAD2}$, BUSY, MISO, $\overline{SS2}$, $\overline{SSB2}$, or MOSI2 V_{OL}/V_{OH} vs V_L or V_{L2} Voltage



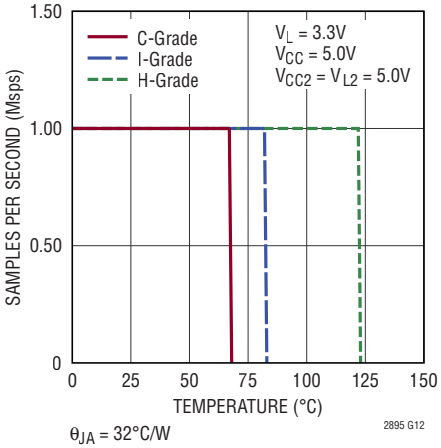
SCK2 Frequency Variation vs Temperature



Supply Current vs Sampling Rate



Temperature Derating Curve



PIN FUNCTIONS

Logic Side

(All Logic Side Inputs and Outputs Referenced to V_L and GND).

ON (A1): LTM2895 Enable. A high input enables the LTM2895 logic side. Do not float. When ON is low and V_L is high, MOSI, SCK, $\overline{LOAD}$, and MISO are high impedance, an external pull-up or pull-down resistor (100k or greater) is required on each pin to minimize possible internal shoot though current if these pins float.

$\overline{SS}$ (A2): Slave Select Input (Low True Slave Chip Select). A low on the $\overline{SS}$ input enables MISO. Frame each word written or read through the isolator with the $\overline{SS}$ input. $\overline{SS}$ contains a weak pull-up to V_L. $\overline{SSB}$ must be high for $\overline{SS}$ to be enabled.

MOSI (A3): Master Out Slave In Input. Serial data to be written to the isolated DAC side (MOSI2). MOSI is also the serial data input for the configuration registers. Add a weak pull-up or pull-down resistor to MOSI pin to set valid logic condition during the high impedance state.

SCK (A4): Serial Port Clock Input. MISO data changes after a rising edge of the SCK input. MOSI data is read in on the rising edge of the SCK input. Add a weak pull-down resistor to SCK to set a valid logic condition if in a high impedance state.

BUSY (A5): Busy Output. A High on the BUSY output indicates the isolator is in progress of startup and the isolated side is not ready. When BUSY goes low, the system is ready.

$\overline{LOAD}$ (A6): DAC Load Input. The falling edge of the $\overline{LOAD}$ signal is transferred to the $\overline{LOAD2}$ output with low jitter creating a narrow 25ns to 80ns pulse. Do not change the $\overline{LOAD}$ input during a read or write of the serial digital interface. $\overline{LOAD}$ is not necessary and is dependent on the DAC requirements. If the LTM2895 is in a generic SPI application or the DAC does not use a $\overline{LOAD}$ signal, connect $\overline{LOAD}$ to V_L. Do not float.

V_L (B1): Logic Interface Supply. Recommended operating voltage is 1.71V to 5.5V. Interface supply voltage for pins SA, SB, SC, ON, MISO, MOSI, SCK, $\overline{SS}$, $\overline{SSB}$, BUSY, $\overline{LOAD}$. Internally bypassed to GND with 1µF.

MISO (B2): Master In Slave Out Output. Serial data output containing the DAC result from MISO2. MISO is high impedance when $\overline{SS}$ is high. Add a weak pull-up or pull-down resistor to MISO pin to set a valid logic condition during the high impedance state.

GND (B3, B5, C2, C3): Circuit Ground. Return for V_L logic supply and V_{CC} supply.

$\overline{SSB}$ (B4): Chip Select Configuration Input ($\overline{SSB}$ Chip Select). A low on the $\overline{SSB}$ input enables access to the configuration register. If configured for a 2nd DAC channel, the $\overline{SSB}$ signal is configured as a second slave select. Configuration Registers section describes configurable options. $\overline{SSB}$ contains a weak pull-up to V_L. $\overline{SS}$ must be high for $\overline{SSB}$ to be enabled.

$\overline{FAULT}$ (B6): Fault Output Open Drain. A low on the $\overline{FAULT}$ output indicates a communication or command error. Connect to an external 10k pull-up to V_L to monitor fault events.

V_{CC} (C1): Supply Voltage. Recommended operating voltage is 3.0V to 5.5V. Internally bypassed to GND with 1µF.

SA (C4): Select Enable Channel A. Select signal pass through to SA2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur within 150ns of a $\overline{LOAD}$, $\overline{SSB}$, or $\overline{SS}$ edge. See section SA, SB, SC Safe Transition Regions for timing constraints. Do not use as a general purpose asynchronous signal. SA contains a weak pull-down. Direction is set in the configuration register. Connect to GND when not used.

SB (C5): Select Enable Channel B. Select signal pass through to SB2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur within 150ns of a $\overline{LOAD}$, $\overline{SSB}$, or $\overline{SS}$ edge. See section SA, SB, SC Safe Transition Regions for timing constraints. Do not use as a general purpose asynchronous signal. SB contains a weak pull-down. Direction is set in the configuration register. Connect to GND when not used.

PIN FUNCTIONS

SC (C6): Select Enable Channel C. Select signal pass through to SC2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur within 150ns of a $\overline{\text{LOAD}}$, $\overline{\text{SSB}}$, or $\overline{\text{SS}}$ edge. See section SA, SB, SC Safe Transition Regions for timing constraints. Do not use as a general purpose asynchronous signal. SC contains a weak pull-down. Direction is set in the configuration register. Connect to GND when not used.

Isolated Side

(All Isolated Side Inputs and Outputs Referenced to V_{L2} and GND2).

V_{CC2} (N1): Isolated Voltage Supply. Recommended operating voltage is 3.0V to 5.5V. Internally bypassed to GND2 with 1µF.

GND2 (N2, N3, P3, P5): Isolated Ground Return. Keep separate from GND.

SA2 (N4): Select Enable Channel A. Select signal pass through from SA to control an external multiplexer or programmable gain amplifier. See section SA, SB, SC Safe Transition Regions for timing constraints. Do not use as a general purpose asynchronous signal. SA2 contains a weak pull-down. Direction is set in the configuration register.

SB2 (N5): Select Enable Channel B. Select signal pass through from SB to control an external multiplexer or programmable gain amplifier. See section SA, SB, SC Safe Transition Regions For timing constraints. Do not use as a general purpose asynchronous signal. SB2 contains a weak pull-down. Direction is set in the configuration register.

SC2 (N6): Select Enable Channel C. Select signal pass through from SC to control an external multiplexer or programmable gain amplifier. See section SA, SB, SC Safe Transition Regions for timing constraints. Do not use as a general purpose asynchronous signal. SC2 contains a weak pull-down. Direction is set in the configuration register.

V_{L2} (P1): Interface Supply Voltage. Recommended operating voltage is 1.71V to 5.5V. Interface supply voltage for pins SA2, SB2, SC2, MISO2, MOSI2, SCK2, $\overline{\text{SS2}}$, $\overline{\text{SSB2}}$ and $\overline{\text{LOAD2}}$. Internally bypassed to GND2 with 1µF.

MISO2 (P2): Master In Slave Out Input. Serial data input receiving the results from a general SPI device or a read back from a DAC. MISO2 is high impedance when $\overline{\text{SS2}}$ and $\overline{\text{SSB2}}$ are high. MISO2 has a weak pull-down to maintain a valid logic low during high impedance conditions when ON2 is high. Connect to GND if not used.

$\overline{\text{SSB2}}$ (P4): Isolated Side Second Slave Select Output (Slave Chip Select 2). Output controlled by internal communication functions to write data to a second DAC or SPI interface.

DNC (P6): Do Not Connect.

ON2 (R1): Isolated Interface Enable. A high input enables the isolated side communication interface. Do not float. When ON2 is low and V_L is high, $\overline{\text{LOAD2}}$, MOSI2, SCK2, and MISO2 are high impedance, an external pull-up or pull-down resistor (100k or greater) is required on each pin to minimize possible internal shoot though current if these pins float.

$\overline{\text{SS2}}$ (R2): Isolated Side Slave Select Output (Slave Chip Select). Output controlled by internal communication functions to write data to slave DAC.

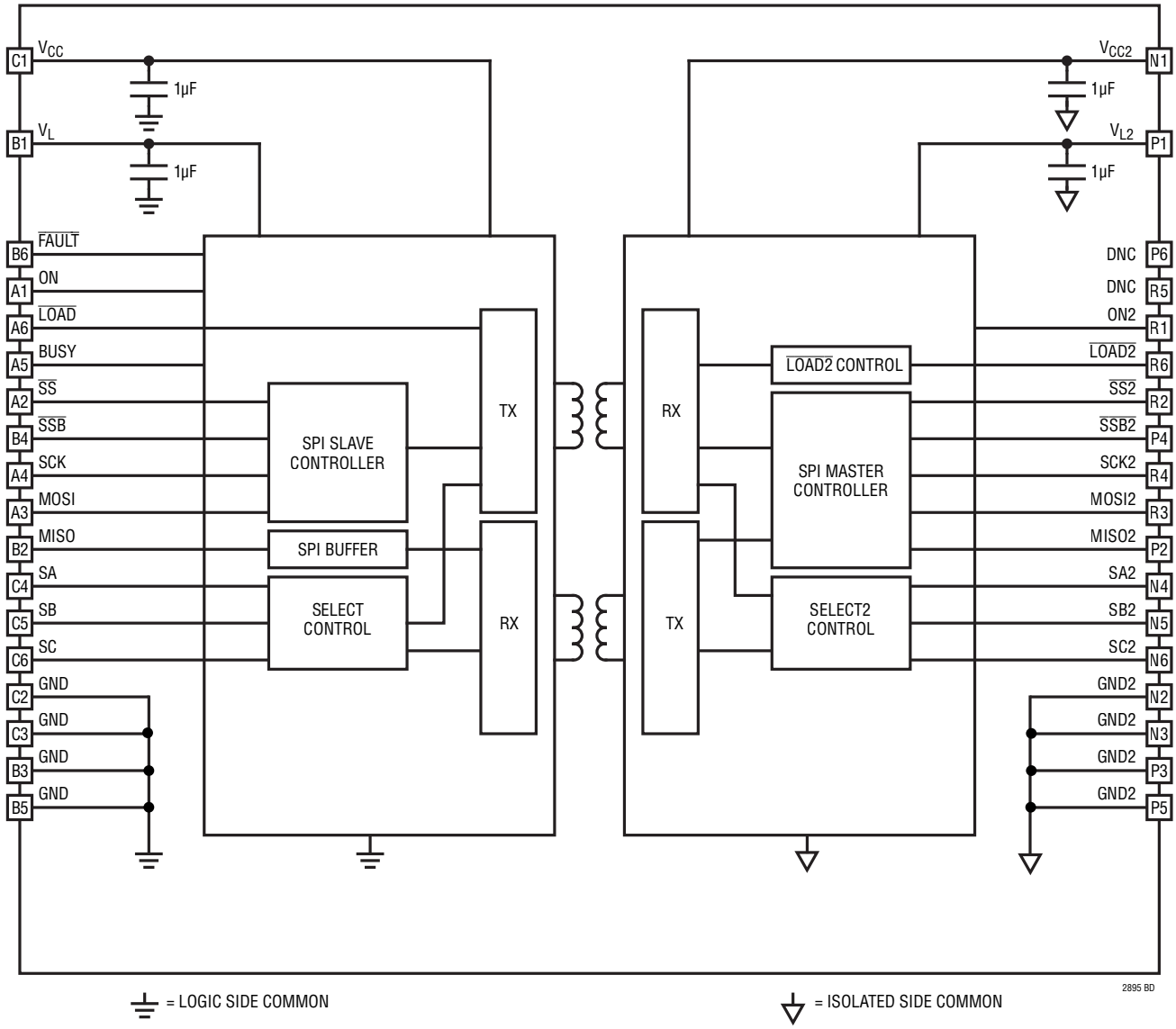
MOSI2 (R3): Isolated Master Out Slave In Output. Serial data output sending command data to the DAC.

SCK2 (R4): Isolated Serial Clock Output. Serial clock output to the SPI interface. SCK2 is low when $\overline{\text{SS2}}$ is high.

DNC (R5): Do Not Connect.

$\overline{\text{LOAD2}}$ (R6): Isolated Load DAC Output. Connect to DAC LDAC input. If unused connect to V_{L2} with a 100k pull-up. Do not float.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

The LTM2895 µModule transceiver provides a galvanically isolated robust SPI interface including decoupling capacitors. This flexible device can support a variety of configurations and SCK frequencies. The LTM2895 is ideal for breaking ground loops, noise isolation, protecting equipment, or level shifting to a different ground reference. Error free operation is maintained through common mode events exceeding 50kV/µs, providing excellent noise isolation.

The LTM2895 can drop into most 4-wire SPI applications from 500kHz to 50MHz, without any configuration required. To meet the specific needs of other SPI and DAC applications, the LTM2895 can be personalized with a configuration register allowing eight frequency and eight word-length choices. The LTM2895 operates as a slave SPI interface on the logic side and as a master SPI interface on the isolated side. Only the necessary signal edges are transferred across the isolation barrier and the SPI pattern is recreated on the isolated side. Data read back from the isolated side is temporarily stored in a buffer and the result is delayed by one word-length. See Figure 9 for a timing diagram of the SPI interface across the LTM2895.

Additional isolated signals are included to support features of an isolated SPI device. DACs that support a LOAD DAC input can use the low jitter $\overline{\text{LOAD}}$ signal for updating their outputs. Reset, clear, or multiplexer functions are supported with the bidirectional select signals SA, SB, and SC.

A fault detection system watches for errors in input conditions and isolated data corruption and reports on a single open drain $\overline{\text{FAULT}}$ output.

ISOLATOR µModule TECHNOLOGY

The LTM2895 utilizes isolator µModule technology to translate signals across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using differential signaling through coreless transformers formed in the µModule substrate. This system, complete with error checking, fault detection on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with our SPI transceiver in one small package.

SPI REQUIREMENTS

The SPI bus lacks a formal standard and, therefore, various implementations of protocol, bit lengths, and signal polarities exist. In the universe of devices with serial peripheral interfaces (SPI), a nominal set of requirements must be met to operate properly with the LTM2895. The signal flow of a standard SPI protocol is used with a requirement that the $\overline{\text{SS}}$ (Chip Select) signal frames the transaction. The LTM2895 supports SPI mode (0, 0), where SCK captures on the rising edge (CPHA = 0) and SCK starts low and transitions high (CPOL = 0).

The following list summarizes the requirements for using the LTM2895.

- Configure the SCK2 frequency to the master and application device requirements
- SPI operates in mode (0, 0) (rising edge SCK captures data)
- Chip Select signal ($\overline{\text{SS}}$ or $\overline{\text{SSB}}$) frames SPI pattern and meets watchdog timeout requirements

First, the SCK2 frequency is selected to operate with the device connected to the isolated side of the LTM2895. The SCK2 frequency sets the low time of the clock signal (t_{SCK2L}) out of the LTM2895 and into the isolated SPI interface. See section SCK2 FREQUENCY for specific timing information. The master SCK frequency must be equal or slower than the SCK2 frequency and greater than the watchdog timeout.

Second, the LTM2895 logic side operates in mode (0, 0) with a variation on which edge of the SCK data shifts out on. For configured SCK2 frequencies of 100MHz and 66MHz, the MOSI data is captured and the MISO data is shifted on the rising edge of SCK, as shown in Figure 2. This variation allows for additional propagation and setup time to the next rising clock (SCK) edge. All setup and hold timing characteristics are related to the rising edge of the SCK. For configured SCK2 frequencies of 50MHz and lower, MOSI is captured on the rising edge and MISO is shifted on the falling edge of SCK, as shown in Figure 3.

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The isolated side always operates in mode (0, 0). MOSI2 sets up data on the falling edge of SCK2 and MISO2 is captured on the rising edge of SCK2.

Third, the slave selects $\overline{SS}$ and $\overline{SSB}$ must be dedicated to framing the operation of reading or writing data. The $\overline{SS}$ or $\overline{SSB}$ must go low at the beginning of the SPI transaction prior to the SCK transitions and must go high after the last SCK rising edge transition, see Figure 4.

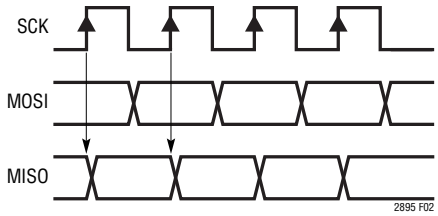

Figure 2. SCK and Data with SCK2 Frequency Configured for 100MHz or 66MHz

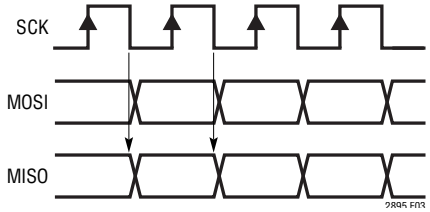

Figure 3. SCK and Data with SCK2 Frequency Configured for 50MHz or Less

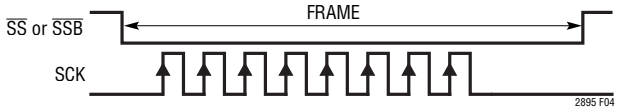

Figure 4. SPI Transaction with $\overline{SS}$ or $\overline{SSB}$ Framing SCK

$\overline{LOAD}$ INPUT

$\overline{LOAD}$ input is a low jitter path available for digital to analog converters that offers a low true LOAD DAC (LDAC) input. The $\overline{LOAD}$ to $\overline{LOAD2}$ signal is initiated on a falling edge. The rising edge of $\overline{LOAD}$ is ignored. The rising edge of $\overline{LOAD2}$ is generated internally and has up to 5ns of jitter. The low pulse width of $\overline{LOAD2}$ is dependent on the configured SCK2 frequency. For SCK2 frequencies of 40MHz or greater, $\overline{LOAD2}$ has a pulse width of ~40ns, and for SCK2 frequencies of 33MHz or below, $\overline{LOAD2}$ has a pulse width of ~60ns.

$\overline{LOAD}$ is not necessary to interact with the isolated SPI device. When $\overline{LOAD}$ is unused connect it to V_L.

READ BACK DATA

Data can be read back from the isolated side MISO2 pin to MISO. The data read out of the MISO pin has one word of latency. The MISO pin is only utilized during transactions when the primary chip select, $\overline{SS}$, is active. When data is read from the isolated side, it is placed in a buffer on the logic side. The current data in the buffer is shifted out on the MISO output. New data from the isolated side will fill in the buffer behind it. The very first word read out of the buffer after a startup is all “0”s.

SPI PAGE MODE

SPI page mode allows large data transfers of multiple words within a slave select frame. To operate in page mode beyond the defined wordlength, maintain $\overline{SS}$ low and continue clocking SCK the desired number of word-length multiples. SCK must end on a wordlength boundary. Further, maintain the timing between rising edges of SCK and the timing between $\overline{SS}$ and SCK so a watchdog event is not triggered.

The read back data on MISO is one word-length delayed. See Figure 14 for an example of page mode operation and the relationship of words into and out of the LTM2895.

STARTUP

The LTM2895 has an internal startup communication routine to verify both sides of the isolation are ready for communication. The startup routine is initiated when power is supplied to V_{CC} and V_{CC2} inputs above 2.75V, V_L and V_{L2} inputs above 1.5V, the logic side ON signal is high, and the isolated ON2 signal is high. The BUSY signal will go high and then low indicating the two internal isolators have completed a startup routine. Once the BUSY output goes low, the system is ready.

The isolated ON2 pin allows independent enabling of the isolator. External voltage monitoring can be used to enable the ON2 input when all isolated supplies and systems are ready.

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BUSY INDICATOR

During startup, the BUSY output is set high to indicate the LTM2895 is powering up and will be de-asserted when isolated communication is verified through a startup routine. Monitor the BUSY output as a system ready signal.

If BUSY goes high during a $\overline{FAULT}$, the internal watchdog timer has been asserted. See section Watchdog Timer for an explanation of situations that cause a watchdog timeout.

$\overline{FAULT}$ REPORTING

A $\overline{FAULT}$ pin is supplied to indicate the occurrence of a communication error or an erroneous input condition. The $\overline{FAULT}$ pin is open drain and requires an external pull-up resistance (10k) to the V_L supply. If the $\overline{FAULT}$ pin is asserted low, data loss may have occurred and the current transaction may be invalid. To clear the $\overline{FAULT}$ pin, return $\overline{LOAD}$ to a high and $\overline{SS}$ and $\overline{SSB}$ to a high and initiate a new transition on one of these signals.

Possible fault conditions are listed in Table 1. Other than a watchdog timeout, the LTM2895 does not indicate which condition caused the fault.

Table 1. Fault Reporting

FAULTS	CAUSE/TROUBLESHOOTING
Idle time during serial digital interface read (watchdog expired), see Table 4	SCK↑ to SCK↑ > $t_{WATCHDOG\_TIMEOUT}$ ns. Minimize the delay between this relationship to less than $t_{WATCHDOG\_TIMEOUT}$ ns.
Transient data loss in isolation communication	Common mode transients (GND to GND2) greater than 50kV/µs. High transient EM field disturbances greater than specified in EN61000, or an ESD event.
Isolated side power loss	ON2, V_{L2}, or V_{CC2} was removed and returned. Indicates unexpected interface loss.
$\overline{LOAD}$ falling edge during serial digital interface read	Avoid transitioning $\overline{LOAD}$ during the read/write of the serial digital interface. $\overline{LOAD}$ will be ignored during the read of the serial digital interface.
Buffer under run	SCK frequency exceeds the SCK2 frequency.

WATCHDOG TIMER

The LTM2895 contains a watchdog timer to monitor interactions between the SPI port and the isolated communication. The watchdog looks for stalled communication on pins $\overline{SS}$ and SCK. A stalled or delayed input on SCK when $\overline{SS}$ is low for a longer time than t_{SCK2} • 128 will flag a fault and reset the core logic. At the maximum SCK2 frequency of 100MHz, the watchdog will timeout if $\overline{SS}$ is low without an SCK transition for greater than 1.25µs. The Table 4 column $t_{WATCHDOG\_TIMEOUT}$ quantifies the trip points for the watchdog for each SCK2 frequency configuration.

The $\overline{FAULT}$ output will be asserted low along with the BUSY output asserted high, when a watchdog timeout occurs. A Fault due to the watchdog will clear the configuration register and re-writing the configuration registers is necessary.

CONFIGURATION REGISTER

The LTM2895 contains a configuration register to adjust parameters of the speed and features of the SPI write and read process. After powering up the LTM2895, and after BUSY goes low, write the configuration register by asserting the $\overline{SSB}$ chip select input low and clock in a one byte configuration word with SCK and MOSI. Two registers are addressable with the most significant bit of the configuration byte. Complete each configuration word by reasserting $\overline{SSB}$ high. The isolated side will be automatically configured to match the logic side. By default SCK2 = 50MHz, SA, SB, SC = 0, and the wordlength is 8 bits.

See Table 3 for the configuration register bit map for controlling the operation and frequency of the logic and isolated SPI ports. The configuration register allows adjustment of the default SCK2 frequency, direction of the SA, SB, SC to SA2, SB2, SC2 signals, and the length of the SPI word.

DUAL CHIP SELECTS ($\overline{SS}$ AND $\overline{SSB}$)

The primary chip select $\overline{SS}$ passes through the isolator to $\overline{SS2}$. The second chip select, $\overline{SSB}$, by default is the enable to the configuration register. $\overline{SSB}$ can be configured as a second slave select, through the configuration register bit 5 (D5) “DAC 2nd Channel” in configuration register 1, address AD7. The “DAC 2nd Channel” bit converts the $\overline{SSB}$ signal from accessing the configuration registers into a second slave select that is communicated across the isolation barrier to output $\overline{SSB2}$. Once the “DAC 2nd

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Channel" is selected, the LTM2895 cannot be reconfigured until a reset due to toggling the ON pin or power loss and recovery. When configured for DAC 2nd Channel, the $\overline{SSB2}$ output can be connected to a second DAC or SPI interface device. The MOSI and SCK pins are shared. The two slave selects are then accessed sequentially requiring a short pause of duration $t_{SSSPACE}$ in between where both the $\overline{SS}$ and $\overline{SSB}$ are high. MISO does not read back from the second channel when $\overline{SSB}$ to $\overline{SSB2}$ is active. MISO is dedicated to reading back data from the primary channel ($\overline{SS}$ to $\overline{SS2}$) only.

The clock speed and wordlength are the same for both channels. Consider the page mode functionality if the word-lengths are different but multiples of one another. An example of this is a primary channel with a 32-bit word-length requirement and secondary channel with a 16-bit word-length requirement. Set the LTM2895 wordlength configuration to 16 bits.

SCK2 FREQUENCY

The SCK2 frequency selection list is shown in Table 4. The selected SCK2 frequency sets the minimum and maximum range the SCK frequency can operate at and sets the fixed low time of SCK2 (t_{SCK2L}). The low time of SCK2 (t_{SCK2L}) sets the setup time of the MOSI2 output to SCK2 rising ($t_{SUMOSI2}$). The Isolated side SCK2 is not a free running shift clock. Each falling edge of SCK2 is driven directly from the rising edge of SCK as shown in Figure 5.

Select the SCK2 frequency that is equal or less than the specifications of the application device's SPI port from Table 2.

SCK2 minimum low time (t_{SCK2L}) must be greater than the following characteristics of the application device:

- Minimum low time of the shift clock (SCK) required by the isolated SPI device
- The required setup time from the isolated SPI device's SDI to SCK
- The data valid response on the SPI device's SDO to the LTM2895's MISO2 setup requirement to SCK2 rising

Example: the LTC®2642 has a minimum SCK low time of 9ns, and a minimum SDI to SCK setup time of 10ns; therefore, configure SCK2 frequency for 40MHz (t_{SCK2L} = 11.4ns) or less. The logic side SPI SCK frequency cannot exceed the SCK2 frequency. Access the LTM2895 with an SCK frequency between the configured SCK2 and ~0.009 • SCK2. This guarantees the internal SPI transfer will not under-run or exceed a watchdog timeout and assert a $\overline{FAULT}$. In the case of an under-run, the $\overline{FAULT}$ flag will assert low.

Table 2. SCK2 Selection to Margin Setup and Low Time

SCK2 Selection (MHz)	t_{SCK2L} Minimum (ns)
100	4.5
66	9.1
50	9.1
40	13.8
33	13.8
25	18.2
12.5	36.4
6.25	72.9

SCK2 DUTY CYCLE

The SCK2 output frequency will match that of SCK, but will not have the same duty cycle unless the frequency of SCK equals the frequency of SCK2. The high time of SCK2 will extend and the low time of SCK2 will remain at the defined low time of the configuration frequency t_{SCK2L} as shown in Figure 5. The high time of SCK2 compensates for the difference between the external SCK frequency and the internal oscillator creating the low time of SCK2.

SELECT SIGNALS

The select signal channels SA, SB, and SC are communicated to the isolated side channels SA2, SB2, and SC2, respectively. The select signals allow control of an external device related to the SPI channel. Analog multiplexers or programmable gain amplifiers with logic control signals are examples of devices to use with the select signals. The signals can be used as logic controls for clear, reset, or power down functions that are not expected to occur during processing of a SPI transaction. The select signals are not designed for use as general purpose logic signals with asynchronous transition times. Use of these signals

TYPICAL APPLICATIONS

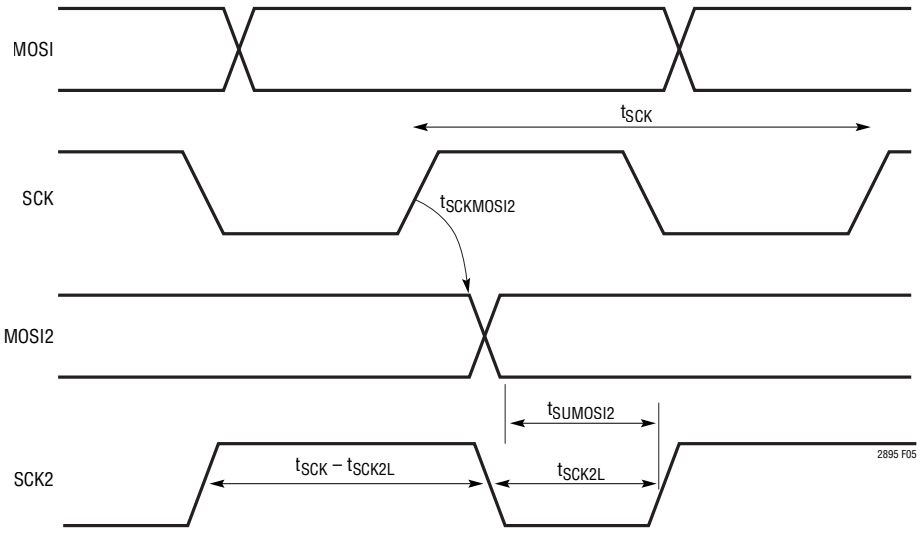

Figure 5. SCK to SCK2 and MOSI to MOSI2 Data Transfer Relationship

must be kept synchronous and outside of the operation of the $\overline{LOAD}$, $\overline{SSB}$, or $\overline{SS}$ active duration. Data and time sensitive information may be lost if a select signal transitions within 150ns of the $\overline{LOAD}$, $\overline{SSB}$ or $\overline{SS}$ signal.

The select signals are sampled and transferred as a packet of the current value of the three signals. The select signal sampling will have up 10ns of sampling jitter. If a signal transitions after another signal was sampled and is in the process of being transferred to the adjacent side, it will be delayed until an available transmission slot is available. The delay may cause a perceived jitter or uncertainty of 80ns.

SELECT SIGNALS DIRECTION

Within the configuration register SA, SB, and SC direction bits allow independent selection of the direction of signal flow from logic-to-isolated or isolated-to-logic. The default direction for each select signal is logic-to-isolated. Loading a "1" into a direction bit will change the direction of that pin to isolated-to-logic. When a "1" is loaded into the direction bit of a specific select signal the logic side select signal will become an output and the isolated side select signal will become and input.

Warning: Careful planning is required for the use of SA, SB, and SC signals. The SA, SB, SC signals must not change state within 150ns prior to $\overline{LOAD}$, $\overline{SSB}$, or $\overline{SS}$ on the logic side. If a signal is configured for isolated-to-logic signal flow, it must not change state within 150ns prior to when $\overline{SS}$ or $\overline{SSB}$ is asserted by the LTM2895. Figure 11 shows the regions were transitions are safe and not safe for the logic side interface.

WORDLENGTH

The word-length configuration bits (D0 – D2, configuration register 0) sets the number of bits per word. The word-length assignment allows the SPI access to be tailored to a specific DAC data length to maximize throughput. Table 6 lists the available combinations. If the master device requires byte-wide increments, set wordlength to a byte size boundary (8, 16, 24, or 32).

For example, a single 16-bit DAC is configured with a wordlength of 16. Two 16-bit DACs in parallel ($\overline{CS}$ of DAC1 connected to $\overline{SS2}$ and $\overline{CS}$ of DAC2 connected to $\overline{SSB2}$) are also configured with a wordlength of 16.

Figure 12 through Figure 14 demonstrates the LTM2895 in a number of flexible applications.

DIGITAL INTERFACE

The flexible V_L and V_{L2} supplies allows the LTM2895 to communicate with digital logic operating between 1.71V and 5.5V, including 2.5V and 3.3V systems.

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Table 3. Configuration Registers

	BIT 7 ADDRESS (AD7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
Configuration Register 0	0	OSCDIV2	OSCDIV1	OSCDIV0	Reserved “0”	SC Direction 0 = Logic-to-ISO 1 = ISO-to-Logic	SB Direction 0 = Logic-to-ISO 1 = ISO-to-Logic	SA Direction 0 = Logic-to-ISO 1 = ISO-to-Logic
Configuration Register 1	1	Reserved “0”	DAC 2nd Channel	Reserved “0”	Reserved “0”	WORDLENGTH2	WORDLENGTH1	WORDLENGTH0

Table 4. SCK2 Frequency Selection Table (Configuration Register 0 BIT 6, 5, and 4)

OSCDIV2 (BIT 6)	OSCDIV1 (BIT 5)	OSCDIV0 (BIT 4)	SELECTED SCK2 AND MAXIMUM SCK FREQUENCY (MHz)	MINIMUM t_{SCK2L} TIME (ns)	MINIMUM SCK FREQUENCY (kHz)	$t_{WATCHDOG\_TIMEOUT}$ MAXIMUM t_{SCK} PERIOD OR IDLE TIME WITH $\overline{SS}$ LOW (t_{SSFSCK}, $t_{SCKSSDIS}$) (µs)
0	0	0	100	4.5	909	1.1
0	0	1	66	9.1	588	1.7
0	**1**	**0**	**50**	**9.1**	**435**	**2.3**
0	1	1	40	13.8	364	2.75
1	0	0	33	13.8	300	3.3
1	0	1	25	18.2	222	4.5
1	1	0	12.5	36.4	111	9
1	1	1	6.25	72.9	26.5	37

Note: Factory default setting is bold (50MHz).

Table 5. SCK Frequency Selection Timing Specifications

SCK2 FREQUENCY, MAXIMUM SCK FREQUENCY (MHz)	SCK PERIOD (t_{SCK})		t_{SSFSCK}		$t_{SCKSSDIS}$	
	MIN (ns)	MAX (µs)	MIN (ns)	MAX (µs)	MIN (ns)	MAX (µs)
100	10	1.1	20	1.1	20	1.1
66	15.15	1.70	20	1.7	25	1.7
50	**20**	**2.3**	**20**	**2.3**	**25**	**2.3**
40	25	2.75	26	2.75	30	2.75
33	30.3	3.3	26	3.3	30	3.3
25	40	4.5	30	4.5	35	4.5
12.5	80	9	50	9	55	9
6.25	160	37	95	37	95	37

Note: Exceeding Max of t_{SCK}, t_{SSFSCK}, or $t_{SCKSSDIS}$ will result in a watchdog timeout setting $\overline{FAULT}$ low, BUSY high and will require reconfiguration.

TYPICAL APPLICATIONS

Table 6. SPI WORDLENGTH Selection Table (Configuration Register 1 Bit 2, 1, 0)

BITS PER WORD (WORDLENGTH)	WORDLENGTH2 (BIT 2)	WORDLENGTH1 (BIT 1)	WORDLENGTH0 (BIT 0)
8	**0**	**0**	**0**
12	0	0	1
14	0	1	0
16	0	1	1
18	1	0	0
20	1	0	1
24	1	1	0
32	1	1	1

Note: Factory default setting is bold (8 bits).

RF, MAGNETIC FIELD IMMUNITY

The isolator µModule technology used within the LTM2895 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, Radio Frequency, Electromagnetic Field Immunity
EN 61000-4-8	Power Frequency Magnetic Field Immunity
EN 61000-4-9	Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 7.

Table 7. Immunity Testing

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz – 1GHz	10V/m
	1.4MHz – 2GHz	3V/m
	2GHz – 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

*Non IEC Method.

PCB LAYOUT

The high integration of the LTM2895 simplifies PCB layout. However, to maintain its electrical isolation characteristics and signal integrity, some layout considerations are necessary.

- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The edge rates of the DAC interface signals are between 300ps and 1ns. At these edge rates, the routing must be treated as a distributed transmission line for lengths greater than 2cm,

  $$\text{length} > t_{RISEFALL}/(2 \bullet 33.3\sqrt{\varepsilon_R}$$

  where $t_{RISEFALL}$ is in ps, the length is in cm, and ε_R is the dielectric constant of the PCB.
- Maintain like load conditions and route lengths on isolated signals MISO2, MOSI2, and SCK2 to minimize the impacts of skewing of the shift clock to the data signals.
- Maintain like load conditions and route lengths on logic signals MISO, MOSI, and SCK to minimize the impacts of skewing of the shift clock to the data signals.

TIMING DIAGRAMS

LOGIC SIDE CONFIGURATION REGISTER INTERFACE

After startup, the LTM2895 should be configured for the specific constraints of the SPI device or digital-to-analog converters with a SPI write operation unless the default configuration is suitable. The configuration register is accessed via the SPI port with a one byte word as shown in Figure 6. A separate chip select ($\overline{SSB}$) is used for configuration. Set the $\overline{SSB}$ pin low and shift in the desired configuration byte where the register address is first (MSB) followed by seven data values. Two registers are available as referenced in Table 3: Configuration Registers. Figure 6 demonstrates the access to the configuration register. The $\overline{SSB}$ signal must be pulled high after a byte is written. A second byte may be written after a short delay $t_{SSSPACE}$ to allow the data from the first byte to be registered and communicated to the isolated side.

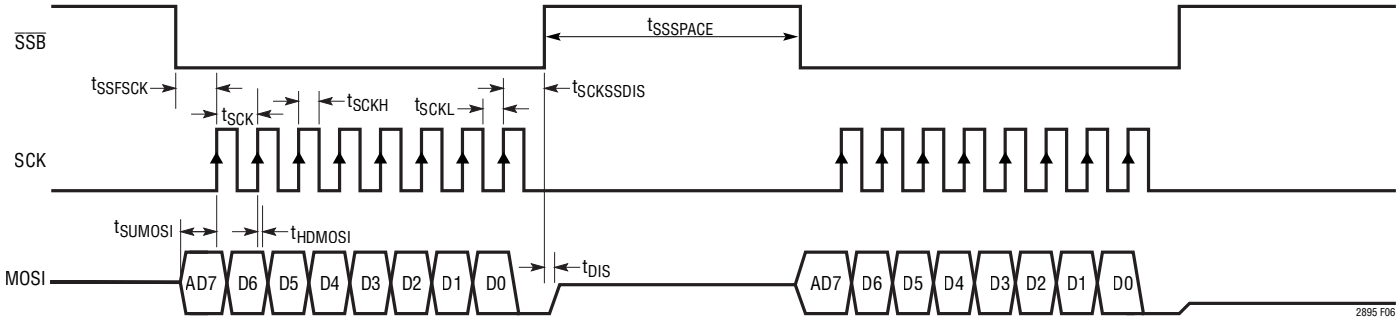
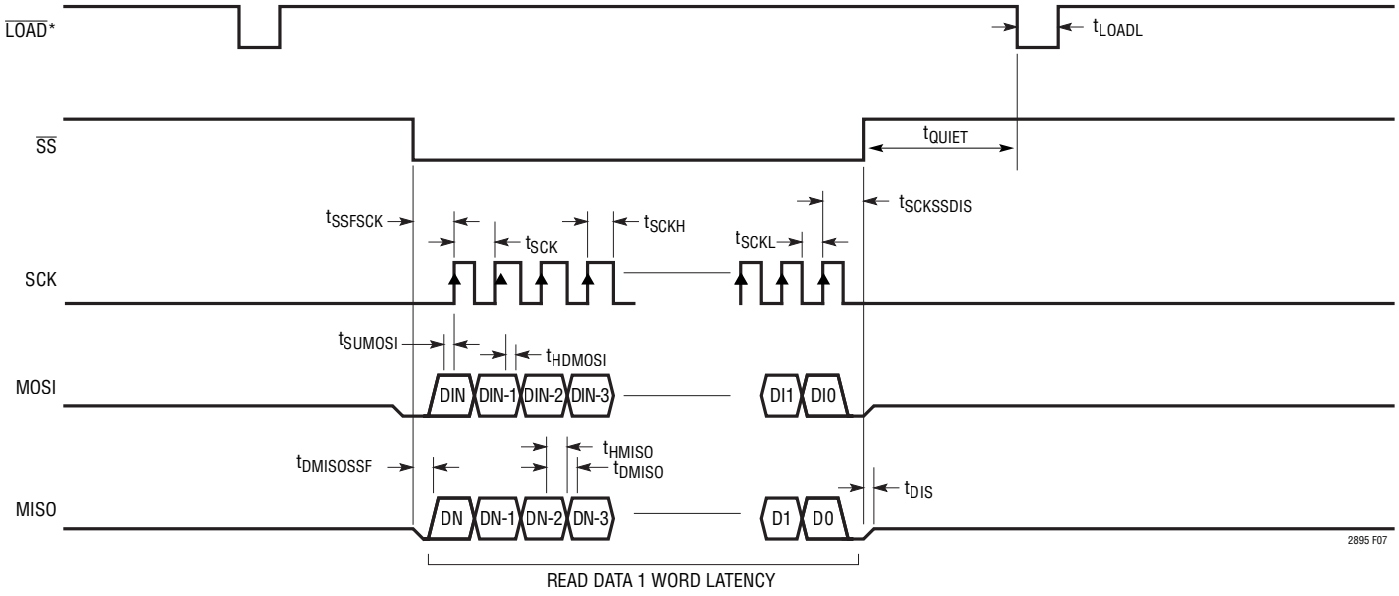


Figure 6. Writing Configuration Registers Timing Diagram

TIMING DIAGRAMS

LOGIC INTERFACE

The LTM2895 logic side interface is similar to a standard SPI interface. The $\overline{LOAD}$ signal is optional and related to DAC applications requiring accurate timed setting of the output voltage. The $\overline{SS}$ select signal frames the SPI transaction and selects the isolator path as the target for the transaction. The $\overline{SSB}$ select input frames configuration register writes or DAC 2nd channel writes. The timing of $\overline{SSB}$ is the same as $\overline{SS}$. The MISO data changes on the rising edge of the SCK input. This results in a shorter hold time for the master, but results in a maximum time for the data to settle to a valid level and maximum setup time. The MISO data word is delayed by one cycle. The MISO word is read from a buffer, which was filled on the prior transaction. At the end of the SPI transaction, after $\overline{SS}$ returns high, the quiet time to the next $\overline{LOAD}$ transition is the greater of either the minimum of $t_{DLYSSLOAD}$ or the requirements of the attached device.



*NOTE: $\overline{LOAD}$ IS NOT NECESSARY. CONNECT TO V_L IF UNUSED

Figure 7. Logic Side Interface

TIMING DIAGRAMS

ISOLATED INTERFACE

The isolated interface of the LTM2895 is driven by the signal transitions on the logic side. The $\overline{LOAD2}$ pulse width is an internally controlled parameter based on the configuration of SCK2. An SCK2 frequency selection of 50MHz or greater will result in a ~40ns $t_{PWLOAD2}$ and a 40MHz or lower frequency will result in a ~60ns $t_{PWLOAD2}$. The falling edge of $\overline{LOAD2}$ has low jitter and the rising edge has ~5ns of jitter.

When connecting a SPI device to the isolated side, select a SCK2 frequency that allows the required setup and hold time for the device and the LTM2895. See section SCK2 FREQUENCY to select the proper operating frequency. The isolated interface sets up data on the falling edge of SCK2 which matches SPI mode (0, 0). MISO2 and MOSI2 timing constraints are measured against the SCK2 falling to rising time, t_{SCK2L}.

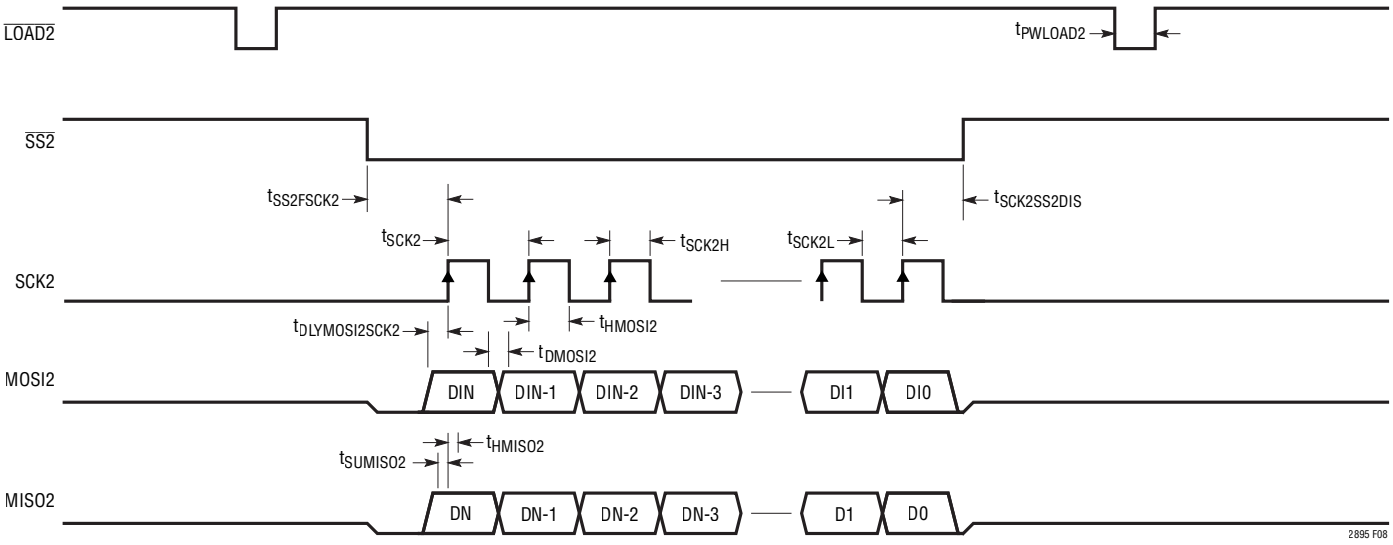


Figure 8. Logic Isolated Side Interface

TIMING DIAGRAMS

INTERFACE SIGNALING FROM LOGIC SIDE TO ISOLATED SIDE

The propagation of inputs $\overline{LOAD}$, $\overline{SS}$, $\overline{SSB}$, and data on an SCK edge to the isolated side is approximately 22ns. Each signal is monitored for specific edge information and is transferred immediately. The exception to this is the rising edge of the $\overline{LOAD}$ signal and the falling edge of SCK, which are ignored. The rising edge of SCK causes the capture and transfer of MOSI data to the isolated side. The reception of MOSI data from the logic side forces SCK2 low and sets the MOSI data value on MOSI2. The rising edge of SCK2 will occur t_{SCK2L} time later.

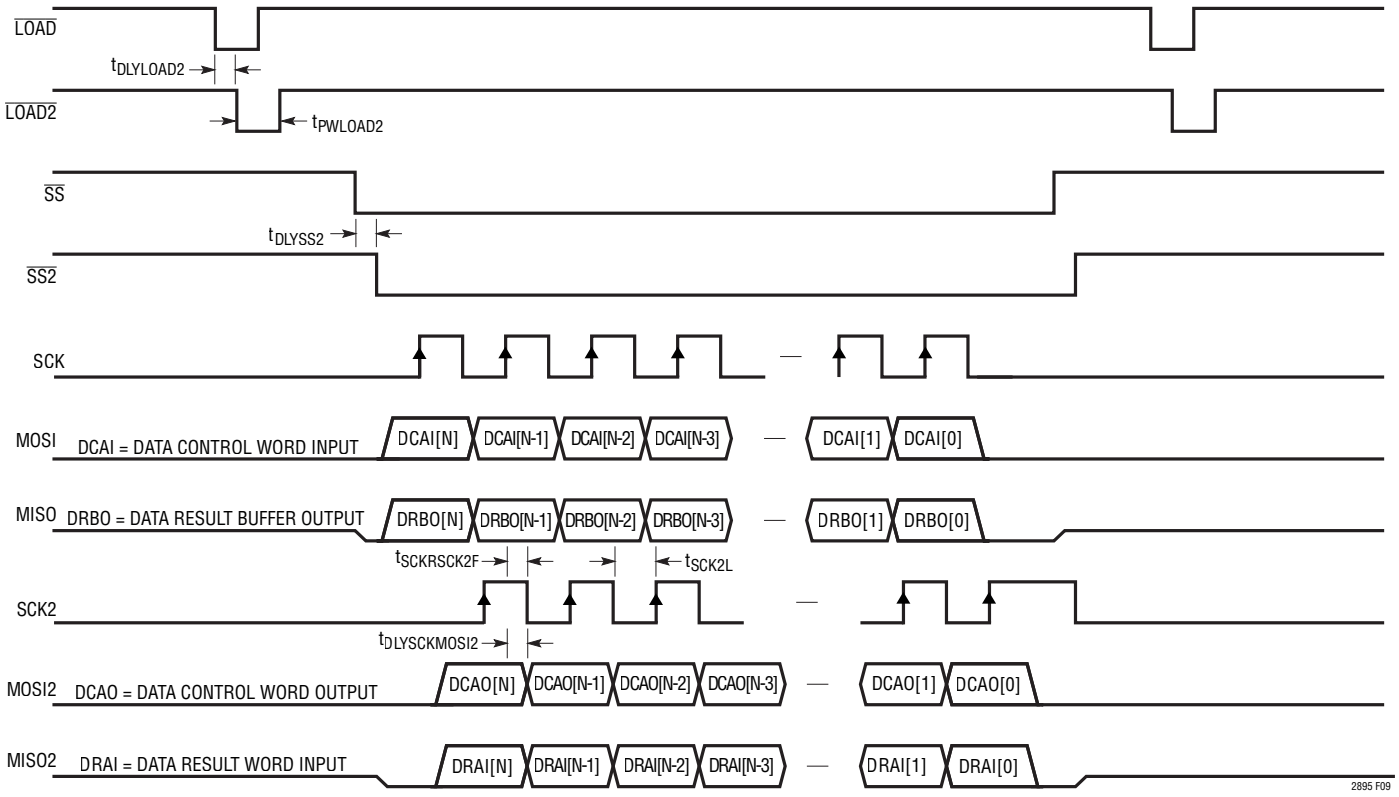


Figure 9. Logic and Isolated Side Interaction

TIMING DIAGRAMS

DUAL SPI WRITE

The dual SPI write function is enabled with the configuration register bit DAC 2nd Channel. When DAC 2nd Channel is enabled the configuration register access is disabled. The $\overline{SSB}$ select is used as an independent chip select to the isolated side output $\overline{SSB2}$. The $\overline{SSB}$ secondary channel can be written only, MISO will be 0. This configuration is useful for offset adjustment or independent DACs. The SCK and MOSI and SCK2 and MOSI2 signals are shared between the primary $\overline{SS}$ chip select and the secondary $\overline{SSB}$ chip select. Maintain $t_{SSSPACE}$ between the two chip select signals.

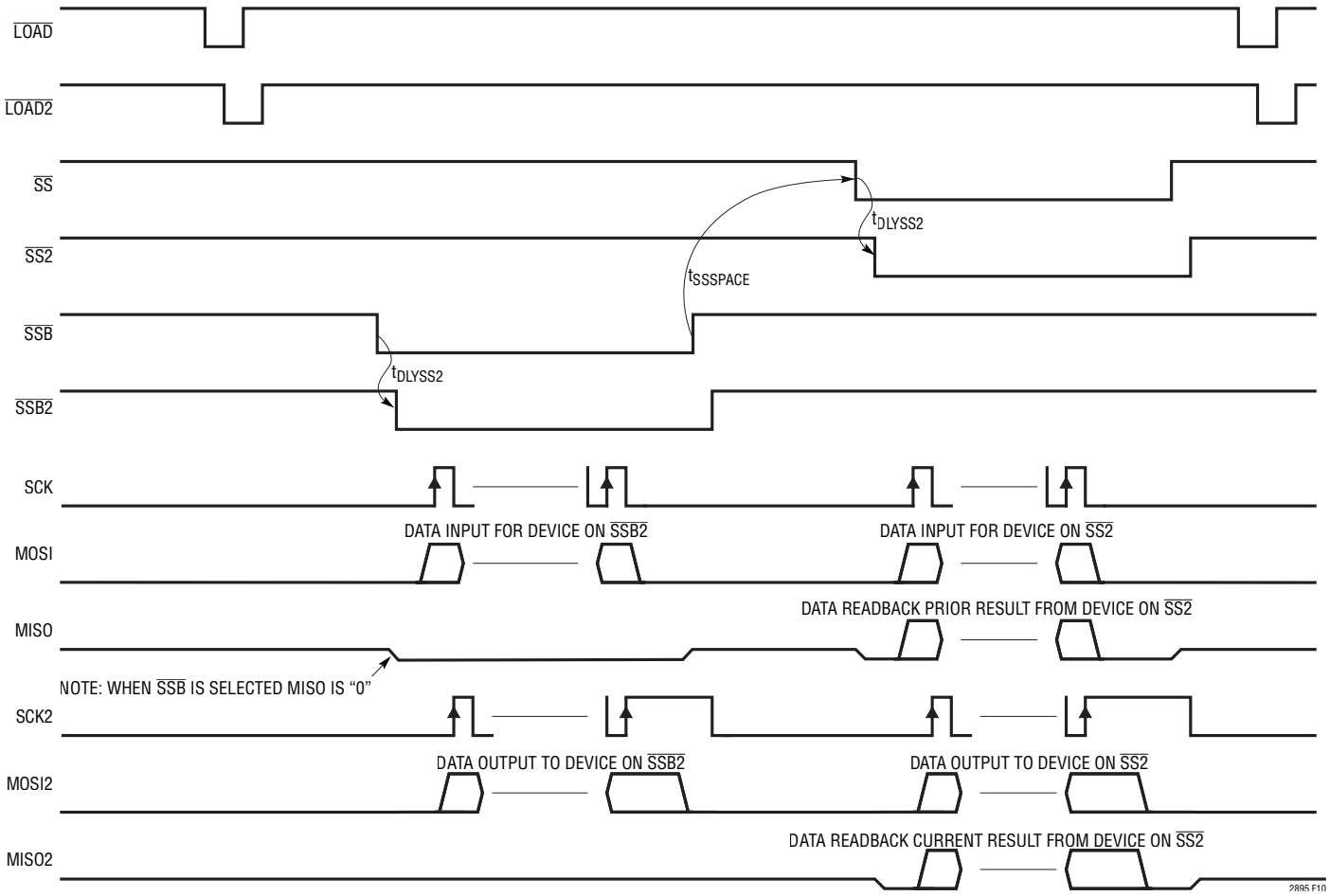


Figure 10. Dual DAC Write

TIMING DIAGRAMS

SA, SB, SC SAFE TRANSITION REGIONS

The select enable signals SA, SB, and SC must be limited in use to transition in a fixed set of safe regions. Transitions within the collision regions may cause data loss or timing loss to important conversion or result information. The intention of these select signals is to control or select functions relative to application settings prior to $\overline{\text{LOAD}}$, $\overline{\text{SS}}$ or $\overline{\text{SSB}}$ chip select commands. Examples are analog multiplexer selections or gain selections to analog circuits on the output of the DAC. Further examples are clear, resets, or power down signals to a DAC or related circuits.

The data direction of SA, SB, and SC may be changed from inputs to outputs. These are independently set with the configuration register.

If the SA2, SB2, or SC2 are configured as inputs, do not change 150ns prior to the $\overline{\text{SS2}}$ or $\overline{\text{SSB2}}$ signal falling. If one of these signals changes in this collision region the SPI process will be corrupted and the $\overline{\text{FAULT}}$ pin is asserted low.

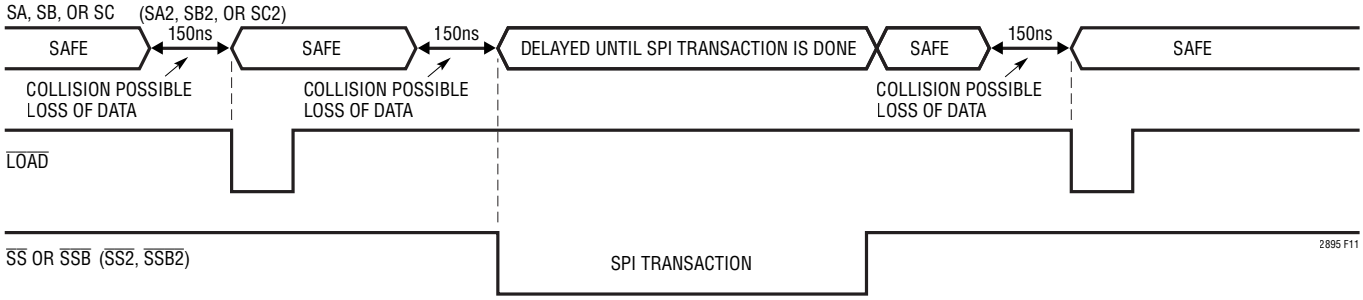


Figure 11. SA, SB, SC Safe Transition Regions

TYPICAL APPLICATION

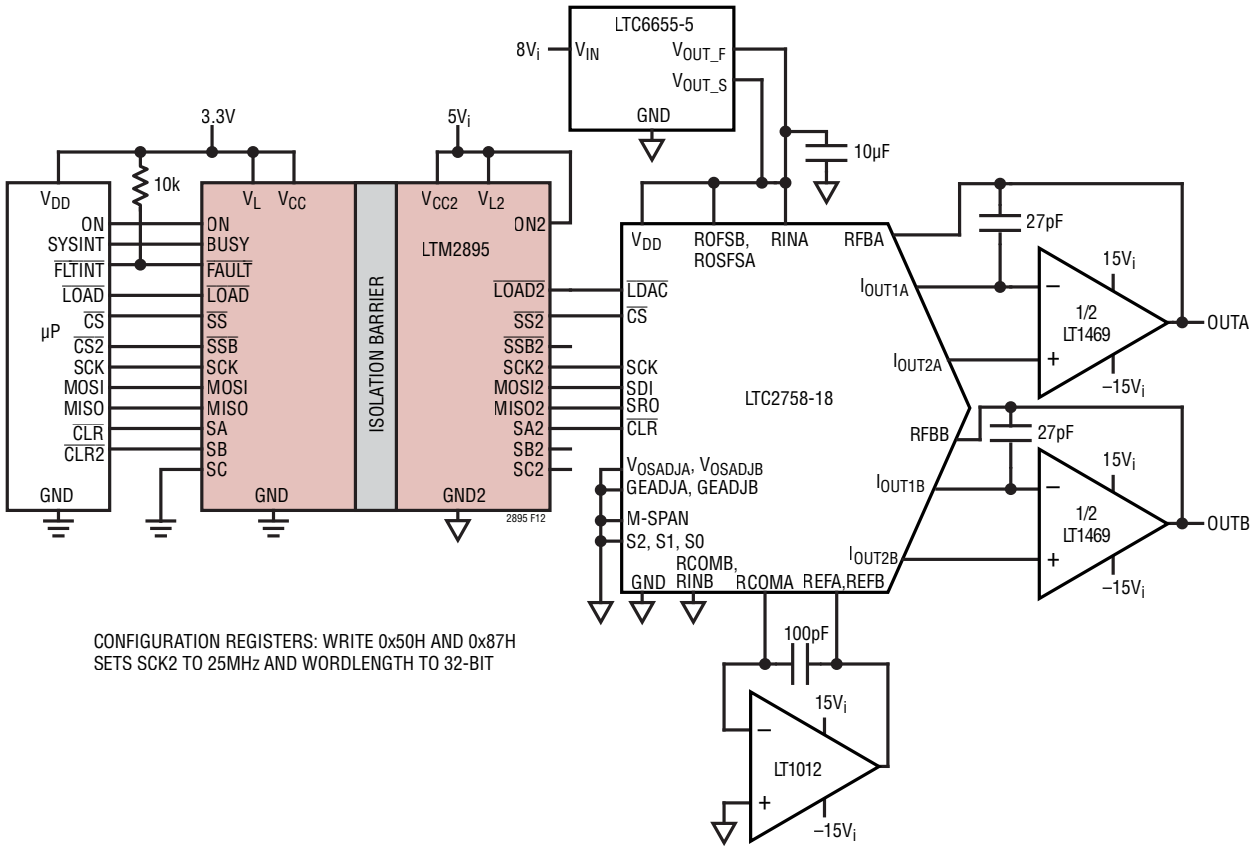


Figure 12. Isolated Dual-Channel 18-Bit DAC with Read Back

TYPICAL APPLICATION

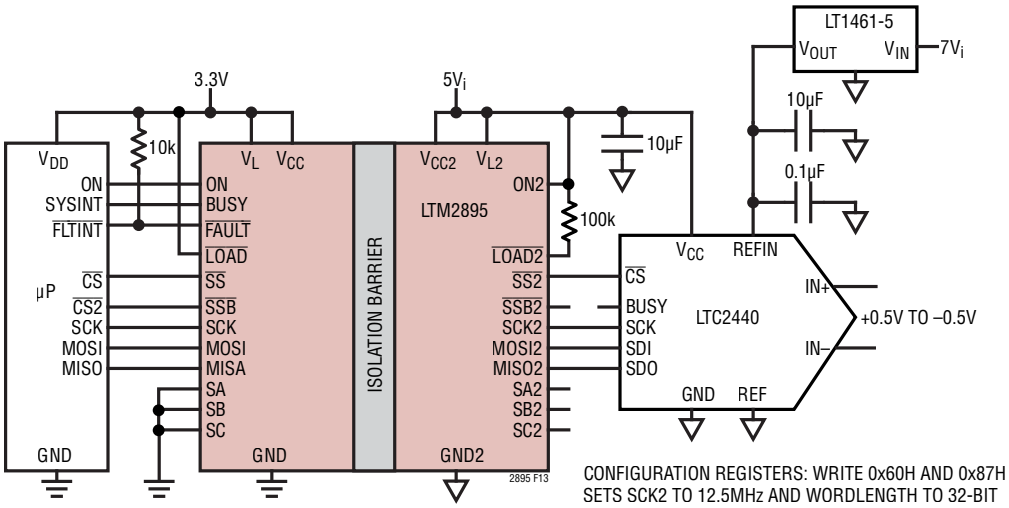


Figure 13. Isolated System Measurement with 24-Bit SDM ADC

TYPICAL APPLICATION

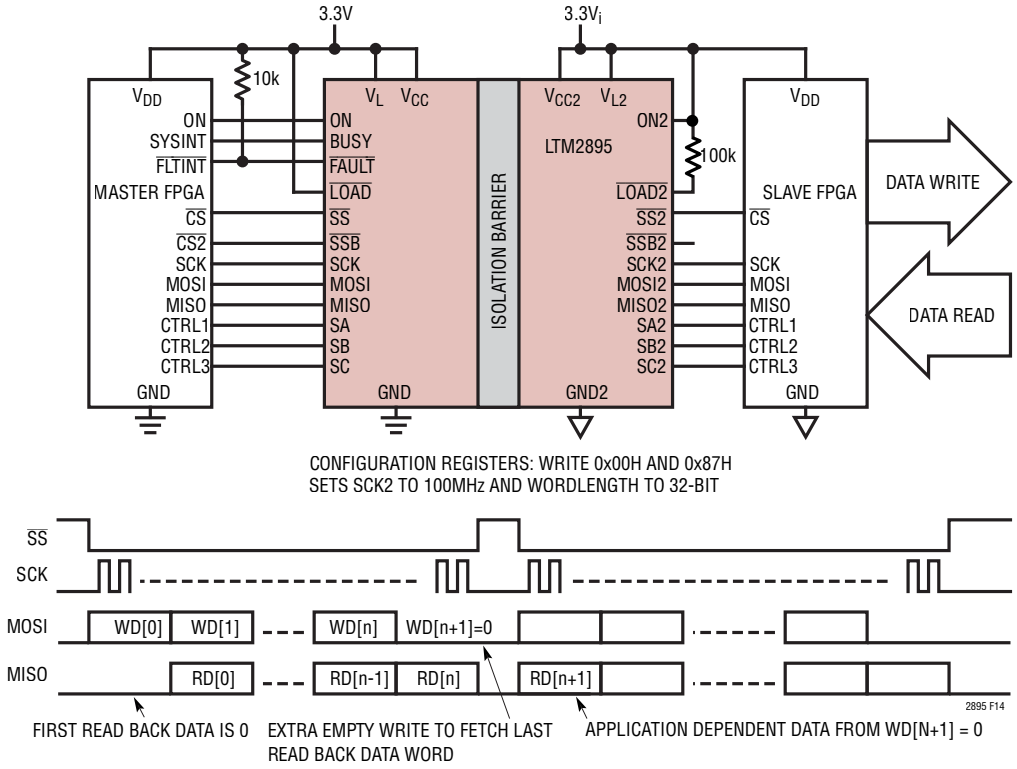
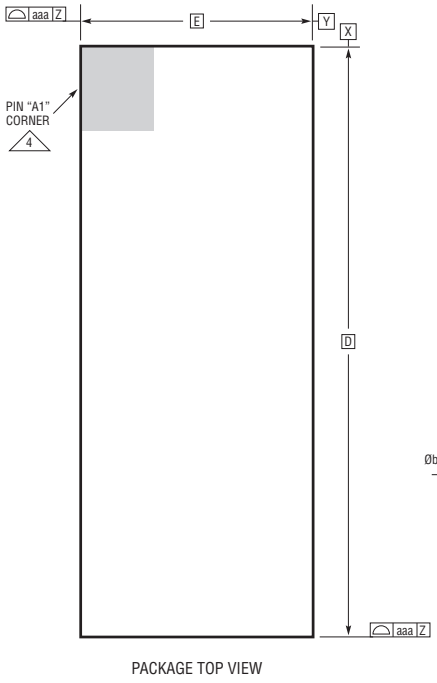


Figure 14. FPGA to Isolated FPGA with Page Mode Data Transfer

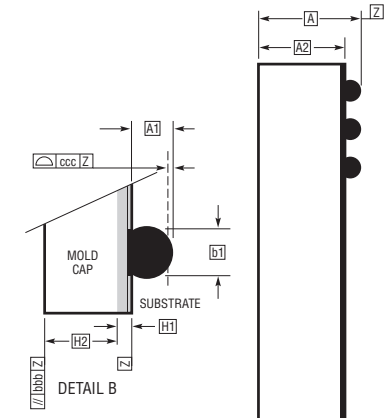
PACKAGE DESCRIPTION

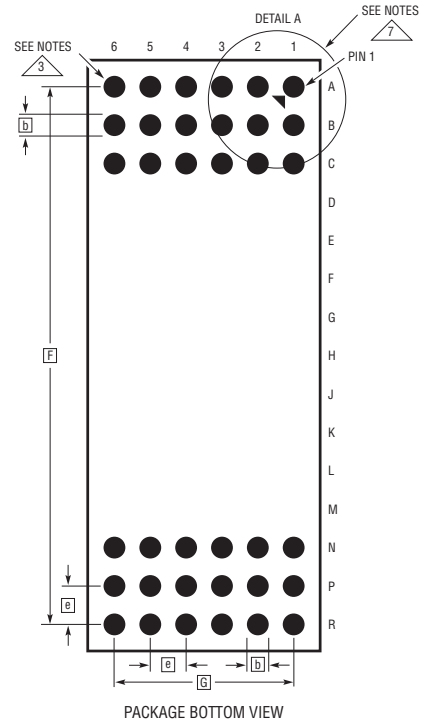
Please refer to http://www.linear.com/product/LTM2895#packaging for the most recent package drawings.

BGA Package
36-Lead (15mm × 6.25mm × 2.06mm)
(Reference LTC DWG# 05-08-1987 Rev Ø)

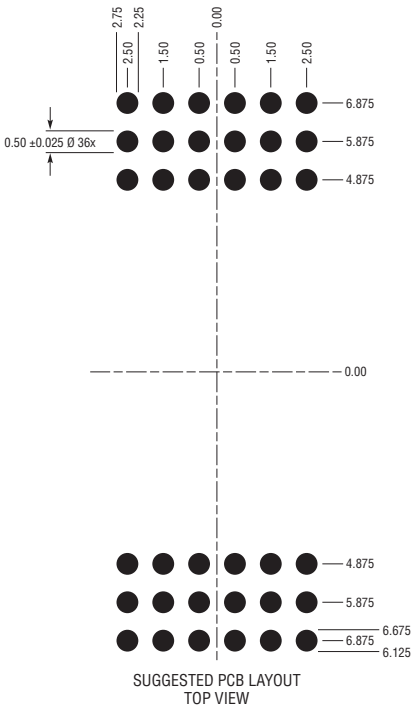


PACKAGE TOP VIEW





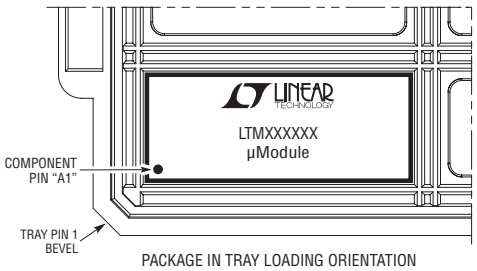
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.86	2.06	2.26	
A1	0.40	0.50	0.60	
A2	1.46	1.56	1.66	
b	0.45	0.60	0.75	
b1	0.47	0.50	0.53	
D		15.00		
E		6.25		
e		1.00		
F		13.75		
G		5.00		
H1	0.51	0.56	0.61	
H2	0.95	1.00	1.05	
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 36				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

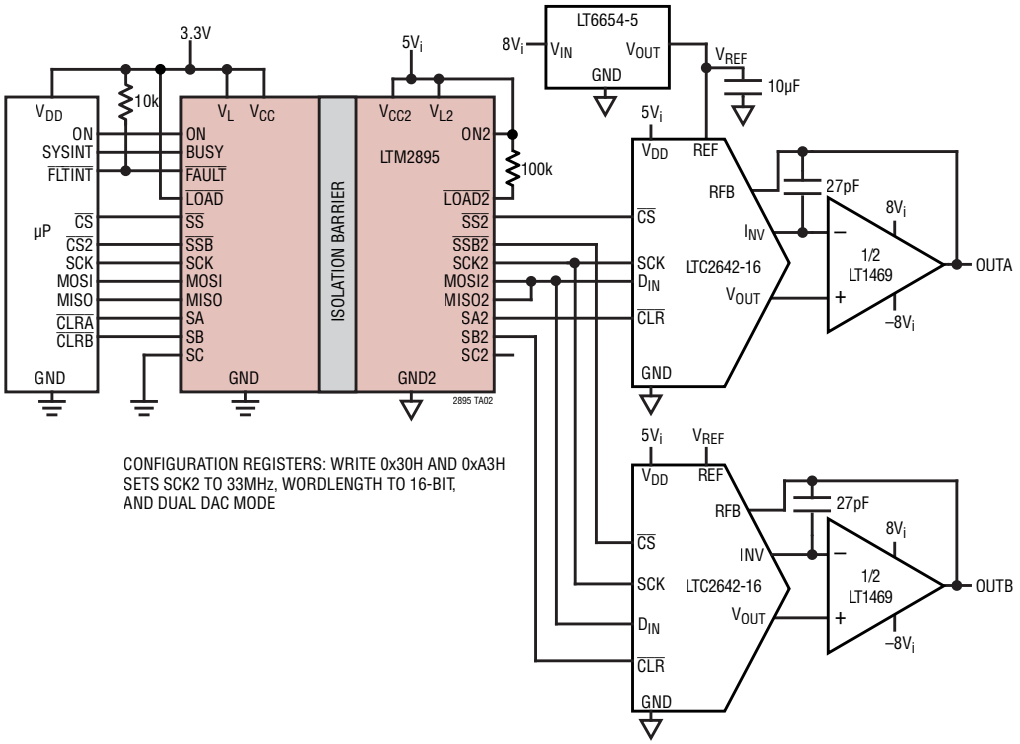


PACKAGE IN TRAY LOADING ORIENTATION

BGA 36 0914 REV Ø

TYPICAL APPLICATION

Dual DAC Circuit



CONFIGURATION REGISTERS: WRITE 0x30H AND 0xA3H
SETS SCK2 TO 33MHz, WORDLENGTH TO 16-BIT,
AND DUAL DAC MODE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2881	Isolated RS485/RS422 µModule Transceiver with Integrated DC/DC Converter	2500V_{RMS} Isolation in Surface Mount BGA or LGA
LTM2882	Dual Isolated RS232 µModule Transceiver with Integrated DC/DC Converter	2500V_{RMS} Isolation in Surface Mount BGA or LGA
LTM2892	SPI/Digital or I^2C Isolated µModule Transceiver	3500V_{RMS} Isolation, 6 Channels
LTM2883	SPI/Digital or I^2C Isolated µModule with Adjustable 5V, and ±12.5V Nominal Voltage Rails	2500V_{RMS} Isolation in Surface Mount BGA
LTM2885	Isolated RS485/RS422 µModule Transceiver	6500V_{RMS} Isolation in Surface Mount BGA
LTM2886	SPI or I^2C µModule Isolator with Adjustable 5V and ±5V Regulated Power	2500V_{RMS} Isolation in Surface Mount BGA
LTM2887	SPI or I^2C µModule Isolator with Dual Adjustable 5V Rails	2500V_{RMS} Isolation in Surface Mount BGA
LTM2889	Complete 4Mbps CAN FD µModule Isolator + Power	2500V_{RMS} Isolation in Surface Mount BGA
LTM2893	Complete 100MHz SPI ADC µModule Isolator	6000V_{RMS} Isolation in Surface Mount BGA
LTM2894	Complete Isolated USB µModule Transceiver	7500V_{RMS} Isolation in Surface Mount BGA
LTM2884	Isolated USB Transceiver with Isolated Power	2500V_{RMS} Isolation in Surface Mount BGA
LTM9100	Isolated Switch Controller with I^2C Command and Telemetry	5000V_{RMS} Isolation in Surface Mount BGA
DACs		
LTC2641-16/ LTC2642-16	16-Bit V_{OUT} DAC in 3mm × 3mm DFN	LTC2641-16/LTC2642-16, Maximum 16-Bit INL Error: ±1LSB Over Temperature
LTC2758-18	Dual Serial 18-Bit SoftSpan™ I_{OUT} DACs	LTC2575-18, Maximum 18-Bit INL Error: ±1LSB Over Temperature

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