High Voltage, Fractional-N/ Integer N PLL Synthesizer

Data Sheet

ADF4152HV

FEATURES

- Fractional-N synthesizer and integer N synthesizer
- High voltage charge pump: V_P = 6.0 V to 30 V
- Radio frequency (RF) bandwidth to 5.0 GHz
- Programmable output divider
- Synthesizer power supply: 3.0 V to 3.6 V
- Programmable dual-modulus prescaler
- Programmable output power level
- Programmable charge pump currents
- RF output mute function
- 3-wire serial interface
- Analog and digital lock detect

APPLICATIONS

- Wireless infrastructure
- Microwave point to point/point to multipoint radios
- Very small aperture terminal (VSAT) radios
- Test equipment
- Private land mobile radios

GENERAL DESCRIPTION

The ADF4152HV is a 5.0 GHz, fractional-N or integer N frequency synthesizer with an integrated high voltage charge pump. The synthesizer can drive external wideband voltage controlled oscillators (VCOs) directly, eliminating the need for operational amplifiers to achieve higher tuning voltages. The integrated high voltage charge pump simplifies design and reduces cost while improving phase noise, in contrast to active filter topologies, which tend to degrade phase noise compared to passive filter topologies.

The VCO frequency can be divided by 1, 2, 4, 8, or 16 to allow the user to generate RF output frequencies as low as 31.25 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin and software controllable.

A simple 3-wire interface controls all on-chip registers. The charge pump operates from a power supply ranging from 6.0 V to 30 V, whereas the rest of the device operates from 3.0 V to 3.6 V. The ADF4152HV can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

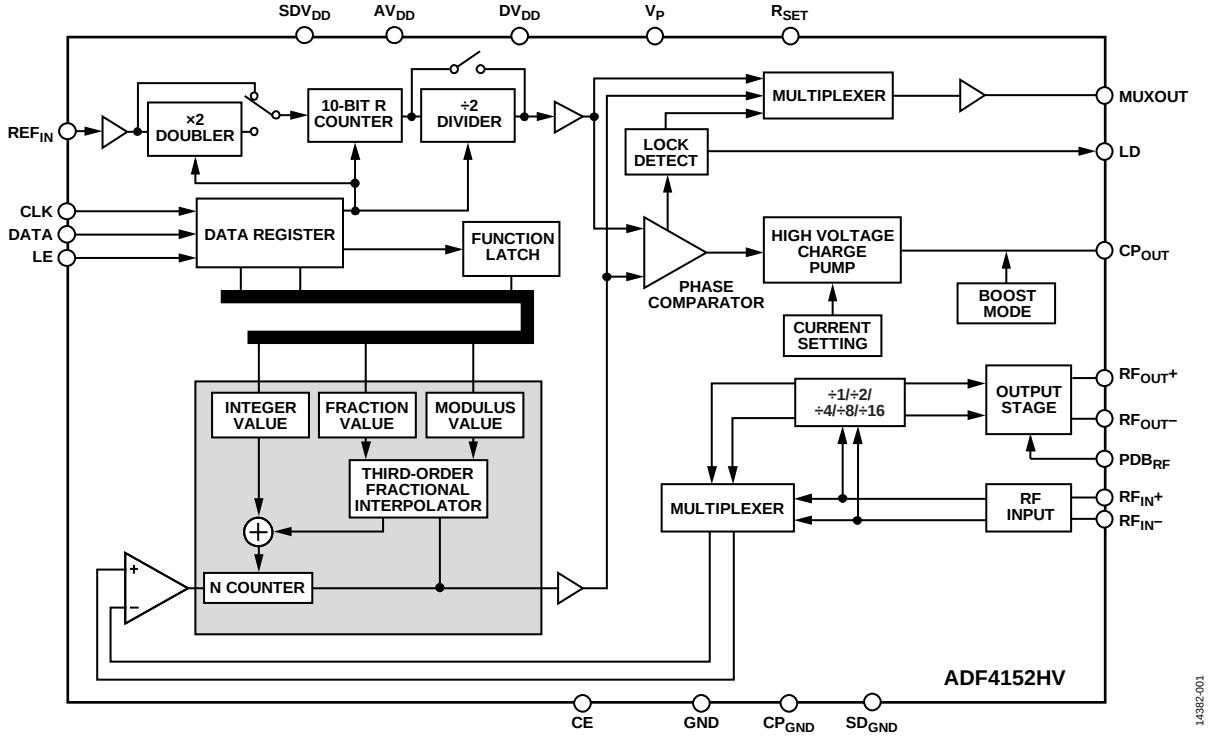

Figure 1.

Rev. 0 Document Feedback

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- ADF4152HV Evaluation Board

DOCUMENTATION

Data Sheet

- ADF4152HV: High Voltage, Fractional-N/Integer N PLL Synthesizer Data Sheet

User Guides

- UG-963: Evaluating the ADF4152HV PLL Frequency Synthesizer

DESIGN RESOURCES

- ADF4152HV Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

7/2016—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = SDV_{DD} = 3.3 V ± 10%; V_P = 6.0 V to 30 V; GND = 0 V; operating temperature range is T_A = −40°C to +85°C, unless otherwise noted. V_{CP} is the voltage at the CP_{OUT} pin.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_{IN} CHARACTERISTICS					
Input Frequency	10		300	MHz	For f < 10 MHz, ensure slew rate > 21 V/µs
	10		30	MHz	Reference doubler enabled (DB25 bit in Register 2 is set to 1)
Input Sensitivity	0.7		AV_{DD}	V p-p	Biased at AV_{DD}/2; ac coupling ensures AV_{DD}/2 bias
Input Capacitance			5.0	pF	
Input Current			±60	µA	
RF INPUT CHARACTERISTICS					For lower RF_{IN}± frequencies, ensure slew rate > 400 V/µs
RF Input Frequency (RF_{IN}±)					
RF Output Buffer Disabled	0.5		4.0	GHz	−10 dBm ≤ RF input power ≤ +5 dBm
	0.5		5.0	GHz	−5 dBm ≤ RF input power ≤ +5 dBm
RF Output Buffer Enabled	0.5		3.5	GHz	−10 dBm ≤ RF input power ≤ +5 dBm
RF Output Buffer and Dividers Enabled	0.5		3.0	GHz	−10 dBm ≤ RF input power ≤ +5 dBm
Prescaler Output Frequency			750	MHz	
PHASE DETECTOR					
Phase Detector Frequency			26	MHz	Low noise mode
			20	MHz	Low spur mode
			26	MHz	Integer N mode
HIGH VOLTAGE CHARGE PUMP					
Charge Pump Current, I_{CP}					
Sink/Source					
High Value		384		µA	R_{SET} = 5.1 kΩ
Low Value		48		µA	R_{SET} = 5.1 kΩ
High Value vs. R_{SET}	196			µA	R_{SET} = 10 kΩ
			594	µA	R_{SET} = 3.3 kΩ
R_{SET} Range	3.3		10	kΩ	
Sink and Source Current Matching		6		%	1.0 V ≤ V_{CP} ≤ (V_P − 1.0 V); V_P = 6 V to 30 V
Absolute I_{CP} Accuracy		3		%	
I_{CP} vs. V_{CP}		2.5		%	1.0 V ≤ V_{CP} ≤ (V_P − 1.0 V)
I_{CP} vs. Temperature		2.5		%	V_{CP} = V_P/2
I_{CP} Leakage		2.5		nA	V_{CP} = V_P/2
LOGIC INPUTS					
Input Voltage					
High, V_{INH}	2.0			V	
Low, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			15.0	pF	
LOGIC OUTPUTS					
Output Voltage					
High, V_{OH}	DV_{DD} − 0.4			V	CMOS output selected
Low, V_{OL}			0.4	V	I_{OL} = 500 µA
Output High Current, I_{OH}			500	µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES					
AV_{DD}	3.0		3.6	V	
DV_{DD}, SDV_{DD}		AV_{DD}		V	
V_P	6.0		30	V	Set the V_P supply at least 1 V above the maximum desired tuning voltage
I_P		1	2.5	mA	V_P = 30 V
$I_{DVDD} + I_{SDVDD} + I_{AVDD}$ [1]		50	60	mA	
Current per Output Divider		6 to 24		mA	Each output divide by 2 consumes 6 mA typical
I_{RFOUT} [2]		20	32	mA	RF output stage is programmable
Low Power Sleep Mode		1		μA	
RF OUTPUT CHARACTERISTICS					
Output Frequency Using RF Output Dividers	31.25			MHz	500 MHz VCO input and divide by 16 selected
Second-Order Harmonic Distortion		−19		dBc	Fundamental VCO output
		−20		dBc	Divided VCO output
Third-Order Harmonic Distortion		−13		dBc	Fundamental VCO output
		−10		dBc	Divided VCO output
Minimum RF Output Power(RF_{OUT}±) [2]		−4		dBm	Programmable in 3 dB steps
Maximum RF Output Power(RF_{OUT}±) [2]		5		dBm	Programmable in 3 dB steps
Output Power Variation vs. Supply		±1		dB	Pull-up supply on Pin 18 and Pin 19 varied from 3.0 V to 3.6 V
Output Power Variation vs. Temperature		±1		dB	From −40°C to +85°C
Level of Signal with RF Mute Enabled		−37		dBm	PDB_{RF} pin brought low; RF_{OUT}± = 2 GHz
NOISE CHARACTERISTICS					
Normalized In-Band Phase Noise Floor (PN_{SYNTH}) [3]		−213		dBc/Hz	Low noise mode
		−203		dBc/Hz	Low spur mode
Normalized 1/f Phase Noise (PN_{1_f}) [4]		−113		dBc/Hz	Low noise mode
		−108		dBc/Hz	Low spur mode
RF Output Divider Noise Floor		−155		dBc/Hz	Measured at 10 MHz offset
Spurious Signals Due to Phase Frequency Detector (PFD) Frequency		−70		dBc	At RF_{OUT}+/RF_{OUT}− pins
		−85		dBc	At VCO output

[1] T_A = 25°C; AV_{DD} = DV_{DD} = 3.3 V; prescaler = 8/9; f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; f_{RF} = 1.75 GHz.
[2] Using 50 Ω resistors to AV_{DD}, into a 50 Ω load.
[3] This figure can be used to calculate phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula:
$PN_{SYNTH} = PN_{TOT} - 10\log(f_{PFD}) - 20\log N$
where PN_{TOT} is the measured in-band phase noise at the VCO output.
[4] The PLL phase noise is composed of flicker (1/f) noise plus the normalized PLL noise floor. The flicker noise is specified at a 10 kHz offset and normalized to 1 GHz. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by $PN = PN_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = SDV_{DD} = 3.3 V ± 10%; V_P = 6.0 V to 30 V; GND = 0 V; operating temperature range is T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Limit	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

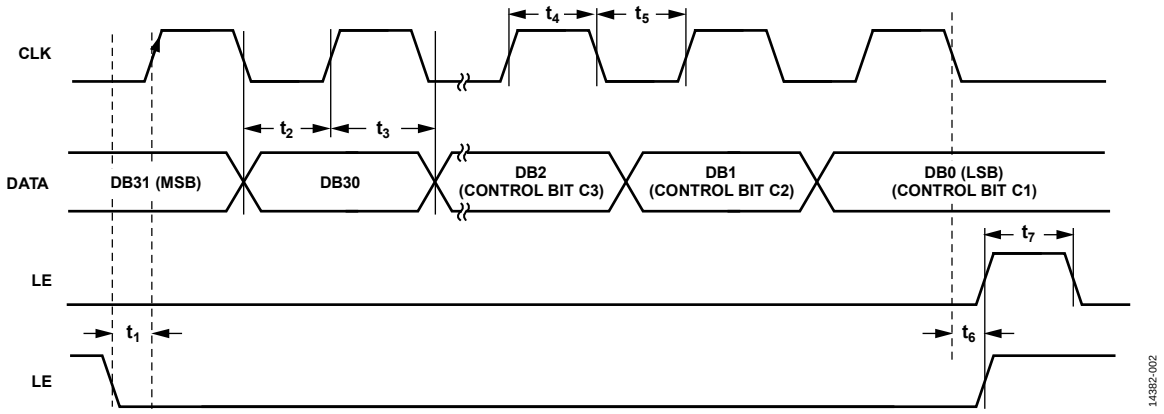

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.9 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND[1]	−0.3 V to +33 V
Digital Input/Output (I/O) Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to DV_{DD} + 0.3 V
REF_{IN} to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = CP_{GND} = SD_{GND} = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRANSISTOR COUNT

The transistor count for the ADF4152HV is 23,380 (CMOS) and 809 (bipolar).

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-32-11	27.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

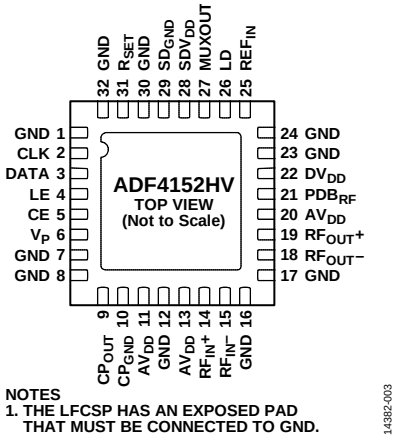

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 8, 12, 16, 17, 23, 24, 30, 32	GND	Ground. Tie all ground pins together.
2	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
3	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
4	LE	Load Enable. When LE goes high, the data stored in the 32-bit shift register is loaded into the register that is selected by the three control bits. This input is a high impedance CMOS input.
5	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device.
6	V_P	High Voltage Charge Pump Power Supply. Place decoupling capacitors to the ground plane as close to this pin as possible. The decoupling capacitors must have the appropriate voltage rating (a value of 10 µF is recommended). Take care to ensure that V_P does not exceed the absolute maximum ratings on power-up (see Table 3). A 10 Ω series resistor can significantly reduce voltage overshoot with minimal voltage drop.
9	CP_{OUT}	High Voltage Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external passive loop filter. The output of the loop filter is connected to the voltage tuning port of the external VCO.
10	CP_{GND}	High Voltage Charge Pump Ground. Tie all ground pins together.
11, 13, 20	AV_{DD}	Analog Power Supply. This pin ranges from 3.0 V to 3.6 V. Place decoupling capacitors to the ground plane as close to this pin as possible. AV_{DD} must have the same value as DV_{DD}.
14	RF_{IN}+	Positive RF Input. The output of the VCO or external prescaler must be ac-coupled to this pin.
15	RF_{IN}–	Complementary RF Input. If a single-ended input is required, this pin can be tied to ground via a 100 pF capacitor.
18	RF_{OUT}–	Divided Down Output of RF_{IN}–. This pin can be left unconnected if the divider functionality is not required.
19	RF_{OUT}+	Divided Down Output of RF_{IN}+. This pin can be left unconnected if the divider functionality is not required.
21	PDB_{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This function is also software controllable.
22	DV_{DD}	Digital Power Supply. Place decoupling capacitors to the ground plane as close to this pin as possible. DV_{DD} must have the same value as AV_{DD}.
25	REF_{IN}	Reference Input. This CMOS input has a nominal threshold of $AV_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. This input can be driven from a thermally compensated crystal oscillator (TCXO) or other reference.
26	LD	Lock Detect Output. A logic high output on this pin indicates a phase-locked loop (PLL) lock. A logic low output indicates loss of PLL lock.

Pin No.	Mnemonic	Description
27	MUXOUT	Multiplexer Output. The multiplexer output allows the lock detect, the N divider value, or the R counter value to be accessed externally.
28	SDV_{DD}	Digital Σ-Δ Modulator Power Supply. Place decoupling capacitors to the ground plane as close to this pin as possible. SDV_{DD} must have the same value as AV_{DD}.
29	SD_{GND}	Digital Σ-Δ Modulator Ground. Tie all ground pins together.
31	R_{SET}	Bias Current Resistor. Connecting a resistor between this pin and GND sets the charge pump output current. Place the resistor as close to this pin as possible. The nominal voltage bias at the R_{SET} pin is 0.55 V. The relationship between I_{CP} and R_{SET} is as follows: $I_{CP} = 1.96/R_{SET}$ where: R_{SET} = 5.1 kΩ. I_{CP} = 384 μA.
EP	Exposed Pad	Exposed Pad. The LFCSP has an exposed pad that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

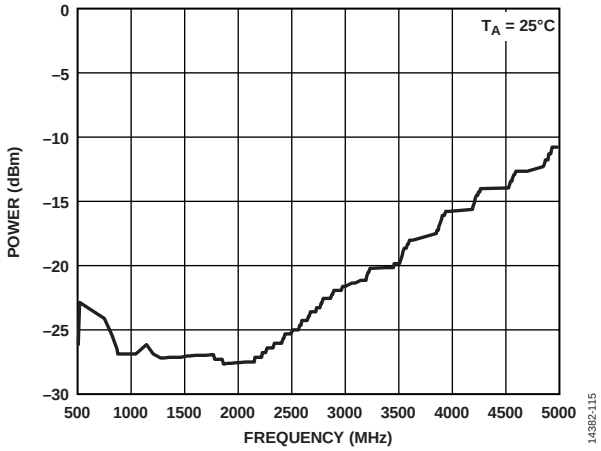

Figure 4. RF Input Sensitivity, RF Output Disabled

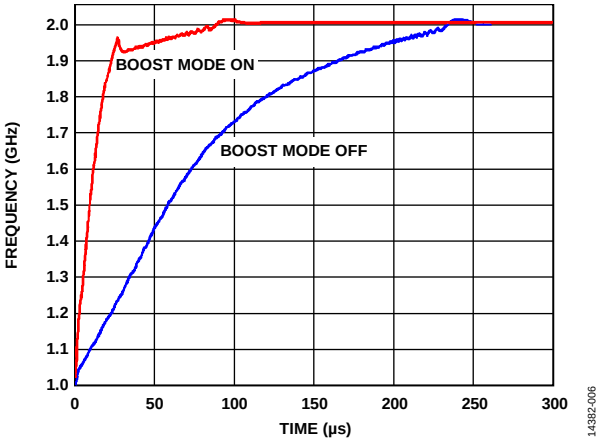

Figure 7. PLL Lock Time with Boost Mode On and Off; Locking over Octave Range Jump (1 GHz to 2 GHz) for PFD = 20 MHz, Loop Bandwidth = 100 kHz, I_{CP} = 300 µA, V_P = 28 V, AV_{DD} = DV_{DD} = SDV_{DD} = 3.3 V, REF_{IN} = 100 MHz

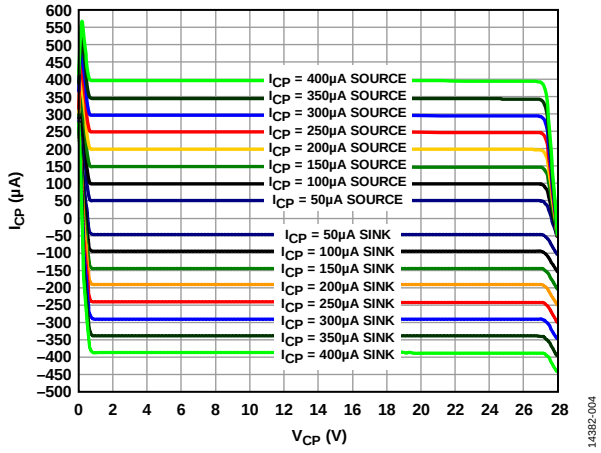

Figure 5. Charge Pump Output Characteristics, V_P = 28 V, I_{CP} Varied from 50 µA to 400 µA, R_{SET} = 5.1 kΩ

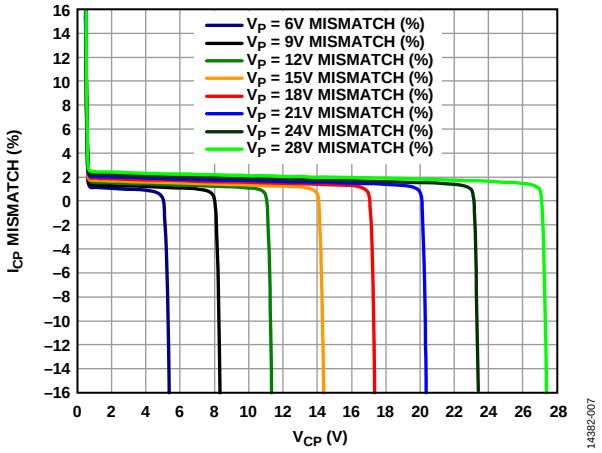

Figure 8. Charge Pump Output (I_{CP}) Mismatch vs. V_{CP}, I_{CP} = 200 µA

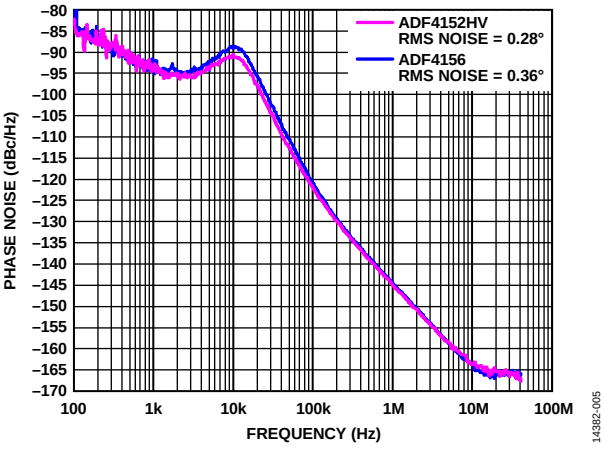

Figure 6. Active Filter Phase Noise, ADF4152HV vs. ADF4156; Active Filter Implemented Using OP27 Op Amp; PFD = 20 MHz, Loop Bandwidth = 10 kHz, I_{CP} = 300 µA, Carrier Frequency = 1.7 GHz, V_P = 28 V

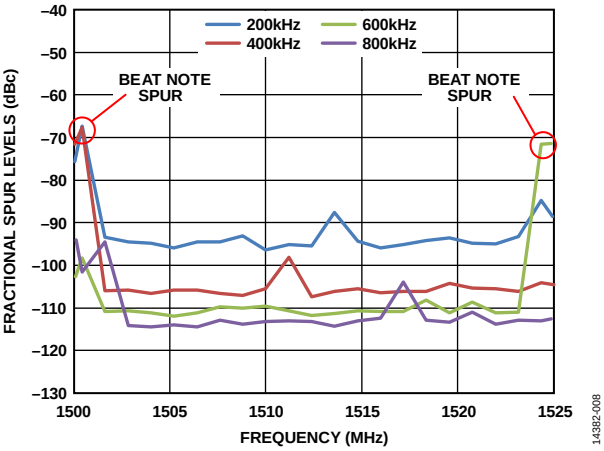

Figure 9. Fractional Spur Levels vs. Frequency, Low Spur Mode; Measured at VCO Output, PFD = 25 MHz, MOD = 125

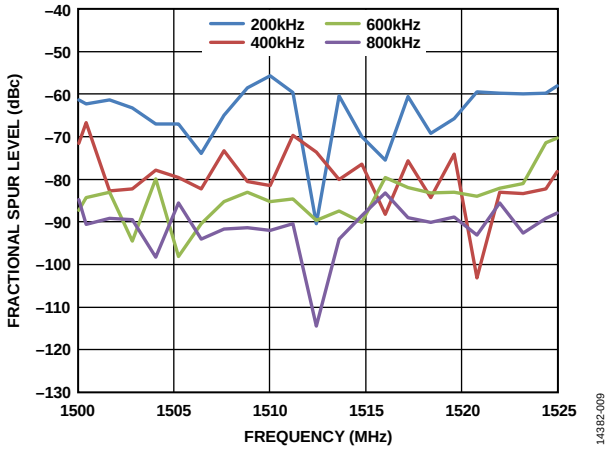

Figure 10. Fractional Spur Levels vs. Frequency, Low Noise Mode; Measured at VCO Output, PFD = 25 MHz, MOD = 125

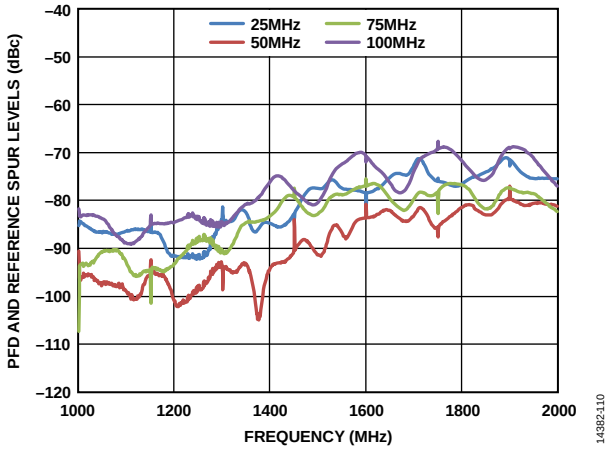

Figure 11. PFD and Reference Spur Levels vs. Frequency, Measured at VCO Output, REF_{IN} = 100 MHz, PFD = 25 MHz

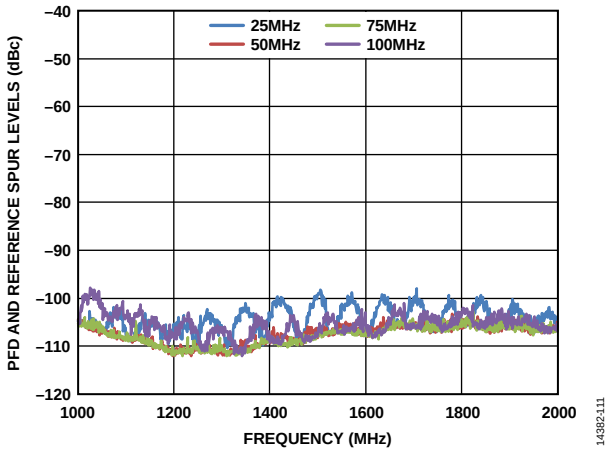

Figure 12. PFD and Reference Spur Levels vs. Frequency, Measured at VCO Output with ADL5541 Buffer Placed Between VCO Output and RF Input, REF_{IN} = 100 MHz, PFD = 25 MHz

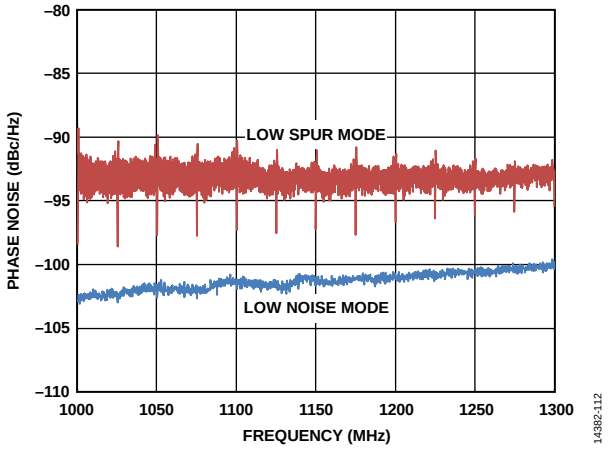

Figure 13. In-Band Phase Noise Measured at 3 kHz Offset for Low Noise Mode and Low Spur Mode, PFD = 25 MHz, PLL Loop Bandwidth = 40 kHz

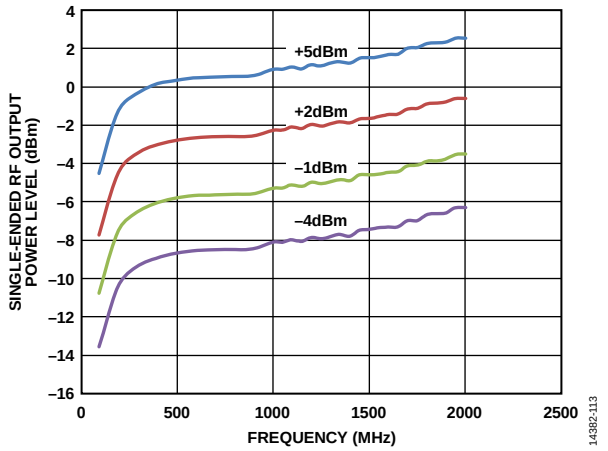

Figure 14. Single-Ended RF Output Power Level vs. Frequency over Various Power Settings, RF Output Pins Pulled Up to 3.3 V via 27 nH||50 Ω

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 15. The SW1 and SW2 switches are normally closed. The SW3 switch is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. In this way, no loading of the REF_{IN} pin occurs during power-down.

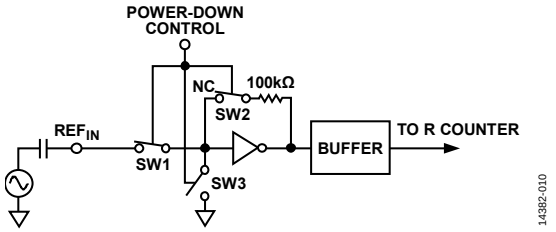

Figure 15. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. This divider comprises the INT, FRAC, and MOD values, which determine the division ratio (see Figure 16).

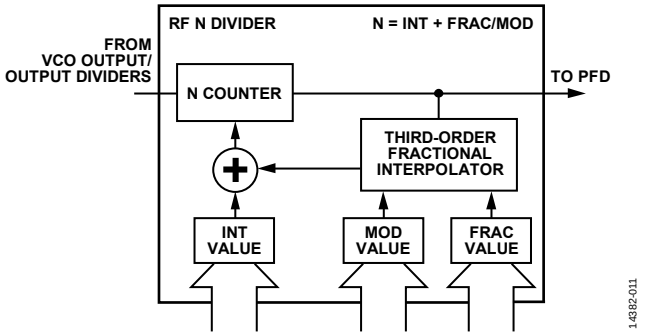

Figure 16. RF N Divider

INT, FRAC, MOD, and R Counter Relationship

The INT, FRAC, and MOD values, in conjunction with the R counter, enable the user to generate output frequencies that are spaced by fractions of the PFD frequency. For more information, see the RF Synthesizer—A Worked Example section.

The RF VCO frequency (RF_{OUT}) is calculated as follows:

$$RF_{OUT} = (f_{PFD}/RF\ Divider) \times (INT + (FRAC/MOD)) \quad (1)$$

where:
RF_{OUT} is the output frequency of the external VCO.
f_{PFD} is the PFD frequency.
RF Divider is the output divider that divides down the VCO frequency.
INT is the preset divide ratio of the binary 16-bit counter (23 to 32,767 for the 4/5 prescaler, 75 to 65,535 for the 8/9 prescaler).
FRAC is the numerator of the fractional division (0 to MOD − 1).
MOD is the preset fractional modulus (2 to 4095).

The PFD frequency (f_{PFD}) equation is

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the reference doubler bit, DB25 in Register 2.
R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023), DB14 to DB23 in Register 2.
T is the reference divide by 2 bit (0 or 1), DB24 in Register 2.

Integer N Mode

If FRAC = 0 and the DB8 (LDF) bit in Register 2 is set to 1, the synthesizer operates in integer-N mode. Set the DB8 bit in Register 2 to 1 for integer N digital lock detect.

R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PFD AND HIGH VOLTAGE CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 17 is a simplified schematic of the PFD.

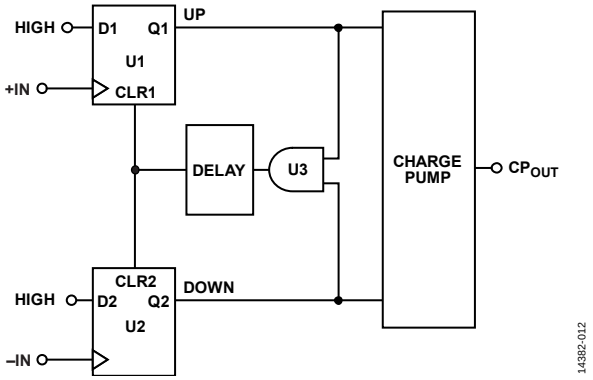

Figure 17. PFD Simplified Schematic

The PFD includes a delay element that sets the width of the antibacklash pulse to 4.2 ns. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level.

The high voltage charge pump is designed on an Analog Devices, Inc., proprietary high voltage process and allows the charge pump to output voltages as high as 29 V when powered by a 30 V supply. The high voltage charge pump removes the need for active filtering when interfacing to a high voltage VCO.

MUXOUT AND LOCK DETECT

The multiplexer output on the ADF4152HV allows the user to access various internal points on the chip. The state of the MUXOUT pin is controlled by the M3, M2, and M1 bits in Register 2 (see Figure 23). Figure 18 shows the MUXOUT section in block diagram form.

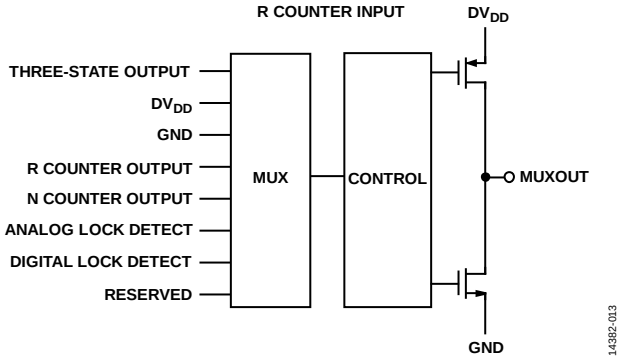

Figure 18. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4152HV digital section includes a 10-bit RF R counter, a 16-bit RF N counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of six latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. As shown in Figure 2, the control bits are the three LSBs: DB2, DB1, and DB0. The truth table for these bits is shown in Table 6. Figure 20 summarizes how the latches are programmed.

Table 6. Truth Table for C3, C2, and C1 Control Bits

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register 0 (R0)
0	0	1	Register 1 (R1)
0	1	0	Register 2 (R2)
0	1	1	Register 3 (R3)
1	0	0	Register 4 (R4)
1	0	1	Register 5 (R5)

PROGRAM MODES

Table 6 and Figure 20 through Figure 26 show how the program modes are set up in the ADF4152HV.

The following settings in the ADF4152HV are double buffered: phase value, modulus value, reference doubler, reference divide by 2, R counter value, and charge pump current setting. Before the device uses a new value for any double-buffered setting, the following two events must occur:

1. Write the appropriate register to latch the new value into the device.
2. Perform a new write on Register 0 (R0).

For example, to ensure that the modulus value is loaded correctly any time that the modulus value is updated, Register 0 (R0) must be written to. The divider select value in Register 4 (R4) is also double buffered, but only when the DB13 bit of Register 2 (R2) is high.

OUTPUT STAGE

The RF_{OUT}+ and RF_{OUT}− pins of the ADF4152HV are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 19. To allow the user to optimize the power dissipation vs. output power requirements, the tail current of the differential pair is programmable using Bits[DB4:DB3] in Register 4 (R4). Four current levels can be set. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respective of RF_{OUT}±, using a 50 Ω resistor to AV_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section). If the outputs are used individually, the optimum output stage consists of a shunt inductor to AV_{DD}.

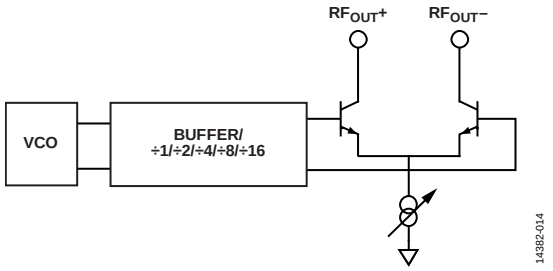

Figure 19. Output Stage

Another feature of the ADF4152HV is that the supply current to the RF output stage can be shut down until the device achieves lock, as measured by the digital lock detect circuitry. This feature is enabled by the mute till lock detect (MTLD) bit in Register 4 (R4).

REGISTER MAPS

REGISTER 0

RESERVED	16-BIT INTEGER VALUE (INT)																12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				PRESCALER	12-BIT PHASE VALUE (PHASE) DBR[1]												12-BIT MODULUS VALUE (MOD) DBR[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	PR1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED	LOW NOISE AND LOW SPUR MODES		MUXOUT			REFERENCE DOUBLER DBR[1]	DBR[1] RDIV2	10-BIT R COUNTER DBR[1]									DOUBLE BUFFER	RESERVED	DBR[1] CHARGE PUMP CURRENT SETTING			LDF	LDP	RESERVED	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	0	CP3	CP2	CP1	U6	U5	1	U3	U2	U1	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED													BOOST EN	RESERVED	CLOCK DIVIDER MODE		12-BIT CLOCK DIVIDER VALUE											CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	B1	0	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED								FEEDBACK SELECT	DBB[2] DIVIDER SELECT			RESERVED									MTLD	RESERVED				RF OUTPUT ENABLE	OUTPUT POWER		CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D13	D12	D11	D10	0	0	0	0	0	0	0	0	0	D8	0	0	0	0	D3	D2	D1	C3(1)	C2(0)	C1(0)

REGISTER 5

ABP WIDTH	CC ENABLE	RESERVED	RESERVED					LD PIN MODE	RESERVED																				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ABP2	ABP1	CE1	1	0	0	0	0	D15	D14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(0)	C1(1)

[1]DBR = DOUBLE-BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE-BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0, ONLY WHEN DB13 OF REGISTER 2 IS HIGH.

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Figure 20. Register Summary

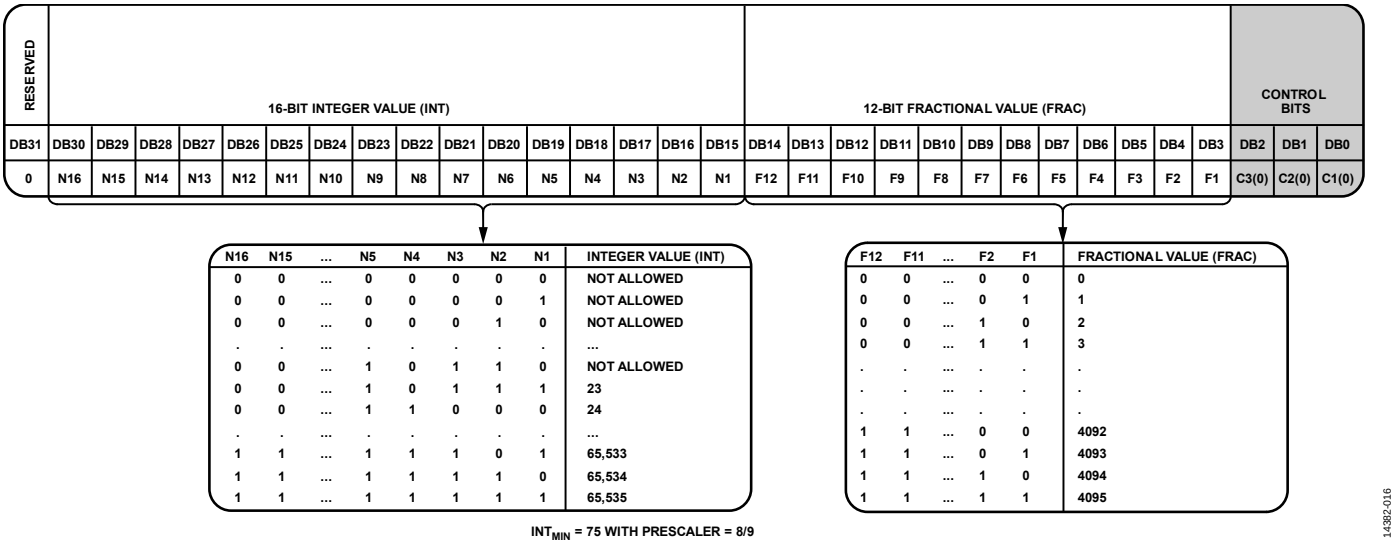


Figure 21. Register 0 (R0)

REGISTER 0

Control Bits

When Bits[C3:C1] are set to 000, Register 0 is programmed. Figure 21 shows the input data format for programming this register.

16-Bit Integer Value (INT)

The 16 INT bits (Bits[DB30:DB15]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 1 (see the INT, FRAC, MOD, and R Counter Relationship section). Integer values from 23 to 32,767 are allowed for the 4/5 prescaler; for the 8/9 prescaler, the minimum integer value is 75 and the maximum value is 65,535.

12-Bit Fractional Value (FRAC)

The 12 FRAC bits (Bits[DB14:DB3]) set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC values from 0 to (MOD − 1) cover channels over a frequency range equal to the PFD reference frequency.

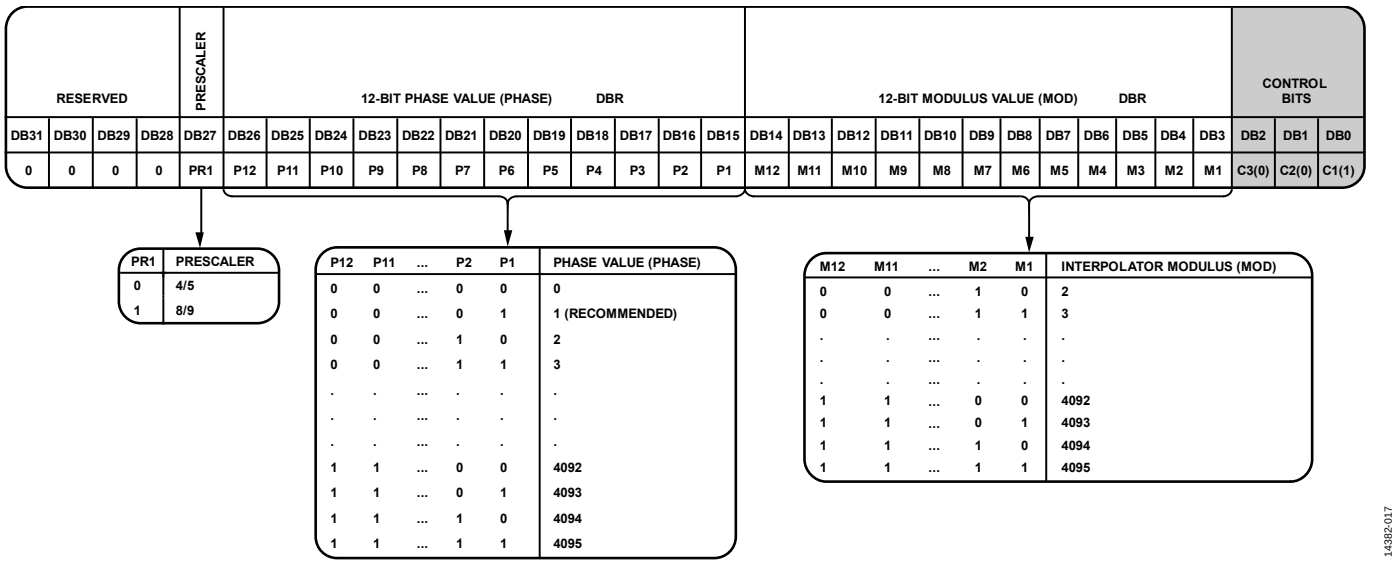


Figure 22. Register 1 (R1)

REGISTER 1

Control Bits

When Bits[C3:C1] are set to 001, Register 1 is programmed. Figure 22 shows the input data format for programming this register.

Prescaler Value

The dual-modulus prescaler, along with the INT, FRAC, and MOD values, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (DB27) in Register 1 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. The prescaler is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4152HV above 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value as follows:

- Prescaler = 4/5: N_{MIN} = 23, where N_{MIN} is the minimum INT value
- Prescaler = 8/9: N_{MIN} = 75

12-Bit Phase Value

Bits[DB26:DB15] control the phase value. The word must be less than the MOD value programmed in Register 1. The phase word programs the RF output phase from 0° to 360° with a resolution of 360°/MOD. For more information, see the Phase Resync section.

In most applications, the phase relationship between the RF signal and the reference is not important. In such applications, the phase value can be used to optimize the fractional and subfractional spur levels. For more information, see the Spur Consistency and Fractional Spur Optimization section.

If neither the phase resync nor the spurious optimization function is used, it is recommended that the phase word be set to 1.

12-Bit Modulus Value (MOD)

The 12 MOD bits (Bits[DB14:DB3]) set the fractional modulus. The fractional modulus is the ratio of the PFD frequency to the channel step resolution on the RF output. For more information, see the 12-Bit Programmable Modulus section.

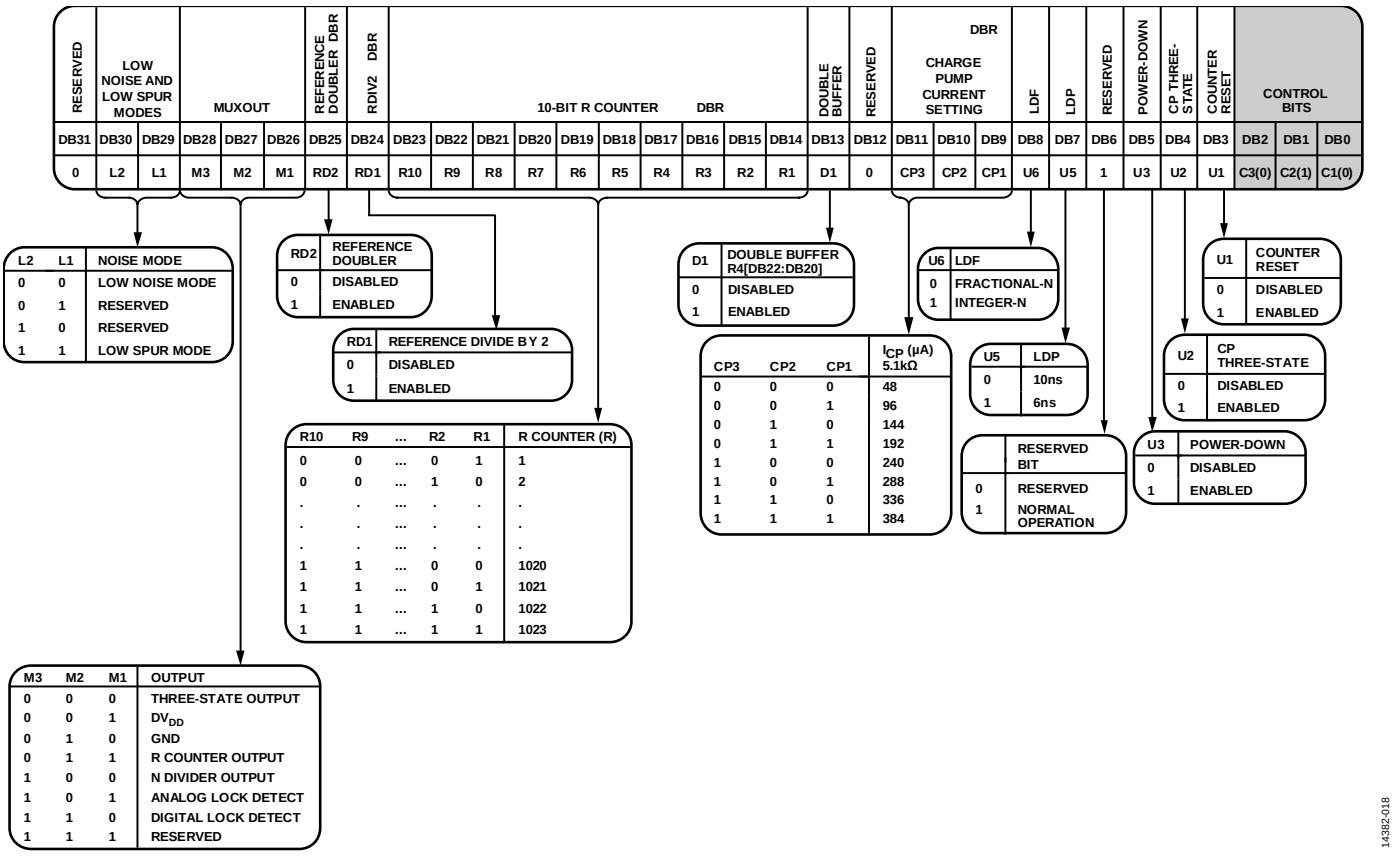


Figure 23. Register 2 (R2)

REGISTER 2

Control Bits

When Bits[C3:C1] are set to 010, Register 2 is programmed. Figure 23 shows the input data format for programming this register.

Low Noise and Low Spur Modes

The noise modes on the ADF4152HV are controlled by setting Bits[DB30:DB29] in Register 2 (see Figure 23). The noise modes allow the user to optimize a design either for improved spurious performance or for improved phase noise performance.

When the low spur mode is chosen, dither is enabled. Dither randomizes the fractional quantization noise so that it resembles white noise rather than spurious noise. As a result, the device is optimized for improved spurious performance. Low spur mode is normally used for fastlocking applications when the PLL closed-loop bandwidth is wide. Wide loop bandwidth is a loop bandwidth greater than 1/10 of the RF VCO frequency, RF_{OUT}. A wide loop filter does not attenuate the spurs to the same level as a narrow loop bandwidth.

For the best noise performance, use the low noise mode option. When the low noise mode is chosen, dither is disabled. This mode ensures that the charge pump operates in an optimum region for noise performance. Low noise mode is extremely useful when a narrow loop filter bandwidth is available. The synthesizer ensures extremely low noise, and the filter attenuates the spurs.

Figure 9 and Figure 10 show fractional spur levels when using low spur mode and low noise mode, respectively. Figure 13 shows the in-band phase noise when using low spur mode and low noise mode.

MUXOUT

The on-chip multiplexer is controlled by Bits[DB28:DB26] (see Figure 23).

Reference Doubler

Setting the DB25 bit to 0 disables the doubler and feeds the REF_{IN} signal directly into the 10-bit R counter. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the low spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the low noise mode and when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

Reference Divide by 2 (RDIV2)

Setting the DB24 bit to 1 inserts a divide by 2 toggle flip flop between the R counter and the PFD. This function allows a 50% duty cycle signal to appear at the PFD input, which is necessary when the charge pump boost mode is enabled (see the Boost Enable section).

10-Bit R Counter

The 10-bit R counter (Bits[DB23:DB14]) allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

Double Buffer

The DB13 bit enables or disables double buffering of Bits[DB22:DB20] in Register 4. For information about how double buffering works, see the Program Modes section.

Charge Pump Current Setting

Bits[DB11:DB9] set the charge pump current. Set this value to the charge pump current that the loop filter is designed with (see Figure 23).

Lock Detect Function (LDF)

The DB8 bit configures the lock detect function (LDF). The LDF controls the number of PFD cycles monitored by the lock detect circuit to ascertain whether lock has been achieved. When DB8 is set to 0, the number of PFD cycles monitored is 40. When DB8 is set to 1, the number of PFD cycles monitored is 5. It is recommended that the DB8 bit be set to 0 for fractional-N mode and 1 for integer N mode.

Lock Detect Precision (LDP)

The lock detect precision bit (Bit DB7) sets the comparison window in the lock detect circuit. When DB7 is set to 0, the comparison window is 10 ns; when DB7 is set to 1, the window is 6 ns. The lock detect circuit goes high when n consecutive PFD cycles are less than the comparison window value; n is set by the LDF bit (DB8). For example, with DB8 = 0 and DB7 = 0, 40 consecutive PFD cycles of 10 ns or less must occur before the digital lock detect goes high. The recommended settings for Bits[DB8:DB7] are listed in Table 7.

Table 7. Recommended LDF and LDP Bit Settings

Mode	DB8 (LDF)	DB7 (LDP)
Integer N	1	1
Fractional N, Low Noise Mode	0	1
Fractional N, Low Spur Mode	0	0

Power-Down (PD)

The DB5 bit provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. In software power-down mode, the device retains all information in its registers. The register contents are lost only when the supply voltages are removed.

When power-down is activated, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The $RF_{OUT}\pm$ buffers are disabled.
- The input registers remain active and capable of loading and latching data.

Charge Pump Three-State

Setting the DB4 bit to 1 sets the charge pump into three-state mode. Set this bit to 0 for normal operation.

Counter Reset

The DB3 bit is the reset bit for the R counter and the N counter of the ADF4152HV. When this bit is set to 1, the RF synthesizer N counter and R counter are held in reset. For normal operation, set this bit to 0.

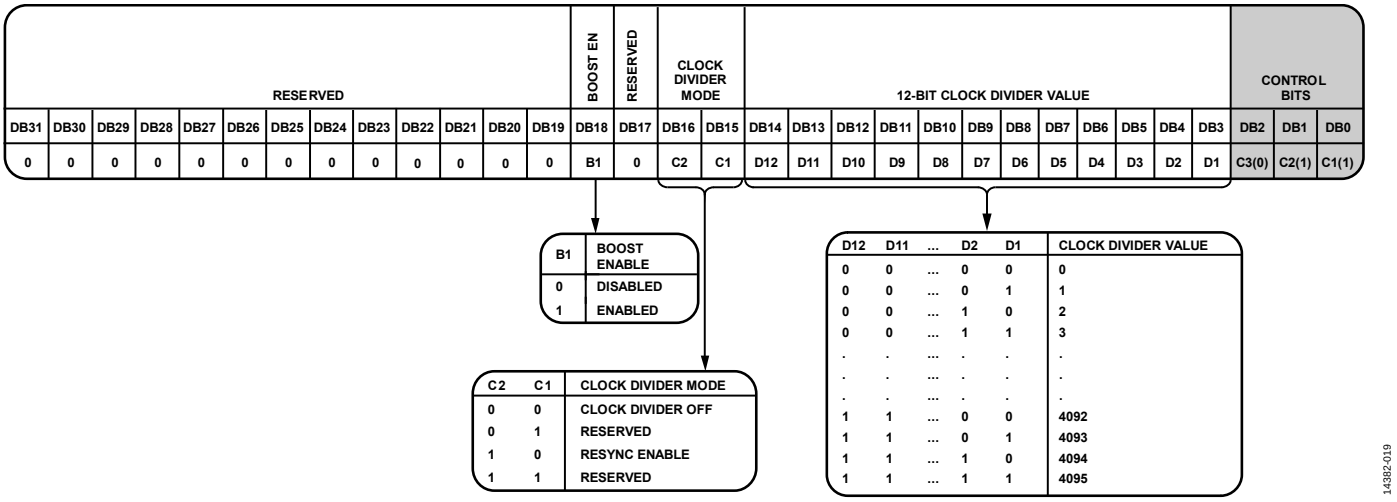


Figure 24. Register 3 (R3)

REGISTER 3

Control Bits

When Bits[C3:C1] are set to 011, Register 3 is programmed. Figure 24 shows the input data format for programming this register.

Boost Enable

Setting the DB18 bit to 1 enables the charge pump boost mode. If boost mode is enabled, the narrow loop bandwidth is maintained for spur attenuation, but faster lock times are still possible. Boost mode speeds up locking significantly for higher values of PFD frequencies that normally have many cycle slips.

When boost mode is enabled, an extra charge pump current cell is turned on. This cell outputs a constant current to the loop filter or removes a constant current from the loop filter (depending on whether the VCO tuning voltage (V_{TUNE}) needs to increase or decrease to acquire the new frequency) until V_{TUNE} approaches the lock voltage. The boost current is then disabled and the charge pump current setting reverts to the user programmed value.

Loop stability is maintained because the current is constant and is not pulsed, so there is no need to switch a compensating loop filter resistor in and out, as in standard fast lock modes. Note that the PFD requires a 45% to 55% duty cycle for the boost mode to operate correctly. This duty cycle can be guaranteed by setting the RDIV2 bit (DB24) in Register 2.

Clock Divider Mode

Bits[DB16:DB15] must be set to 10 to activate phase resync (see the Phase Resync section). Setting Bits[DB16:DB15] to 00 disables the clock divider (see Figure 24).

12-Bit Clock Divider Value

Bits[DB14:DB3] set the 12-bit clock divider value. This value is the timeout counter for activation of the phase resync. For more information, see the Phase Resync section.

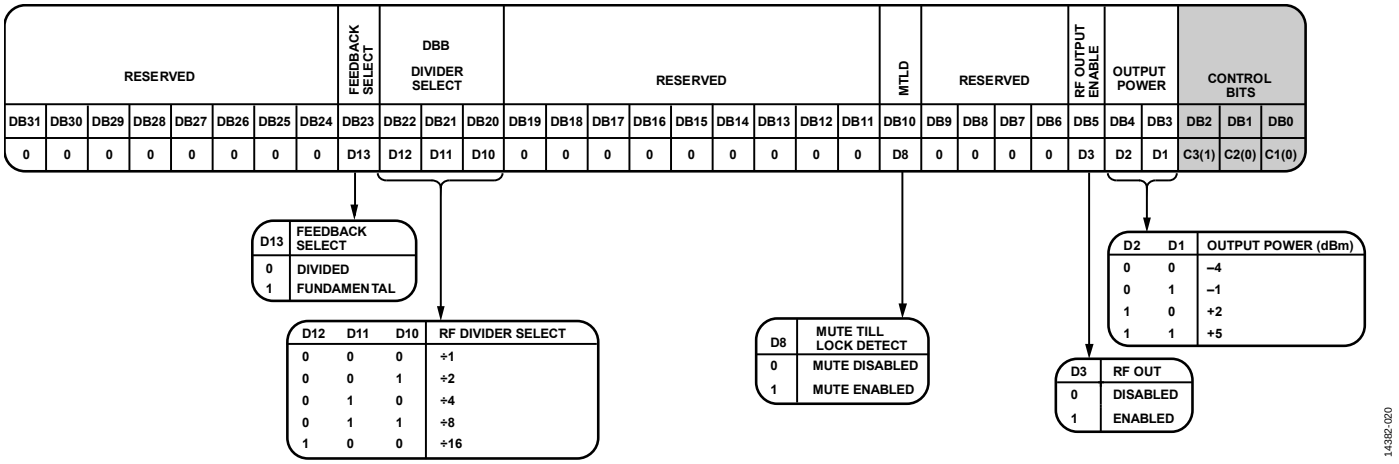


Figure 25. Register 4 (R4)

REGISTER 4

Control Bits

When Bits[C3:C1] are set to 100, Register 4 is programmed. Figure 25 shows the input data format for programming this register.

Feedback Select

The DB23 bit selects the feedback from the VCO output to the N counter. When this bit is set to 1, the signal is taken directly from the VCO. When this bit is set to 0, the signal is taken from the output of the output dividers. The dividers enable coverage of the wide frequency band (31.25 MHz to 3.0 GHz). When the dividers are enabled and the feedback signal is taken from the divider output, the RF output signals of two separately configured PLLs are in phase. Enabling the drivers is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

Bits[DB22:DB20] select the value of the output divider (see Figure 25).

Mute Till Lock Detect (MTLD)

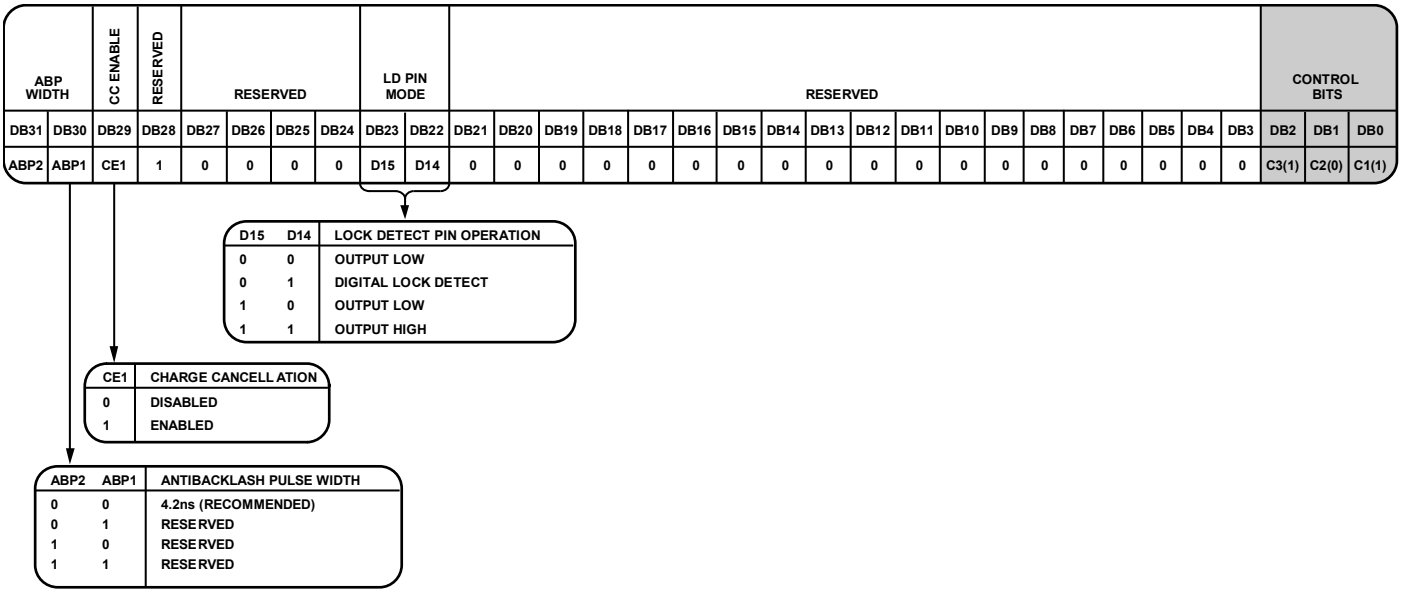
When the DB10 bit is set to 1, the supply current to the RF output stage is shut down until the device achieves lock, as measured by the digital lock detect circuitry.

RF Output Enable

The DB5 bit enables or disables the primary RF output. If DB5 is set to 0, the primary RF output is disabled; if DB5 is set to 1, the primary RF output is enabled.

Output Power

Bits[DB4:DB3] set the value of the primary RF output power level (see Figure 25).



[1]MUXOUT IN REGISTER 2 MUST ALSO BE SET TO DIGITAL LOCK DETECT FOR THE LOCK DETECT PIN TO OPERATE CORRECTLY.

Figure 26. Register 5 (R5)

REGISTER 5

Control Bits

When Bits[C3:C1] are set to 101, Register 5 is programmed. Figure 26 shows the input data format for programming this register.

Antibacklash Pulse (ABP) Width

Bits[DB31:DB30] set the PFD antibacklash pulse width. The recommended value for all operating modes is 4.2 ns (set Bits[DB31:DB30] to 00). Other antibacklash pulse width settings are reserved and are not recommended.

Charge Cancellation (CC) Enable

Setting the DB29 bit to 1 enables charge pump charge cancellation, which has the effect of reducing PFD spurs in integer N mode. In fractional-N mode, set this bit to 0.

Lock Detect Pin Operation

Bits[DB23:DB22] set the operation of the lock detect (LD) pin (see Figure 26).

REGISTER INITIALIZATION SEQUENCE

At initial power-up, after the correct application of voltages to the supply pins, program the ADF4152HV registers in the following sequence:

1. Register 5
2. Register 4
3. Register 3
4. Register 2
5. Register 1
6. Register 0

RF SYNTHESIZER—A WORKED EXAMPLE

Use the following equations to program the ADF4152HV synthesizer:

$$RF_{OUT} = (INT + (FRAC/MOD)) \times (f_{PFD}/RF\ Divider) \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC$ is the numerator of the fractional division (0 to MOD − 1).
MOD is the modulus.
RF Divider is the output divider that divides down the VCO frequency.
f_{PFD} is the PFD frequency, calculated in Equation 4.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF reference doubler bit (0 or 1), DB25 in Register R2.
R is the RF reference division factor (1 to 1023).
T is the reference divide by 2 bit (0 or 1).

In this example, a 1.5 GHz RF frequency output (RF_{OUT}) with a 500 kHz channel resolution at RF_{OUT} (f_{RESOUT}) required on the RF output is programmed. The reference frequency input (REF_{IN}) is 25 MHz. The VCO options available to the user include the following:

- 1.5 GHz VCO in fundamental mode
- 3 GHz VCO with the RF divider set to 2

When enabling the RF divider, the user must choose to either close the PLL loop before the RF divider or after the RF divider. In this example, the PLL loop is closed before the RF divider (see Figure 27).

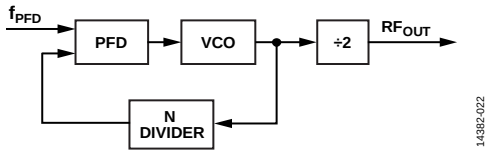


Figure 27. PLL Loop Closed Before Output Divider

To minimize VCO feedthrough, the 3 GHz VCO is selected. A channel resolution (f_{RESOUT}) of 500 kHz is required at the output of the RF divider. Therefore, the channel resolution at the output of the VCO (f_{RES}) must be 2 × f_{RESOUT}, that is, 1 MHz.

$$MOD = REF_{IN}/f_{RES}$$
$$MOD = 25\ MHz/1\ MHz = 25$$

From Equation 4,

$$f_{PFD} = (25\ MHz \times (1 + 0)/1) = 25\ MHz \quad (5)$$

From Equation 3,

$$1500.5\ MHz = 25\ MHz \times ((INT + (FRAC/25))/2) \quad (6)$$

where:
INT = 120.
FRAC = 1.

The RF divider value is fixed at 2.

Use the ADF4152HV evaluation software to determine integer and fractional values for a given setup, as well as the actual register settings to be programmed.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. Doubling the reference signal doubles the PFD comparison frequency, which improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. Note that the PFD cannot operate above 26 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency. The 50% duty cycle PFD frequency is necessary for the correct operation of the charge pump boost mode. For more information, see the Boost Enable section.

12-BIT PROGRAMMABLE MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution at RF_{OUT} (f_{RESOUT}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65, which means that the RF output resolution (f_{RESOUT}) is the 200 kHz (13 MHz/65) necessary for GSM. With dither off, the fractional spur interval depends on the modulus values chosen (see Table 8).

Unlike most other fractional-N PLLs, the ADF4152HV allows the user to program the modulus over a 12-bit range. When combined with the reference doubler and the 10-bit R counter, the 12-bit modulus allows the user to set up the device in many different configurations for the application.

For example, consider an application that requires a 1.75 GHz RF frequency output with a 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is to feed the 13 MHz reference signal directly into the PFD and to program the modulus to divide by 65. This setup results in the required 200 kHz resolution.

Another possible setup is to use the reference doubler to create 26 MHz from the 13 MHz input signal. The 26 MHz is then fed into the PFD, and the modulus is programmed to divide by 130. This setup also results in 200 kHz resolution but offers superior phase noise performance over the first setup.

The programmable modulus is also very useful for multistandard applications with different channel spacing requirements.

It is important that the PFD frequency remain constant (in this example, 13 MHz). The constant PFD frequency allows the user to design one loop filter for both setups without encountering stability issues. Note that the ratio of the RF frequency to the PFD frequency principally affects the loop filter design, and not the actual channel spacing.

SPURIOUS OPTIMIZATION AND BOOST MODE

Narrow loop bandwidths can filter unwanted spurious signals, but these bandwidths usually have a long lock time. A wider loop bandwidth achieves faster lock times, but may lead to increased spurious signals inside the loop bandwidth.

The boost mode feature can achieve the same fast lock time as the wider bandwidth, but with the advantage of a narrow final loop bandwidth to keep spurs low (see the Boost Enable section).

SPUR MECHANISMS

This section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4152HV.

Fractional Spurs

The fractional interpolator in the ADF4152HV is a third-order, Σ-Δ modulator with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither on), the minimum allowable value of MOD is 50. The Σ-Δ modulator is clocked at the PFD reference rate (f_{PFD}), which allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

In low noise mode (dither off), the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order Σ-Δ modulator used in the ADF4152HV, the repeat length depends on the value of MOD, as listed in Table 8.

Table 8. Fractional Spurs with Dither Off (Low Noise Mode)

MOD Value (Dither Off)	Repeat Length	Spur Interval
Divisible by 2, But Not by 3	2 × MOD	Channel step/2
Divisible by 3, But Not by 2	3 × MOD	Channel step/3
Divisible by 6	6 × MOD	Channel step/6
Not Divisible by 2, 3, or 6	MOD	Channel step

In low spur mode (dither on), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum appear as broadband noise. This dither may degrade the in-band phase noise at the PLL output by as much as 10 dB. For lowest noise, dither off is a better choice, particularly when the final loop bandwidth is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note, or difference frequency, between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth (thus the name integer boundary spurs).

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop may cause a problem. The PCB layout must ensure adequate isolation between VCO traces and the input reference to avoid a possible feedthrough path on the board.

SPUR CONSISTENCY AND FRACTIONAL SPUR OPTIMIZATION

With dither off, the fractional spur pattern due to the quantization noise of the Σ-Δ modulator also depends on the particular phase word with which the modulator is seeded.

The phase word can be varied to optimize the fractional and subfractional spur levels on any particular frequency. Thus, a lookup table of phase values corresponding to each frequency can be constructed for use when programming the ADF4152HV.

If a lookup table is not used, keep the phase word at a constant value to ensure consistent spur levels on any particular frequency.

PHASE RESYNC

The output of a fractional-N PLL can settle to any one of the MOD phase offsets with respect to the input reference, where MOD is the fractional modulus. The phase resync feature of the ADF4152HV produces a consistent output phase offset with respect to the input reference. The consistent output phase offset with respect to the input reference is necessary in applications where the output phase and frequency are important, such as digital beamforming. For information about how to program a specific RF output phase when using phase resync, see the Phase Programmability section.

Phase resync is enabled by setting Bits[DB16:DB15] in Register 3 to 10. When phase resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} given by the following formula:

$$t_{SYNC} = CLK\_DIV\_VALUE \times MOD \times t_{PFD}$$

where:

t_{SYNC} is the time interval between sync signals.
CLK_DIV_VALUE is the decimal value programmed in Bits[DB14:DB3] of Register 3 and can be any integer in the range of 1 to 4095.
MOD is the modulus value programmed in Bits[DB14:DB3] of Register 1.
t_{PFD} is the PFD reference period.

When a new frequency is programmed, the second sync pulse after the LE rising edge resynchronizes the output phase to the reference. The t_{SYNC} time must be programmed to a value that is at least as long as the worst case lock time to guarantee that the phase resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 28, the PFD reference is 25 MHz and MOD is 125 for a 200 kHz channel spacing. t_{SYNC} is set to 400 µs by programming CLK_DIV_VALUE = 80.

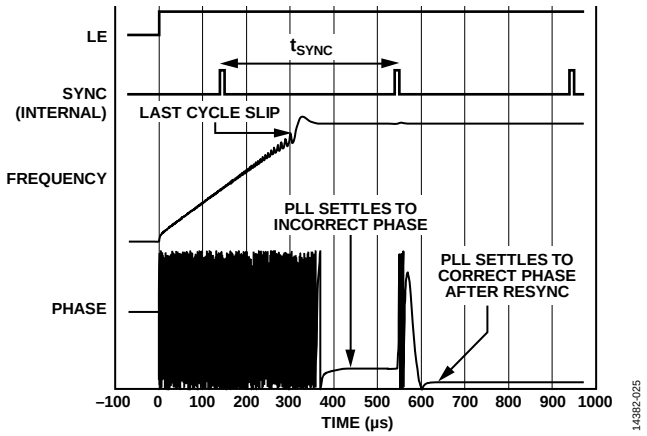


Figure 28. Phase Resync Example

Phase Programmability

The phase word in Register 1 controls the RF output phase. As this word is swept from 0 to MOD, the RF output phase sweeps over a 360° range in steps of 360°/MOD.

APPLICATIONS INFORMATION

ULTRAWIDEBAND PLL

When paired with an octave tuning range VCO, the ADF4152HV provides an ultrawideband PLL function using the on-board RF dividers. With an octave tuning range at the fundamental frequency, the RF dividers provide full frequency coverage with no gaps down to much lower frequencies.

For example, using a 1 GHz to 2 GHz octave tuning range VCO (such as the Synergy DCYS100200-12), the user can obtain contiguous output frequencies from 62.5 MHz to 2 GHz at the ADF4152HV RF outputs, as shown in Figure 29. A broadband output match is achieved using a 27 nH inductor in parallel with a 50 Ω resistor (for more information, see the Output Matching section). With such a wide output range, the same PLL hardware design can generate different frequencies for each of the different hardware platforms in the system.

MICROWAVE PLL

The ADF4152HV can be interfaced directly to a wide tuning range microwave VCO without the need for an active filter. Typically, most microwave VCOs have a maximum tuning range of 15 V. In this case, set V_P on the ADF4152HV to a value of 16 V or higher to ensure sufficient headroom in the charge pump. An external prescaler, such as the ADF5001, is required to divide down VCO frequencies that are above the maximum RF input frequency of 5.0 GHz.

In the application circuit shown in Figure 30, the ADF5001 divides down the 16 GHz VCO signal to 4 GHz, which can then be input directly into the ADF4152HV RF inputs. The ADF5001 can be connected either single-endedly or differentially to the ADF4152HV. For best performance and to achieve maximum power transfer, it is recommended that a differential connection be used.

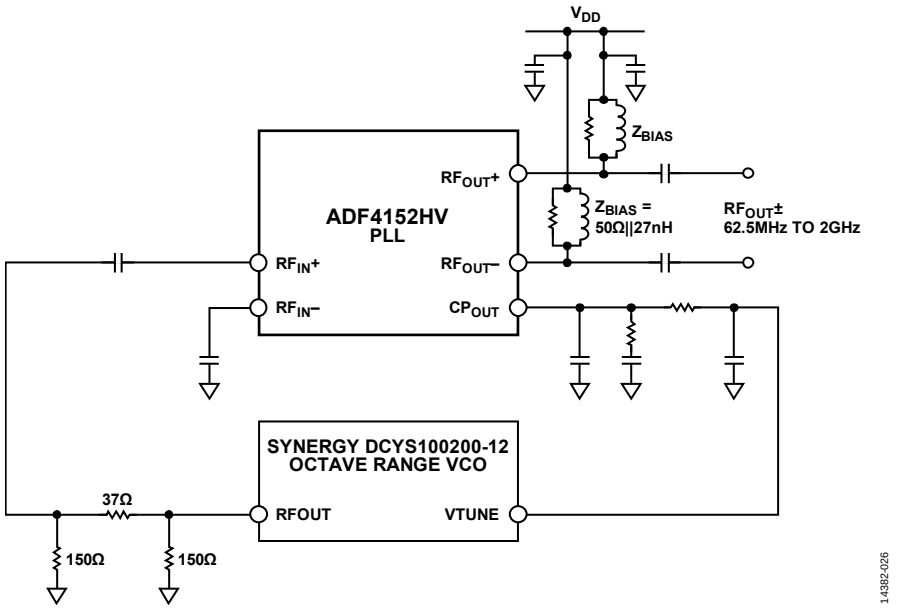


Figure 29. Ultrawideband PLL Using the ADF4152HV and an Octave Tuning Range VCO

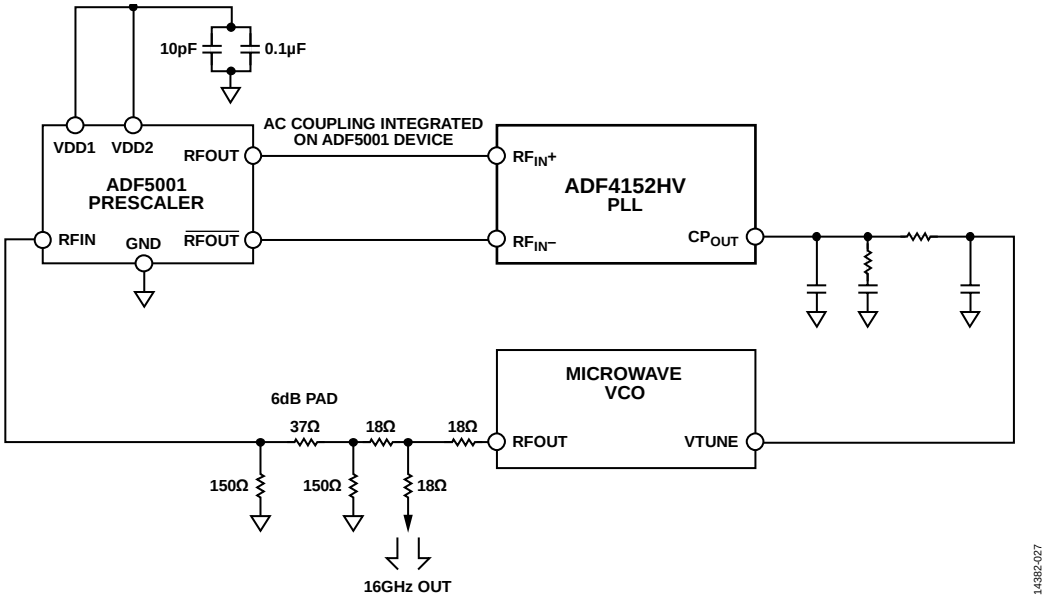


Figure 30. 16 GHz Microwave PLL

GENERATING THE HIGH VOLTAGE SUPPLY

It is possible to use a boost converter such as the Analog Devices ADP1613 to generate the high voltage charge pump supply from a lower voltage rail without degrading PLL performance. To minimize any switching noise feedthrough, ensure that sufficient decoupling is placed close to the charge pump supply pin (Pin 6). Take care to use capacitors with the appropriate voltage rating; for example, if using a boost converter to generate a 20 V V_P supply, use capacitors with a rating of 20 V or higher.

The design of the boost converter is simplified using the Excel-based boost regulator design tool. This tool is available from the ADP1613 product page under tools and simulations. Figure 31 shows the user inputs for a 5 V input to 20 V output design. To minimize voltage ripple at the output of the converter stage, select the **Noise Filter** check box, and set the **Vout Ripple** box to its minimum value. The high voltage charge pump current draw is 2 mA maximum; therefore, a value of 0.01 A is entered in the **Iout** box to provide a margin.

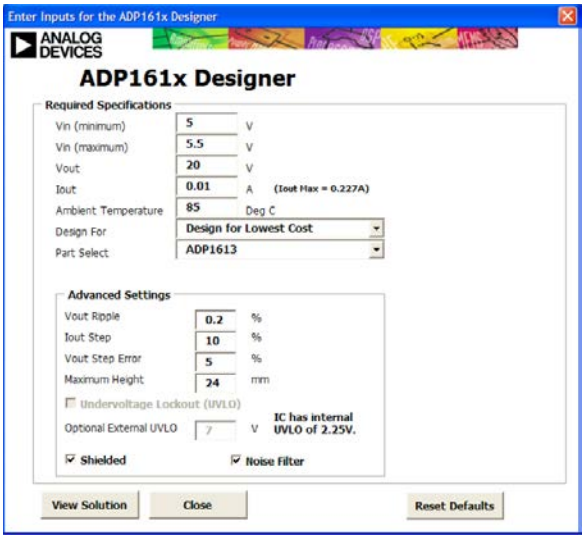


Figure 31. Designer Tool

INTERFACING THE ADF4152HV TO THE ADUC7024 OR THE ADSP-BF527

The ADF4152HV has a simple SPI-compatible serial interface for writing to the device. The CLK, DATA, and LE pins control the data transfer. When LE goes high, the 32 bits that were clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 6 for the register address truth table.

ADuC7024 Interface

Figure 32 shows the interface between the ADF4152HV and the ADuC7024 analog microcontroller. The ADuC7024 is based on an ARM7 core, but the same interface can be used with any 8051-based microcontroller.

The microcontroller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4152HV needs a 32-bit word, which is accomplished by writing four 8-bit bytes from the microcontroller to the device. After the fourth byte is written, bring the LE input high to complete the transfer.

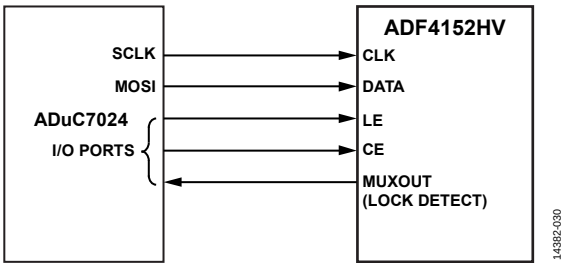


Figure 32. ADuC7024 to ADF4152HV Interface

I/O port lines on the ADuC7024 also control the power-down input (CE) and the lock detect (MUXOUT configured for lock detect and polled by the port input). When operating in the SPI master mode with CPHA = 0, the maximum SPI transfer rate of the ADuC7024 is 20 Mbps. This transfer rate means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock, ensure that the SPI timing requirements listed in Table 2 are adhered to.

Blackfin ADSP-BF527 Interface

Figure 33 shows the interface between the ADF4152HV and the Blackfin® ADSP-BF527 digital signal processor (DSP). The ADF4152HV needs a 32-bit serial word for each latch write. The easiest way to accomplish this using the Blackfin family is to use the autobuffered transmit mode of operation with alternate framing. This mode provides a means for transmitting an entire block of serial data before an interrupt is generated.

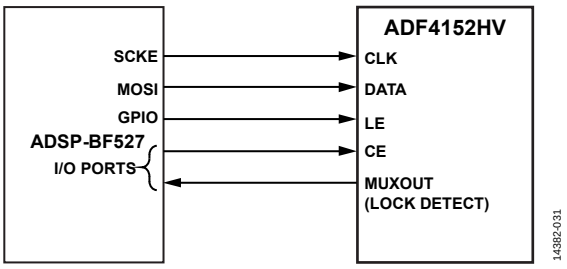


Figure 33. ADSP-BF527 to ADF4152HV Interface

Set up the word length for eight bits and use four memory locations for each 32-bit word. To program each 32-bit latch, store the 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. If using a faster SPI clock, ensure that the SPI timing requirements listed in Table 2 are adhered to.

PCB DESIGN GUIDELINES FOR A CHIP SCALE PACKAGE

The lands on the chip scale package (CP-32-11) are rectangular. The PCB pad for these lands must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Each land must be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central exposed thermal pad. The thermal pad on the PCB must be at least as large as the exposed pad. On the PCB, there must be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, they must be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. of copper to plug the via.

OUTPUT MATCHING

The output of the ADF4152HV can be matched in a number of ways for optimum operation; the most basic is to connect a 50 Ω resistor to AV_{DD}. A dc bypass capacitor of 100 pF is connected in series, as shown in Figure 34. Because the resistor is not frequency dependent, this method provides a good broadband match. When connected to a 50 Ω load, this circuit typically gives a differential output power equal to the values chosen by Bits[DB4:DB3] in Register 4.

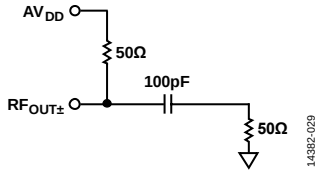


Figure 34. Simple ADF4152HV Output Stage

Another solution is to connect a shunt inductor (acting as an RF choke) to AV_{DD}. This solution can help provide a better narrow-band match and, therefore, more output power. However, because the output stage is open-collector, it is recommended that a termination resistor be used in addition to the RF choke to give a defined output impedance. The termination resistor can be either 50 Ω in parallel with the RF choke or 100 Ω connected across the RF output pins.

The circuit shown in Figure 35 provides a good broadband match to 50 Ω for frequencies from 250 MHz to 5.0 GHz. The maximum output power in this case is approximately 5 dBm. The inductor can be increased for operation below 250 MHz. Both single-ended architectures can be examined using the EVAL-ADF4152HVEB1Z evaluation board.

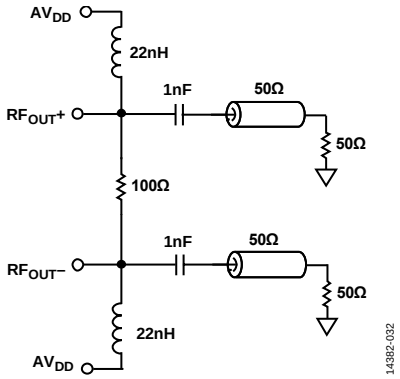


Figure 35. Optimum ADF4152HV Output Stage

If differential outputs are not needed, the unused output can be terminated, or both outputs can be combined using a balun.

OUTLINE DIMENSIONS

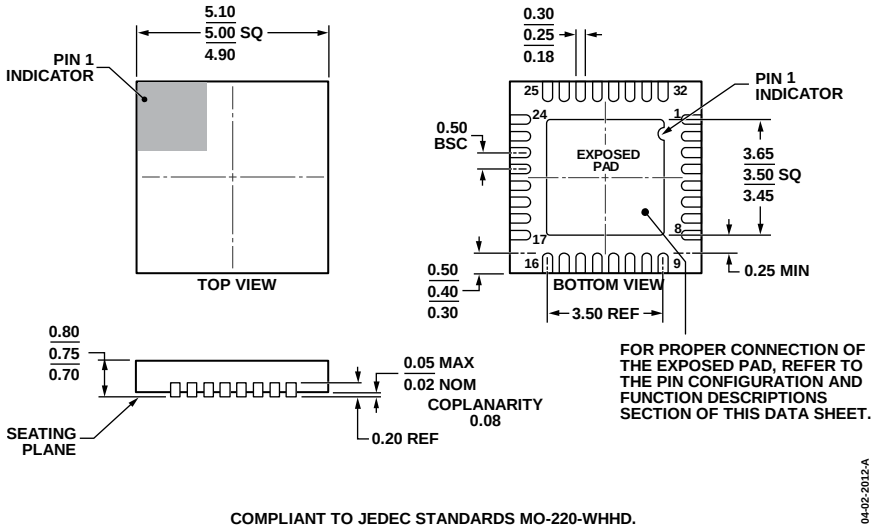


Figure 36. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4152HVBCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11
ADF4152HVBCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11
EVAL-ADF4152HVEB1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.