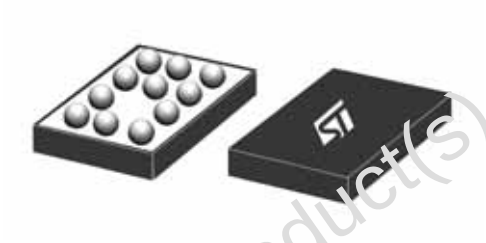
STG4259

Low voltage 0.3Ω max dual SPDT switch with break-before-make feature and 15KV ESD protection

Features

- Wide operating voltage range: V_{CC} (Opr) = 1.65 V to 4.8 V
- Low power dissipation: I_{CC} = 0.2 µA (max) at T_A = 85°C
- Low ON resistance V_{IN} = 0V:
  - R_{ON} = 0.4 Ω (max T_A = 25ºC) at V_{CC} = 2.25 V
  - R_{ON} = 0.35 Ω (max T_A = 25ºC) at V_{CC} = 3.0 V
  - R_{ON} = 0.30 Ω (max T_A = 25ºC) at V_{CC} = 4.3 V
- Separate supply voltage for switch and control pin
- Separate control pin for each switch
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD performance tested on common channels (D1 and D2 pins)
  - 9 kV IEC-61000-4-2 ESD, contact discharge
  - 15 kV IEC-61000-4-2 ESD, air gap discharge
- ESD performance tested on all other pins
  - 8 kV IEC-61000-4-2 ESD, contact discharge
  - 500 V machine model (JESD22 A115-A)
  - 1500 V charged-device model (JESD22 C101)
  - 8 kV IEC-61000-4-2 ESD, air gap discharge



Flip-Chip11

Description

The STG4259 is a high-speed CMOS low voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/ demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65 V to 4.8 V, making this device ideal for portable applications. It offers low ON resistance (0.30 Ω) at V_{CC} = 4.3 V. The SEL inputs are provided to control the switches.

The switch S1 is ON (connected to common port D) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common port D) when the SEL input is held low and OFF (high impedance state exist between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packing
STG4259BJR	Flip-Chip11	Tape and Reel

Contents

1 Logic diagram and pin-out information 3

2 Maximum rating 5

3 Electrical characteristics 7

4 Test circuits 10

5 Package mechanical data 13

6 Revision history 18

1 Logic diagram and pin-out information

Figure 1. Functional diagram

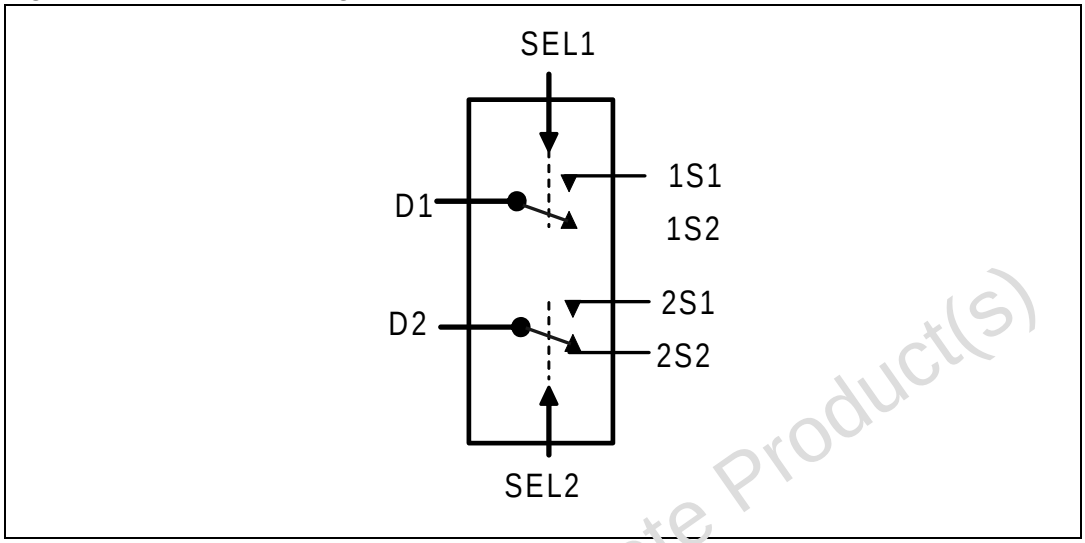


Figure 2. Input equivalent circuit

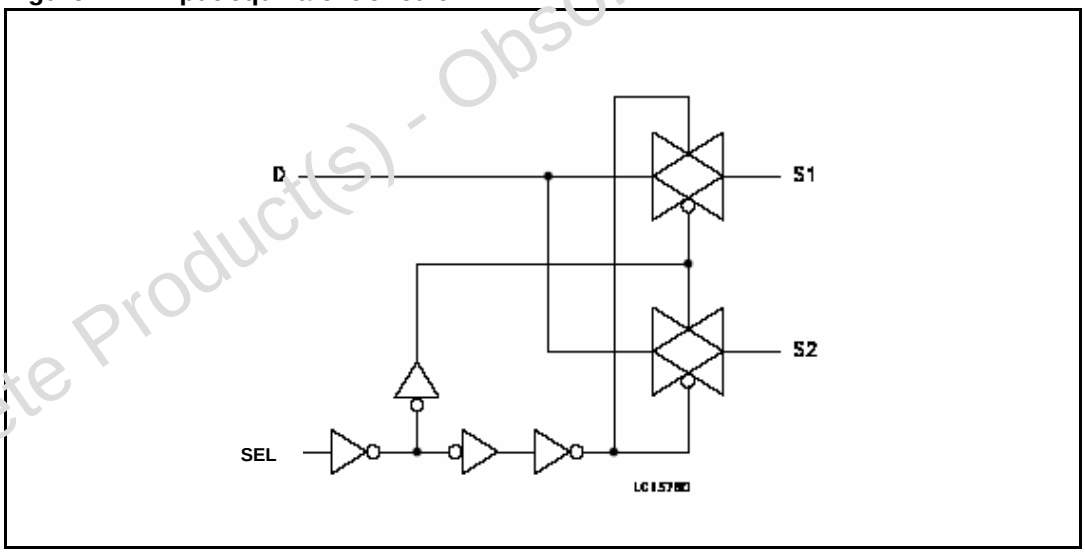
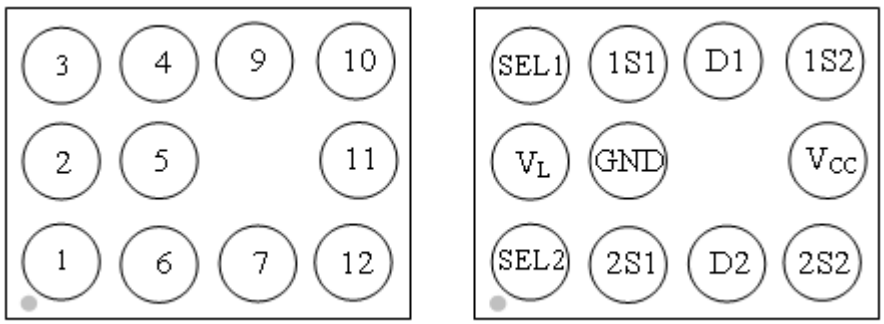


Table 2. Truth table

SELn	Switch nS1	Switch nS2
H	ON	OFF (1)
L	OFF (1)	ON

1. High impedance

Figure 3. Pin connection (bump side view)



Flip-Chip11

Table 3. Pin description

Flip-Chip11	Symbol	Name and function
4, 10, 6, 12	1S1, 1S2, 2S1, 2S2	Independent channels
9, 7	D1, D2	Common channels
3, 1	SEL1, SEL2	Control
11	V_{CC}	Positive supply voltage
2	V_L	Logic supply voltage
5	GND	Ground (0V)

2 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_L	Logic supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to V_L + 0.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL}< 0V)	- 50	mA
I_{IK}	DC input diode current (V_{SEL}< 0V)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at T_A = 70ºC (1)	500	mW
T_{stg}	Storage temperature	-50 to 105	°C
T_L	Lead temperature (10 sec)	260	°C

1. Derate above 70ºC by 18.5mW/C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		1.65 to 4.8	V
V_L	Logic supply voltage		1.65 to V_{CC}	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to V_L	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_L = 1.65 V to 2.7 V	0 to 20	ns/V
		V_L = 3.0 to 4.8 V	0 to 10	

1. Truth table guaranteed: 1.65 V to 4.8 V

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 - 4.3	1.65 - 1.95		1.25			1.25		V
			2.3 - 2.7		1.75			1.75		
			3.0 - 3.6		2.35			2.35		
			4.3		2.8			2.8		
V_{IL}	Low level input voltage	1.65 - 4.3	1.65 - 1.95				0.6		0.6	V
			2.3 - 2.7				0.8		0.8	
			3.0 - 3.6				1.05		1.05	
			4.3				1.5		1.5	
R_{ON}	ON resistance	1.8	1.65 - 4.8	V_S = 0 V to V_{CC} I_S = 100 mA		0.49	0.65		0.85	Ω
		2.25				0.30	0.40		0.50	
		3				0.25	0.35		0.45	
		3.7				0.22	0.32		0.42	
		4.3				0.21	0.30		0.40	
ΔR_{ON}	ON resistance match between channels (1)	1.8	1.65 - 4.8	V_S = 0 V to V_{CC} I_S = 100 mA		5				mΩ
		2.25				3				
		3				3				
		3.7				3				
		4.3				3				
R_{FLAT}	ON resistance flatness (2)	1.8	1.65 - 4.8	V_S = 0 V to V_{CC} I_S = 100 mA		300	400		450	mΩ
		2.5				130	170		230	
		3				90	120		170	
		3.7				90	120		170	
		4.3				90	120		170	
I_{OFF}	Sn OFF state leakage current	1.65 - 4.8	1.65 - 4.8	V_S = 0 to V_{CC} V_D = 0 to V_{CC}	-20		20	-300	300	nA
I_{ON}	Sn ON state leakage current	1.65 - 4.8	1.65 - 4.8	V_S = 0 to V_{CC} V_D = open	-20		20	-100	100	nA

Table 6. DC specifications (continued)

I_D	D ON state leakage current	1.65 - 4.8	1.65 - 4.8	V_S = open V_D = 0 to V_{CC}	-20		20	-100	100	nA
I_{CC}	Quiescent supply current	1.65-4.8	1.65 - 4.8	V_{SEL}= V_{CC} or GND	-0.05		0.05	-0.2	0.2	µA
I_{SEL}	SEL leakage current	1.65-4.8	1.65 - 4.8	V_{SEL}= 4.3V or GND	-0.1		0.1	-1	1	µA

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$
2. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$5 ns)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 - 1.95	1.65 - 4.8			0.13				ns
		2.3 - 2.7				0.15				
		3.0 - 3.3				0.16				
		3.6 - 4.3				0.16				
t_{ON}	Turn-ON time	1.65 - 1.95	1.65 - 4.8	V_S = V_{CC} R_L = 50 Ω C_L = 30 pF		95	123		95	ns
		2.3 - 2.7				48	62		70	
		3 - 3.6				33	43		55	
		4.3				29	38		40	
t_{OFF}	Turn-OFF time	1.65 - 1.95	1.65 - 4.8	V_S = V_{CC} R_L = 50 Ω C_L = 30 pF		12	15		70	ns
		2.3 - 2.7				12	16		55	
		3 - 3.6				13	17		40	
		4.3				13	17		35	
t_D	Break-before-make time delay	1.65 - 1.95	1.65 - 4.8	C_L = 35 pF R_L = 50 Ω V_S = V_{CC}/2	10	66				ns
		2.3 - 2.7			10	28				
		3 - 3.6			10	18				
		4.3			10	12				
Q	Charge injection	1.65-1.95	1.65-4.8	C_L = 1nF V_{GEN} = 0V		86				pC
		2.3-2.7				95				
		3.0-3.3				98				
		3.6-4.3				103				

Table 8. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
O_{IRR}	OFF isolation (1)	1.65 - 4.3	4.3	V_S = 1V_{RMS} f = 100kHz		-71				dB
Xtalk	Crosstalk	1.6 - 4.3	4.3	V_S = 1V_{RMS} f = 100 kHz		-93				dB
T_{HD}	Total harmonic distortion	2.3 - 4.3	4.3	R_L = 600 Ω C_L = 50 pF V_S = V_{CC} V_{PP} f = 600Hz to 20 kHz		0.01				%
BW	-3dB bandwidth (switch ON)	1.65 - 4.3	4.3	R_L = 50Ω		40				MHz
C_{SEL}	Control pin input capacitance	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}		30				pF
C_{Sn}	Sn port capacitance	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}		95				pF
C_D	D port capacitance when switch is enabled	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}		230				pF

1. OFF-isolation = 20 $\log_{10}$ (VD/VS), V_D = output, V_S = input to off switch

4 Test circuits

Figure 4. ON resistance

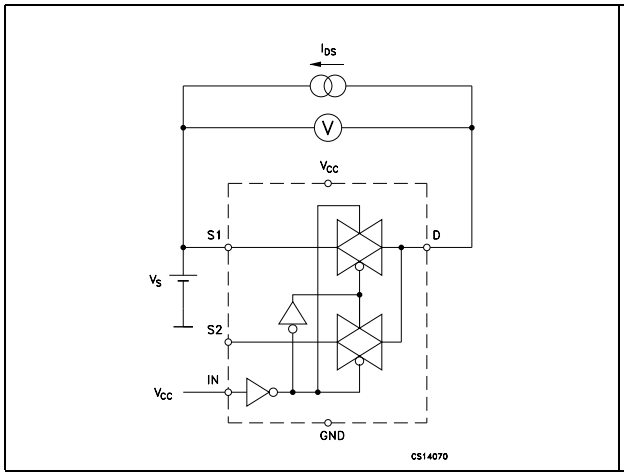


Figure 5. Bandwidth

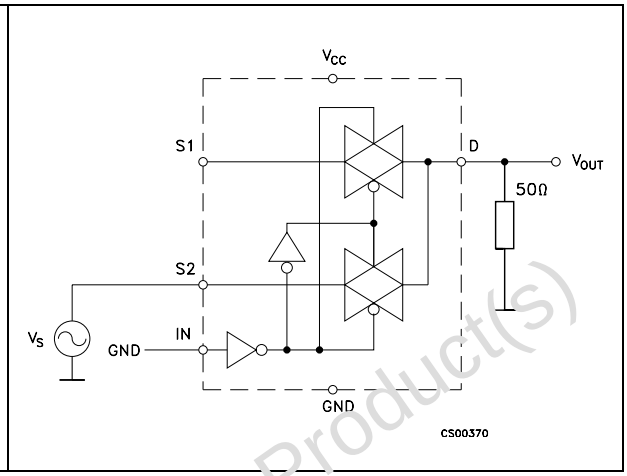


Figure 6. OFF leakage

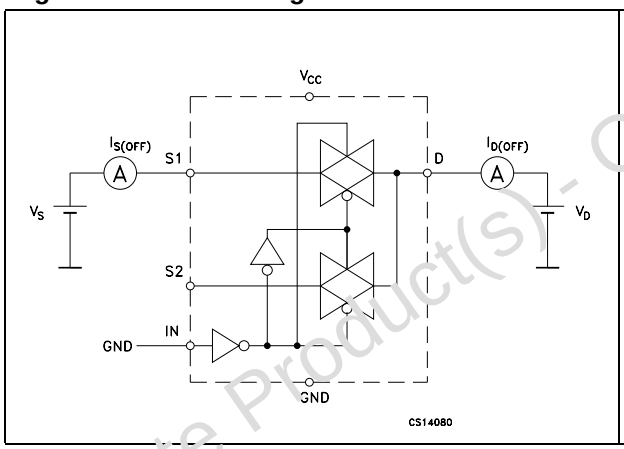


Figure 7. Channel-to-channel crosstalk

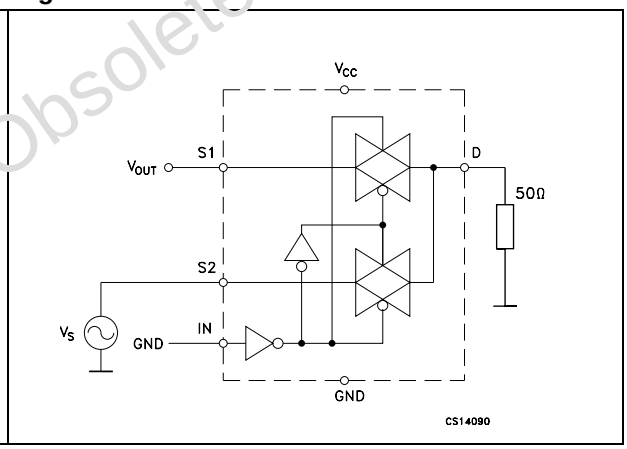


Figure 8. OFF isolation

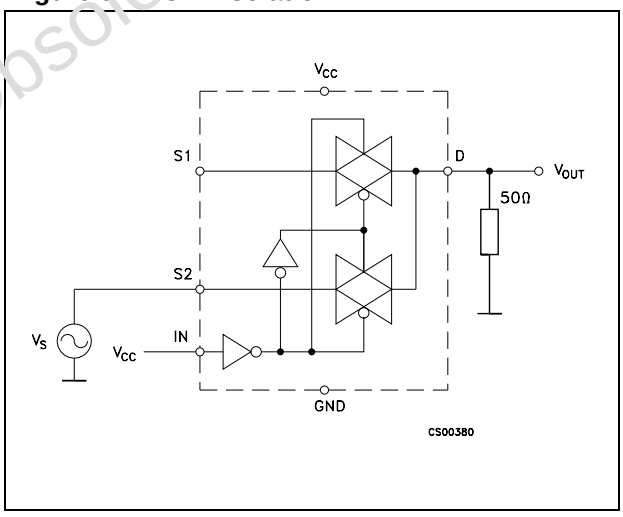
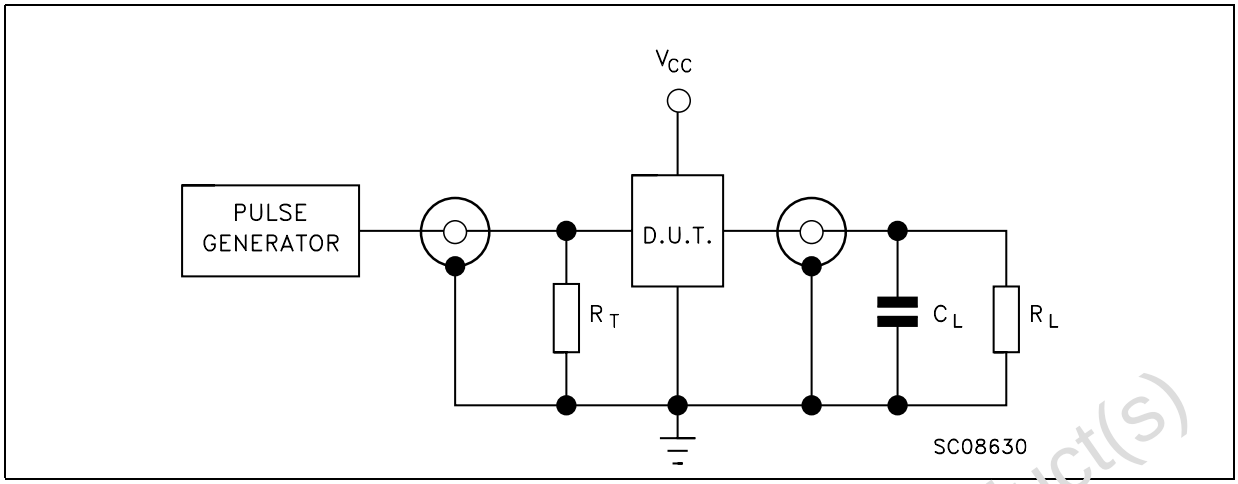


Figure 9. Test circuit



Note: *1* C_L = 5/35pF or equivalent: (includes jig capacitance)

2 R_L = 50Ω *or equivalent*

3 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 10. Break-before-make time delay

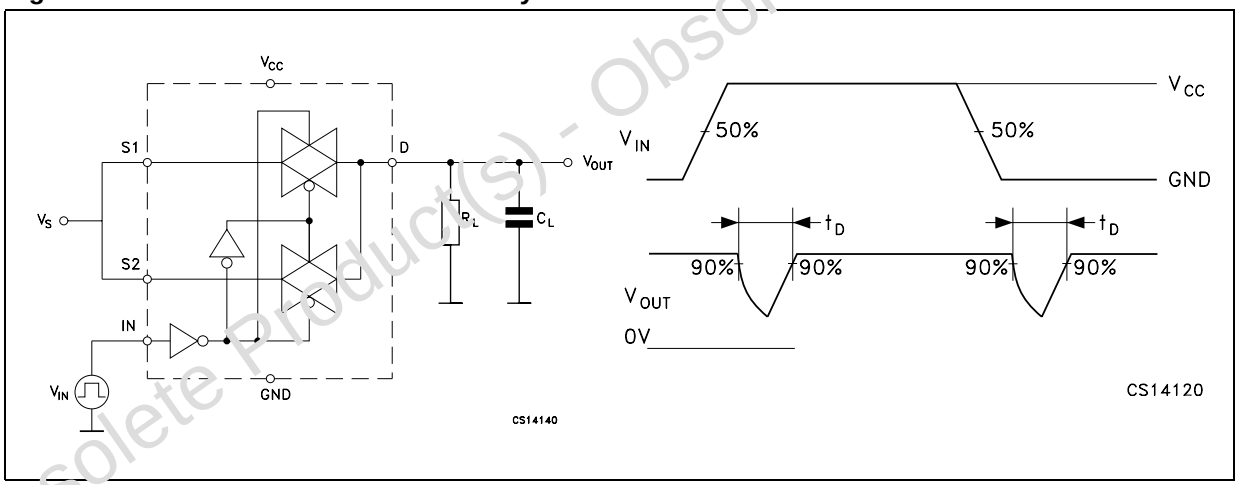


Figure 11. Switching time and charge injection
(V_{GEN} = 0V, R_{GEN} = 0Ω, R_L = 1MΩ, C_L = 100pF)

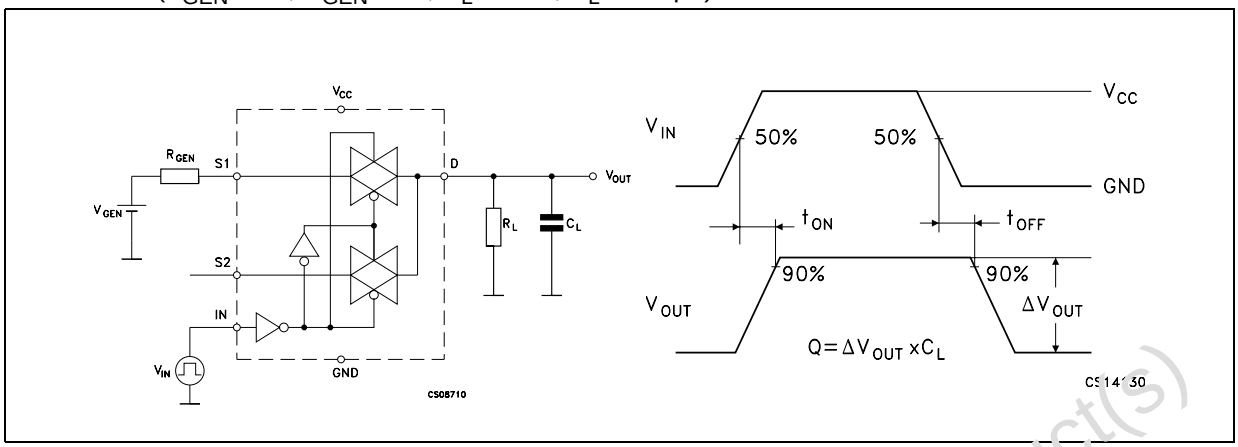
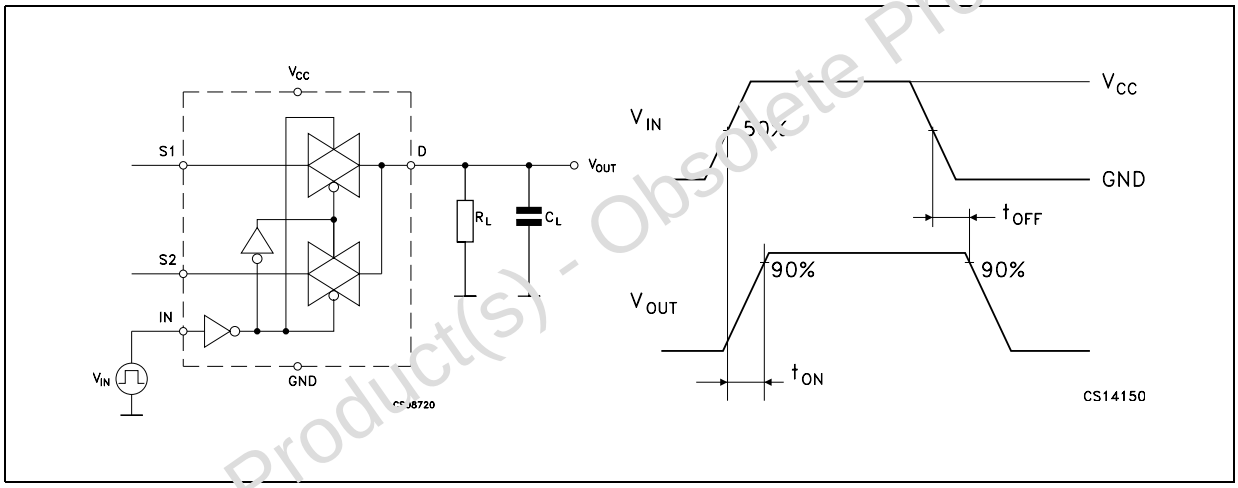


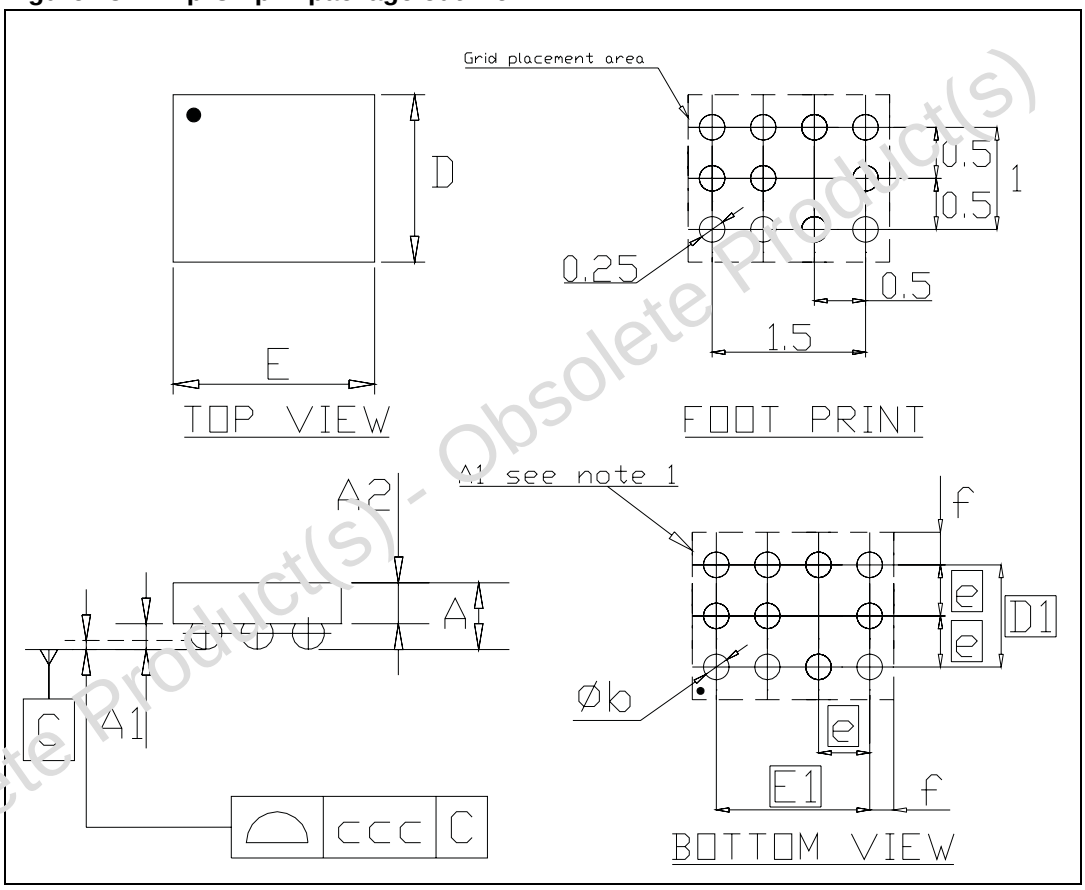
Figure 12. Turn ON, turn OFF delay time



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 13. Flip-Chip11 package outline



1. Drawing not to scale.

Table 9. Flip-Chip11 mechanical data

Dim.	Data book (mm)			Drawing (mm)		
	Min	Typ	Max	Min	Typ	Max
A	0.585	0.65	0.715	0.60	0.65	0.70
A1	0.21	0.25	0.29	0.22	0.25	0.28
A2		0.4		0.38	0.4	0.42
b	0.265	0.315	0.365	0.290	0.315	0.340
D	1.518	1.568	1.618	1.553	1.568	1.583
D1		1		0.99	1	1.01
E	2.018	2.068	2.118	2.083	2.068	2.118
E1		1.5		1.49	1.5	1.51
e	0.45	0.5	0.55	0.46	0.5	0.54
f		0.284		0.272	0.284	0.292
ccc		0.08			0.08	

The terminal A1 on the bumps side is identified by a distinguishing feature (for instance by a circular “clear area” - typically 0.1 mm diameter) and/or a missing bump. The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular “dot” - typically 0.5 mm diameter).

Figure 14. Foot print recommendations

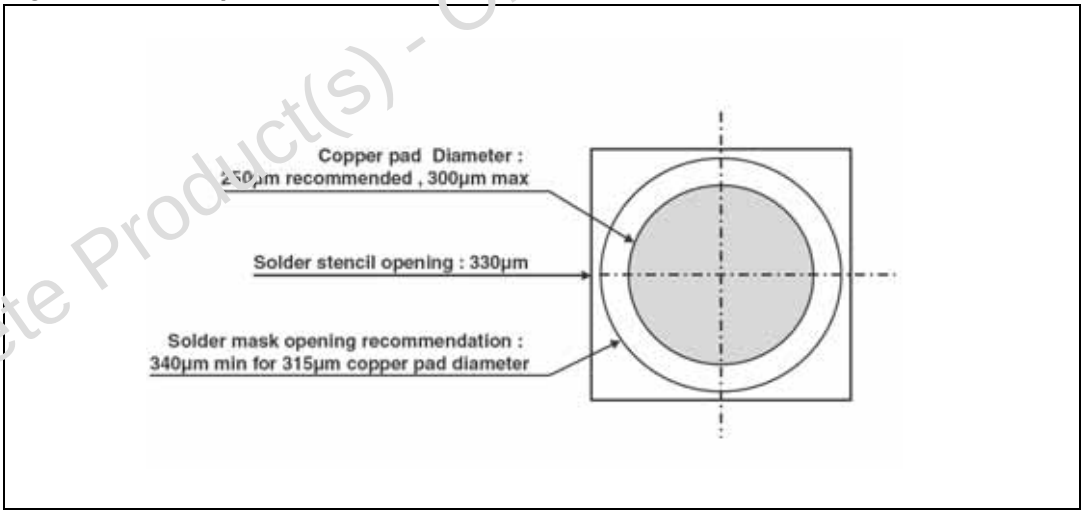


Figure 15. Marking

Dot, ST logo
S2 = marking
V = manufacturing Location
yww = datecode (y = year, ww = week)

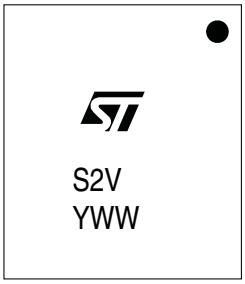


Figure 16. Flip-Chip11 tape specification

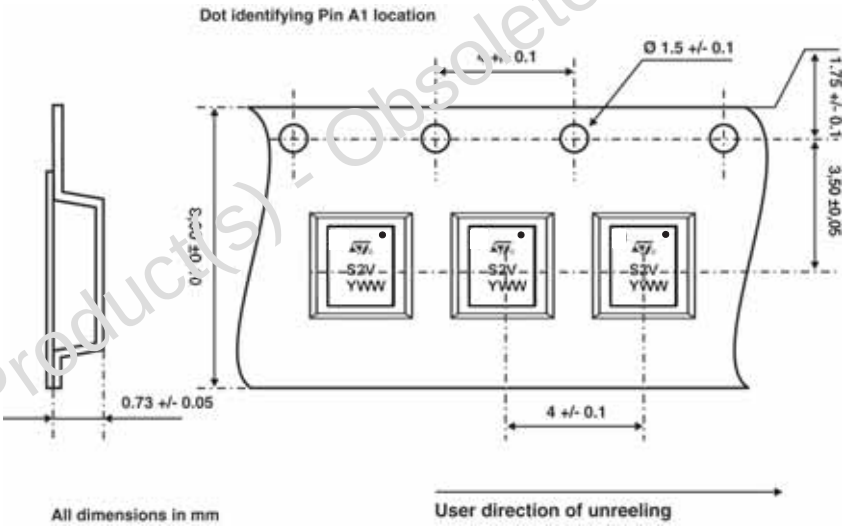


Figure 17. Flip-Chip11 reel information

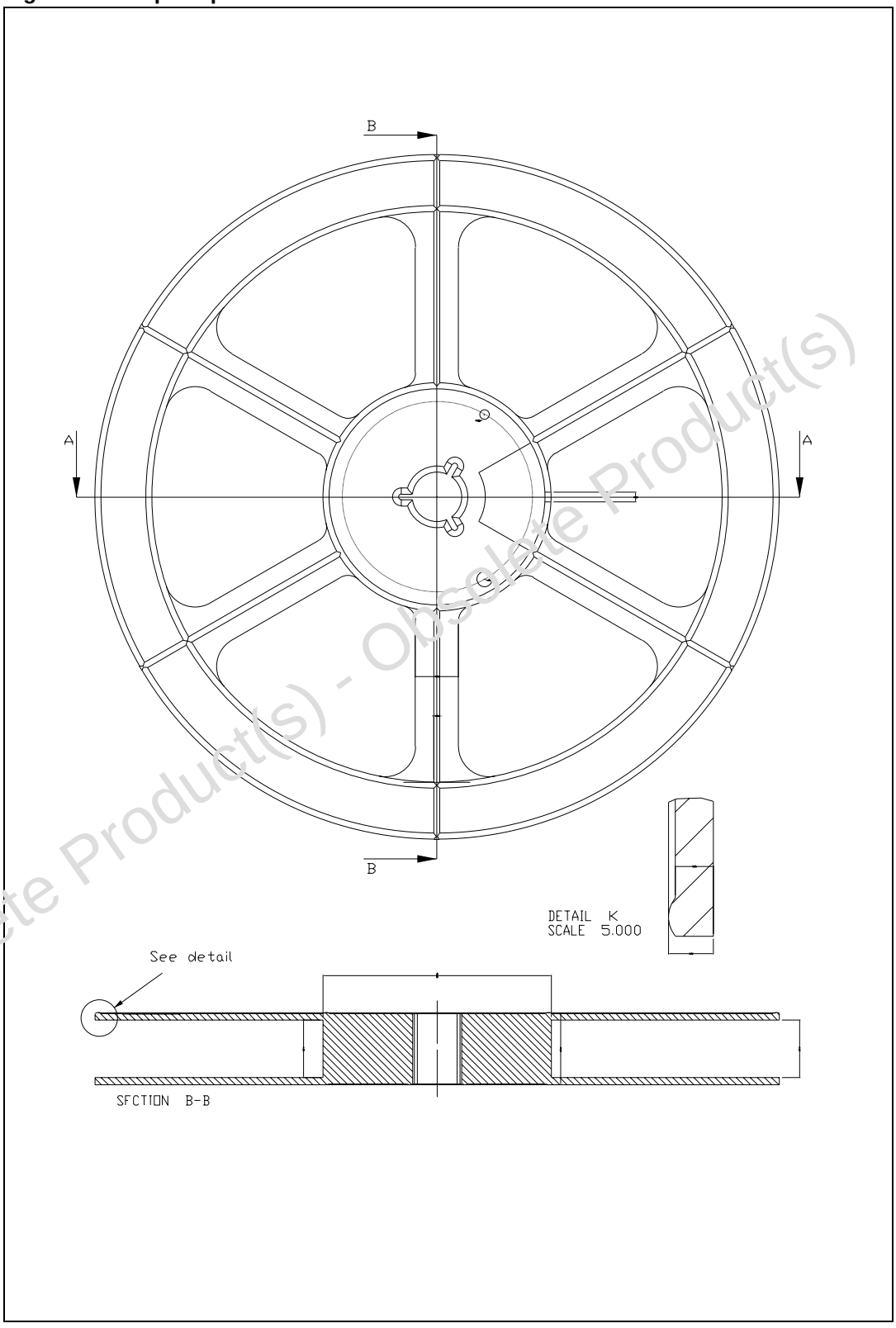
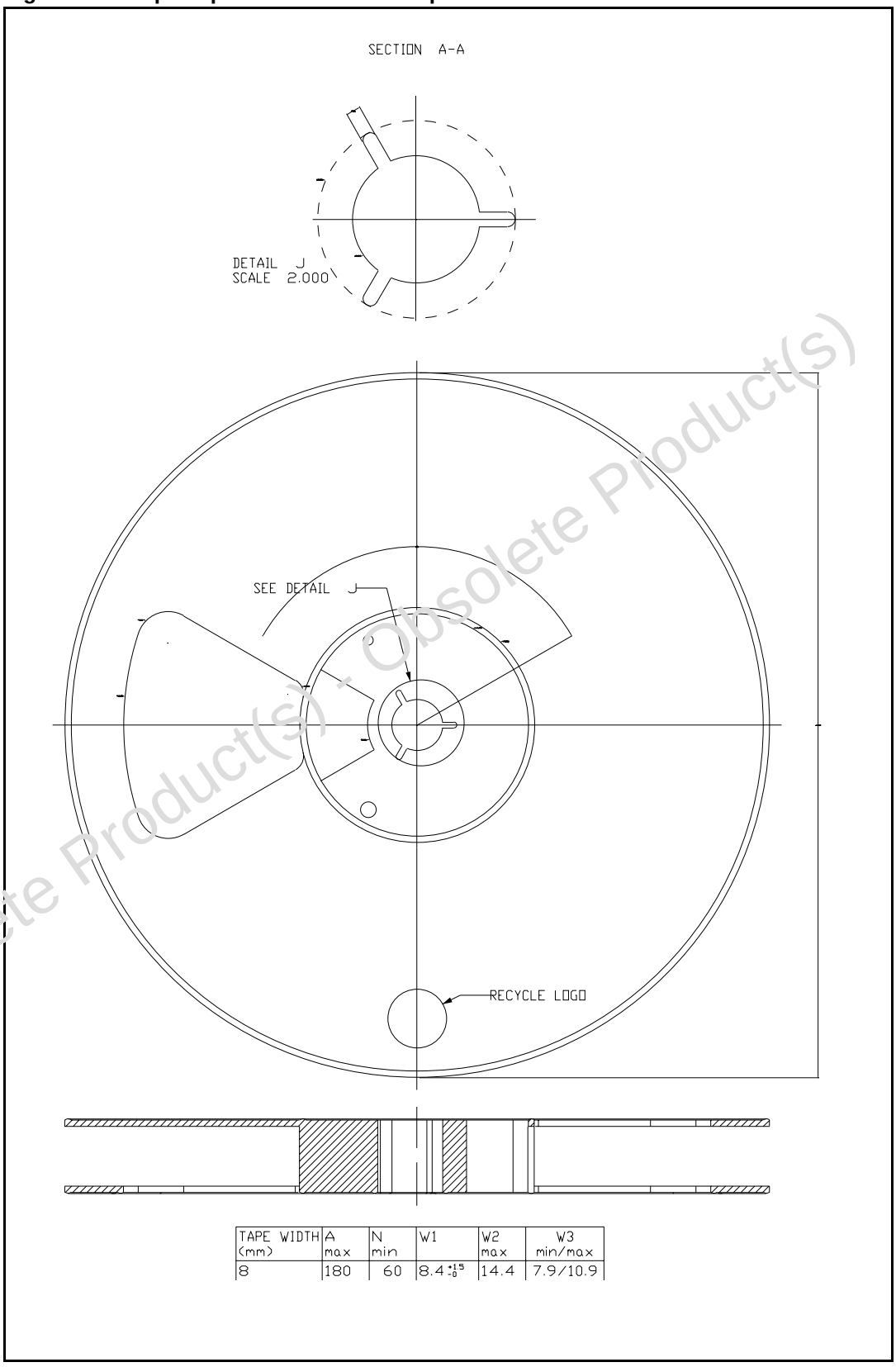


Figure 18. Flip-Chip11 reel for carrier tape information



TAPE WIDTH (mm)	A max	N min	W1	W2 max	W3 min/max
8	180	60	$8.4^{+1.5}_{-0}$	14.4	7.9/10.9

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
03-Oct-2006	1	First release
16-Oct-2006	2	Schematic *Figure 1 on page 3* updated
07-Aug-2007	3	Air discharge ESD rating updated
28-Aug-2007	4	Changed *Figure 16 on page 15*