PIC18F2480/2580/4480/4580

PIC18F2480/2580/4480/4580
Silicon Errata and Data Sheet Clarification

The PIC18F2480/2580/4480/4580 family devices that you have received conform functionally to the current Device Data Sheet (DS39637**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F2480/2580/4480/4580 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B2**).

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F2480/2580/4480/4580 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]		
		A1	B0	B2
PIC18F2480	1AEh			
PIC18F2580	1ACh	1h	2h	4h
PIC18F4480	1AAh			
PIC18F4580	1A8h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F2XXX/4XXXX Family Flash Microcontroller Programming Specification"* (DS39622) for detailed information on Device and Revision IDs for your specific device.

PIC18F2480/2580/4480/4580

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A1	B0	B2
Master Synchro-nous Serial Port (MSSP)	I2C	1.	Slave reception receives incorrect data if not read at the correct time.	X	X	X
Brown-out Reset (BOR)	Trip Level	2.	Trip levels are off at high frequencies.		X	
ECCP	Special Event Trigger	3.	The Special Event Trigger Reset does not occur on the next rollover of the prescaler counter.	X		
EUSART	Transmission	4.	9-bit timing can be corrupted if the TX9D bit is not written immediately after TXIF is set.	X		
Timer1/3	16-Bit Mode	5.	The TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer.	X		
Interrupts	2-Cycle Instruction	6.	If an interrupt occurs during a 2-cycle instruction modifying the STATUS, BSR or WREG register, the previous value is saved to the Fast Return register.	X		
ECAN™ Technol-ogy	Transmit Buffer ID	7.	The first five bits of a transmitted identifier may not match the transmit buffer ID.	X		
ECAN Technology	Error Interruption Flag	8.	The error interrupt flag may not be able to be cleared in software if the TXERRCNT or RXERRCNT counters exceed 127.	X		
ECAN Technology	Configuration Mode	9.	After an error on the bus, the module is unable to switch directly from Listen Only mode to Configuration mode.	X		
ECAN Technology	TXBnSIDH Register	10.	May become corrupted.	X		
ECAN Technology	Listen Only Mode	11.	IRXIF, RXB0IF and RXFUL flags are consistently set after 129 or more consistent error frames.	X		
10-Bit Analog-to-Digital Converter	E_{IL} and E_{DL}	12.	E_{IL} and E_{DL} may exceed data sheet specifications at codes, 511 and 512.	X		
MSSP	SPI	13.	SDO output may change after inactive lock edge of Bit 0.	X		
Timer1/3	Interrupt	14.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B2**).

1. Module: Master Synchronous Serial Port (MSSP)

When configured for I^{2}C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^{2}C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A1	B0	B2					
X	X	X					

2. Module: Brown-out Reset (BOR)

The BOR module may reset above the parameter D005 value specified in **Section 28.1 "DC Characteristics: Supply Voltage"** when:

- BORV<1:0> = 01 or 00
- F$_{OSC}$ is above 26 MHz

The updated BOR voltage specifications are shown in the **Section 28.1** table.

28.1 DC Characteristics: Supply Voltage
PIC18F2480/2580/4480/4580 (Industrial, Extended)
PIC18LF2480/2580/4480/4580 (Industrial)

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
D005	V$_{BOR}$	**Brown-out Reset Voltage**					
		BORV<1:0> = 01	4.47	4.69	4.91	V	F$_{OSC}$ > 26 MHz
		BORV<1:0> = 00	4.72	4.95	5.18	V	F$_{OSC}$ > 26 MHz

Work around

To address this situation:

- Reduce F$_{OSC}$ to 25 MHz
- Use the lower of the two affected BOR voltage thresholds, BORV<1:0> (CONFIG2L<4:3>) = 01

This will ensure detection of V$_{DD}$ below 5.0V.

Affected Silicon Revisions

A1	B0	B2					
	X						

3. Module: ECCP

When operating either Timer1 or Timer3 as a counter, with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits, CCP1M<3:0> = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F458, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter, after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period as the PIC18F458 devices, for a given clock source, add 1 to the value in CCPR1H:CCPR1L. If CCPR1H:CCPR1L = x for the PIC18F458, achieve the same Reset period on a PIC18F2480/2580/4480/4580 device by using CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 (depending on the T1CKPS<1:0> bit values).

Affected Silicon Revisions

A1	B0	B2					
X							

4. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a Reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine. Alternately, only write to TX9D when a transmission is not in progress (TRMT = 1).

Affected Silicon Revisions

A1	B0	B2					
X							

5. Module: Timer1/3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H were written. It does not change the actual prescale value.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

Affected Silicon Revisions

A1	B0	B2					
X							

6. Module: Interrupts

If an interrupt occurs during a 2-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (shadow) register. Upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high-priority interrupt occurs during the instruction, MOVFF TEMP, WREG, the MOVFF instruction will be completed and WREG will be loaded with the value of TEMP before branching to the ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG.

This results in WREG containing the value it had before execution of MOVFF TEMP, WREG.

Affected instructions are:

```
MOVFF  Fs, Fd
```
Where Fd is WREG, BSR or STATUS

```
MOVSF  Zs, Fd
```
Where Fd is WREG, BSR or STATUS

```
MOVSS  [Zs], [Zd]
```
Where the destination is WREG, BSR or STATUS

Work around

1. Assembly Language Programming:

   If any 2-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the RETFIE FAST instruction to return from the interrupt. Instead, save and then restore WREG, BSR and STATUS via software, as shown in Example 8-1 in the Device Data Sheet.

   Alternatively, in the case of MOVFF, use the MOVF instruction to write to WREG instead. For example:

   Use

   ```
   MOVF    TEMP, W
   MOVWF   BSR
   ```

   Instead of

   ```
   MOVFF TEMP, BSR
   ```

   As another alternative, the work-around in Example 1 can be used. This example overwrites the Fast Return register by making a dummy call to Foo with the fast option in the high-priority service routine.

EXAMPLE 1: ASSEMBLY LANGUAGE INTERRUPT SERVICE

```
ISR @ 0x0008
    CALL       Foo, FAST  ; store current value of WREG, BSR, STATUS for a second time
Foo:
    POP                   ; clears return address of Foo call
    :                     ; insert high priority ISR code here
    :
    RETFIE     FAST
```

2. C Language Programming:

The exact work-around depends on the compiler in use. Consult the C compiler's documentation for details.

If using the Microchip MPLAB® C18 C Compiler, define both high and low-priority interrupt handler functions as "low priority" by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high-priority interrupt bit is set in the IPRx register, the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

The code segment, shown in Example 2, demonstrates the work around using the C18 compiler.

EXAMPLE 2:   INTERRUPT SERVICE ROUTINE IN C

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

An optimized C18 version, illustrating how to reduce the instruction cycle count to three, is provided in Example 3.

Affected Silicon Revisions

A1	B0	B2					
X							

EXAMPLE 3:   OPTIMIZED INTERRUPT SERVICE ROUTINE

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
  _asm
    CALL high_vector_branch, 1
  _endasm
}

void high_vector_branch (void)
{
  _asm
    POP
    GOTO high_isr
  _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
  ...
}
```

7. Module: ECAN™ Technology

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the Transmit Buffer ID register, TXBnSIDH. The following conditions must exist for the corruption to occur:

- A transmit message must be pending
- The ECAN module must detect a Start-of-Frame (SOF) in the third bit of the interframe space.

Work around

None.

Affected Silicon Revisions

A1	B0	B2					
X							

8. Module: ECAN Technology

The Error Interrupt Flag, ERRIF (PIR3<5>), may not be able to be cleared in software after either of the following counter registers exceeds 127:

- Transmit Error Counter Register (TXERRCNT)
- Receive Error Counter Register (RXERRCNT)

Work around

Monitor the EWARN (COMSTAT<0>) bit to determine if either the TXERRCNT or the RXERRCNT exceeds 95 and clear the ERRIF flag before either counter reaches 127.

Affected Silicon Revisions

A1	B0	B2					
X							

9. Module: ECAN Technology

Following an error on the bus, the ECAN module is unable to switch from Listen Only mode directly to Configuration mode.

Work around

Use the REQOP (CANCON<7:5>) bits to select Normal mode as an intermediate step when switching from Listen Only mode to Configuration mode.

Affected Silicon Revisions

A1	B0	B2					
X							

10. Module: ECAN Technology

Under specific conditions, the TXBnSIDH register of the pending message for transmission may be corrupted. This occurs when the following conditions exist:

- A transmit message is pending.
- All of the receive buffers are full and a received message is in the Message Assembly Buffer (MAB).
- A receive buffer is made available (RXFUL (RXBxCON<7>) set to '0') at either of the following times:
  - When a Start-of-Frame (SOF) is recognized on the CAN bus
  - On the instruction cycle prior to the SOF

The timing of this event is crucial.

Work around

Ensure that a receive buffer overflow condition does not occur and/or ensure that a transmit request is not pending if a receive buffer overflow condition does exist.

The pseudo code segment in Example 4 is an example of how to disable a pending transmission. This code is for illustration purposes only.

Affected Silicon Revisions

A1	B0	B2					
X							

EXAMPLE 4: DISABLING A PENDING TRANSMISSION

```
If (RXBnOVFL == 1)                       // Has an overflow occurred?
    {       If (TXREQ == 1)              // Is a transmission pending?
            {       TXREQ = 0;           // Clear transmit request
                    If (TXABT == 1)      // Store transmission aborted status value
                            MyFlag = 1;
            }
    }
    Temp_RXREG = RXBx;                   // Read receive buffer
    If (MyFlag)                          // Was previous transmission aborted?
    {       TXREQ = 1;                   // Set transmit request
            MyFlag = 0;                  // Reset stored transmission aborted status
    }
```

PIC18F2480/2580/4480/4580

11. Module: ECAN Technology

In Listen Only mode, the module may persistently set the IRXIF and RXB0IF interrupt flags, and the RXFUL status flag, after receiving 129 or more consecutive error frames. In this case, the flags can be cleared, but then will become set again immediately and continuously without receiving a bus message.

Work around

Place the ECAN module in Configuration mode before receiving 129 consecutive error frames and then place it back into Listen Only mode.

Affected Silicon Revisions

A1	B0	B2					
X							

12. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 T_{OSC} or RC (when ADCS<2:0> = 000 or x11), in extremely rare cases, the E_{IL} (Integral Linearity Error) and E_{DL} (Differential Linearity Error) may exceed the data sheet specifications at codes, 511 and 512 only.

Work around

Select the AD clock source as 4 T_{OSC}, 8 T_{OSC}, 16 T_{OSC}, 32 T_{OSC} or 64 T_{OSC} and avoid selecting 2 T_{OSC} or RC.

Affected Silicon Revisions

A1	B0	B2					
X							

13. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the Bit 0 output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

Work around

None.

Affected Silicon Revisions

A1	B0	B2					
X							

14. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 5.

EXAMPLE 5:   ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;           //Stop timer from incrementing
PIE1bits.TMR1IE = 0;            //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                   //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;           //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);            //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A1	B0	B2					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39637**D**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Packaging Information

The "Pin 1" dot on the 28-Lead QFN package, in the Package Marking Information section, is incorrectly placed. The correct placement is indicated in **Section 29.1 "28-Lead QFN Package Marking Information"** below:

29.1 28-Lead QFN Package Marking Information
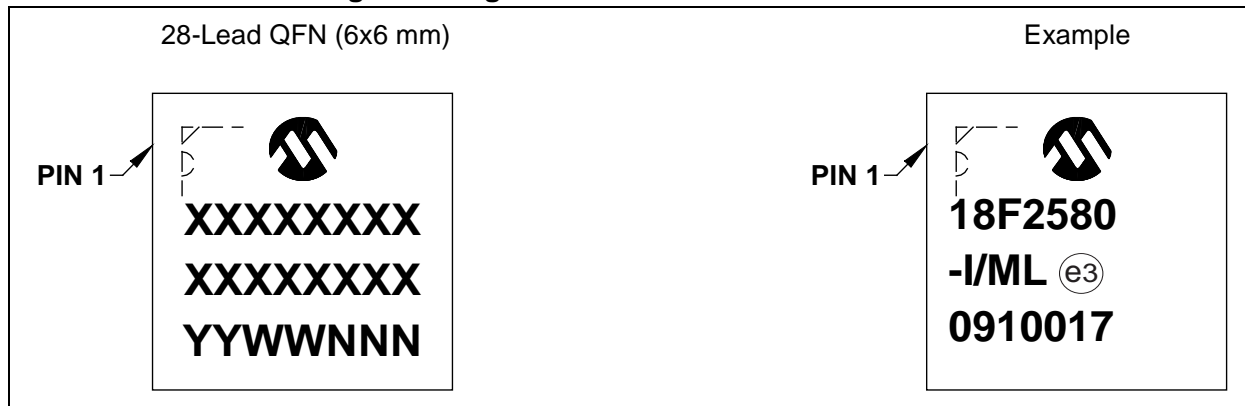
APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2010)

Original release of this errata, combining previous errata for silicon revisions, A1 and B0, and superseding the data sheet errata. Added the B2 silicon revision, which had no issues. No data sheet issues were included as they had been resolved with a data sheet revision.

This document replaces these errata documents:

- DS80419B, *"PIC18F2480/2580/4480/4580 Rev. B0 Silicon Errata"*
- DS80219E, *"PIC18F2480/2580/4480/4580 Rev. A1 Silicon Errata"*
- DS80267C, *"PIC18F2480/2580/4480/4580 Data Sheet Errata"*

Rev B Document (3/2010)

Corrected an erroneous silicon revision reference in the revision history.

Rev C Document (3/2010)

Removed issue #1 from the document and renumbered the previous issues 2-14. Added B2 silicon as being affected by issue 1 (formerly 2) and removed A1 silicon from issue 2 (formerly 3).

Rev D Document (7/2014)

Updated errata to new format; Added MPLAB X IDE; Added Module 14, Timer1/3, to Silicon Errata Issues section.

Rev D Document (4/2016)

Added Module 1, Package Marking Information, to the Data Sheet Clarifications section. Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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