IRFR3707ZPbF
IRFU3707ZPbF

HEXFET® Power MOSFET

Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
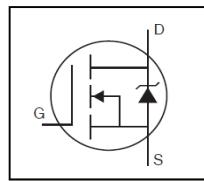
V_{DSS}	30V
$R_{DS(on)}$ max	9.5mΩ
Qg	9.6nC

D- Pak
IRFR3707ZPbF

I- Pak
IRFU3707ZPbF

G	D	S
Gate	Drain	Source
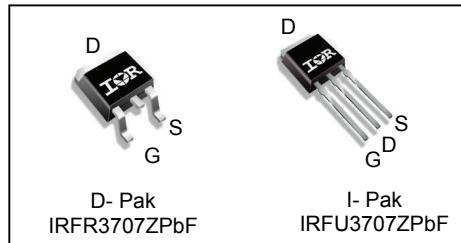
Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra - Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	**Quantity**	
IRFU3707ZPbF	I-Pak	Tube	75	IRFU3707ZPbF
IRFR3707ZPbF	D-Pak	Tube	75	IRFR3707ZPbF
		Tape and Reel Left	3000	IRFR3707ZTRLPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain -to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	56④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	39④	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Maximum Power Dissipation	50	W
P_D @T_C = 100°C	Maximum Power Dissipation	25	W
	Linear Derating Factor	0.33	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Notes ① through ⑤ are on page 2.

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Static @ T$_J$ = 25°C (unless otherwise specified)

Parameter		Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔV$_{(BR)DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.023	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	7.5	9.5	mΩ	V$_{GS}$ = 10V, I$_D$ = 15A ③
		——	10	12.5		V$_{GS}$ = 4.5V, I$_D$ = 12A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 25µA
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Temp. Coefficient	——	-5.0	——	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	1.0	µA	V$_{DS}$ = 24V, V$_{GS}$ = 0V
		——	——	150		V$_{DS}$ = 24V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——		-100		V$_{GS}$ = -20V
gfs	Forward Trans conductance	71	——	——	S	V$_{DS}$ = 15V, I$_D$ = 12A
Q$_g$	Total Gate Charge	——	9.6	14	nC	V$_{DS}$ = 15V V$_{GS}$ = 4.5V I$_D$ = 12A See Fig. 16
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	——	2.6	——		
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	——	0.90	——		
Q$_{gd}$	Gate-to-Drain Charge	——	3.5	——		
Q$_{godr}$	Gate Charge Overdrive	——	2.6	——		
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	——	4.4	——		
Q$_{oss}$	Output Charge	——	5.8	——	nC	V$_{DS}$ = 15V, V$_{GS}$ = 0V
t$_{d(on)}$	Turn-On Delay Time	——	8.0	——	ns	V$_{DD}$ = 16V, V$_{GS}$ = 4.5V ③ I$_D$ = 12A Clamped Inductive Load
t$_r$	Rise Time	——	11	——		
t$_{d(off)}$	Turn-Off Delay Time	——	12	——		
t$_f$	Fall Time	——	3.3	——		
C$_{iss}$	Input Capacitance	——	1150	——	pF	V$_{GS}$ = 0V V$_{DS}$ = 15V ƒ = 1.0MHz
C$_{oss}$	Output Capacitance	——	260	——		
C$_{rss}$	Reverse Transfer Capacitance	——	120	——		

Avalanche Characteristics

Parameter		Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy ②	42	mJ
I$_{AR}$	Avalanche Current ①	12	A
E$_{AR}$	Repetitive Avalanche Energy ①	5.0	mJ

Diode Characteristics

Parameter		Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	56④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	220		
V$_{SD}$	Diode Forward Voltage	——	——	1.0	V	T$_J$ = 25°C, I$_S$ = 12A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	25	38	ns	T$_J$ = 25°C, I$_F$ = 12A, V$_{DS}$ = 15V di/dt = 100A/µs ③
Q$_{rr}$	Reverse Recovery Charge	——	17	26	nC	
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L$_S$+L$_D$)				
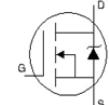
Notes:

① Repetitive rating; pulse width limited by max. junction temperature

② starting T$_J$ = 25°C, L = 0.58mH, R$_G$ = 25Ω, I$_{AS}$ = 12A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics


Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance
vs. Temperature
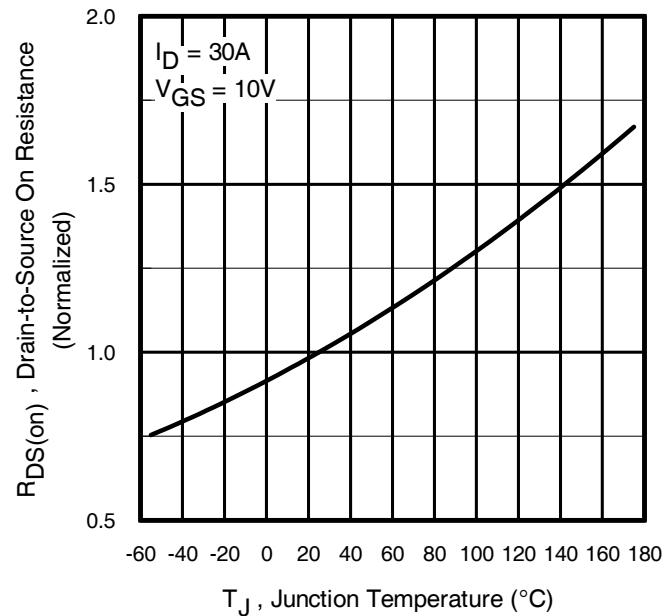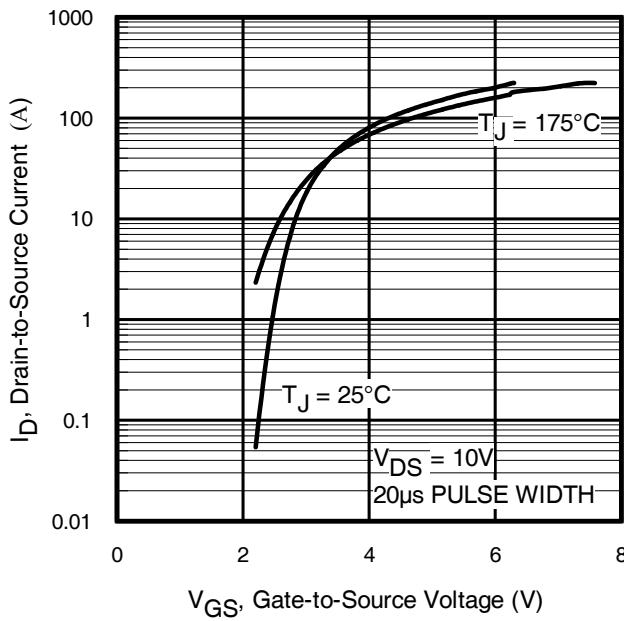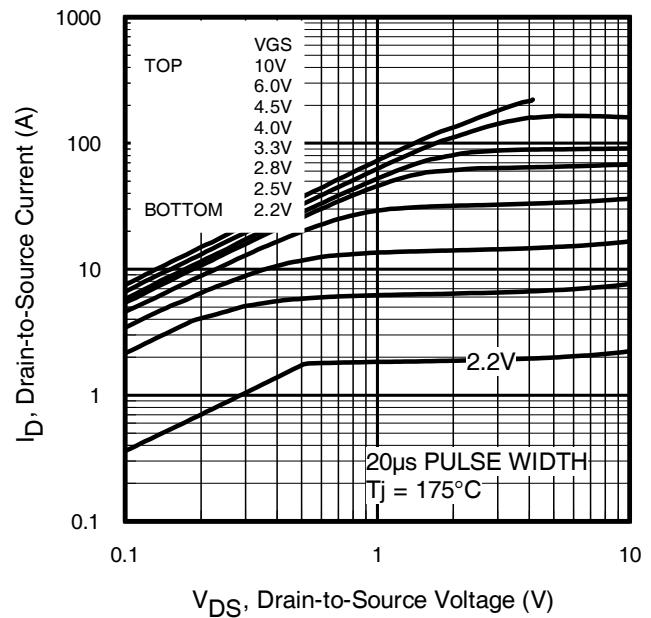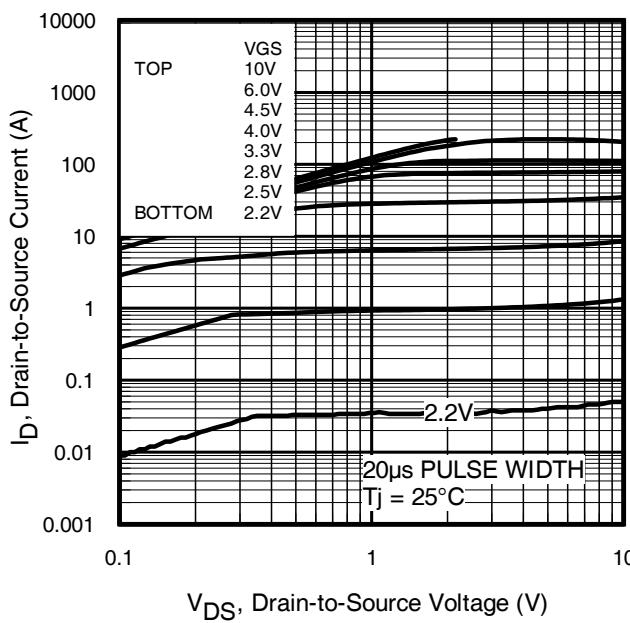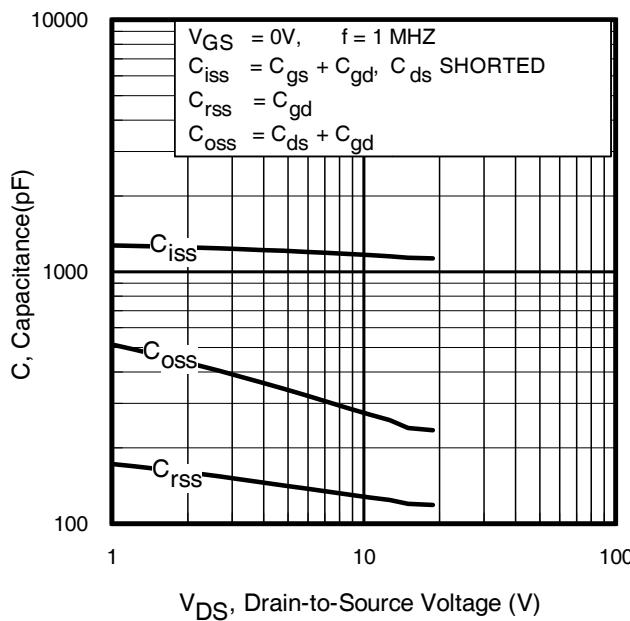
Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage
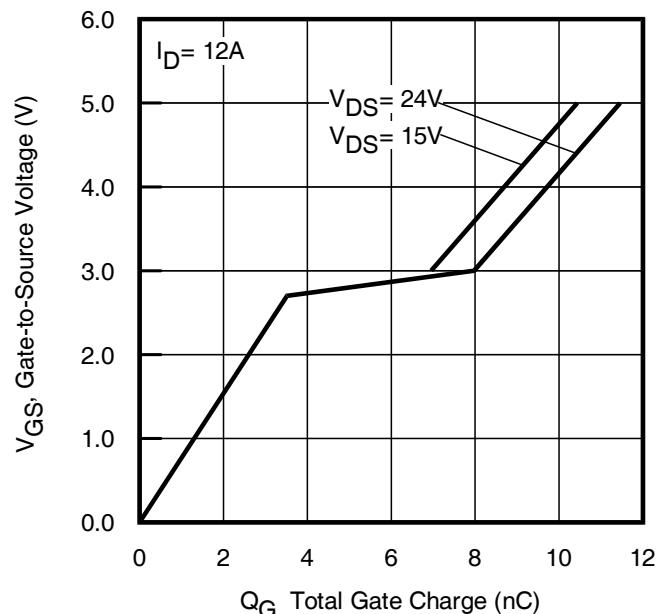
Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage
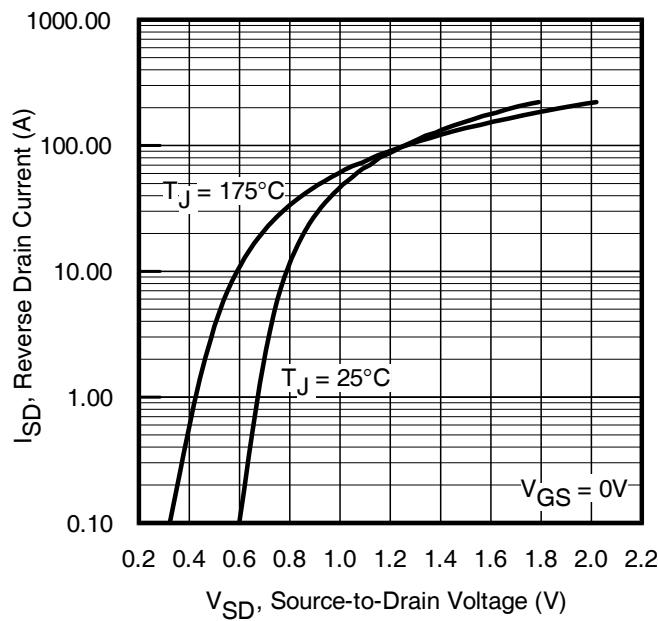
Fig. 7 Typical Source-to-Drain Diode
Forward Voltage
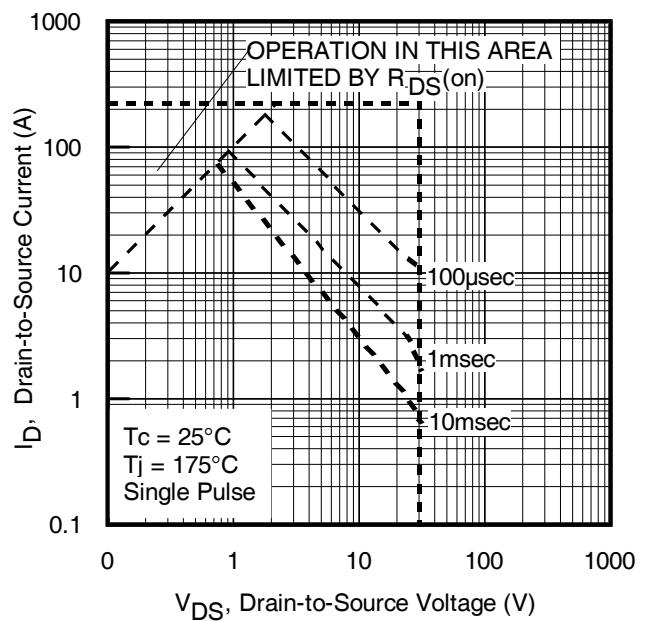
Fig 8. Maximum Safe Operating Area
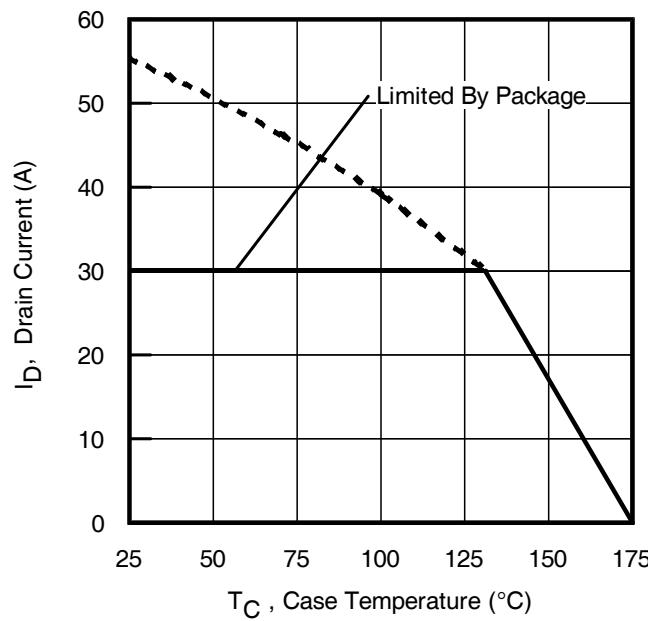
Fig 9. Maximum Drain Current vs. Case Temperature
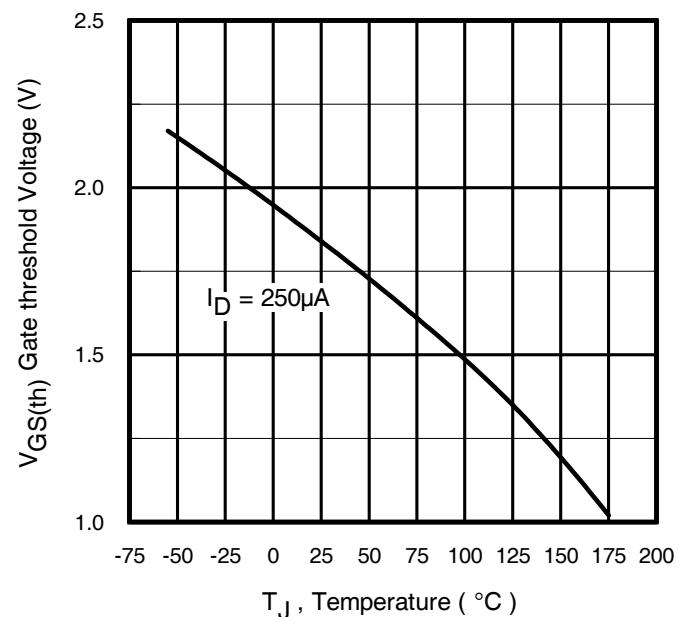
Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τi (sec)
0.823	0.000128
1.698	0.000845
0.481	0.016503

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

SINGLE PULSE
(THERMAL RESPONSE)

$C_i = \tau_i / R_i$
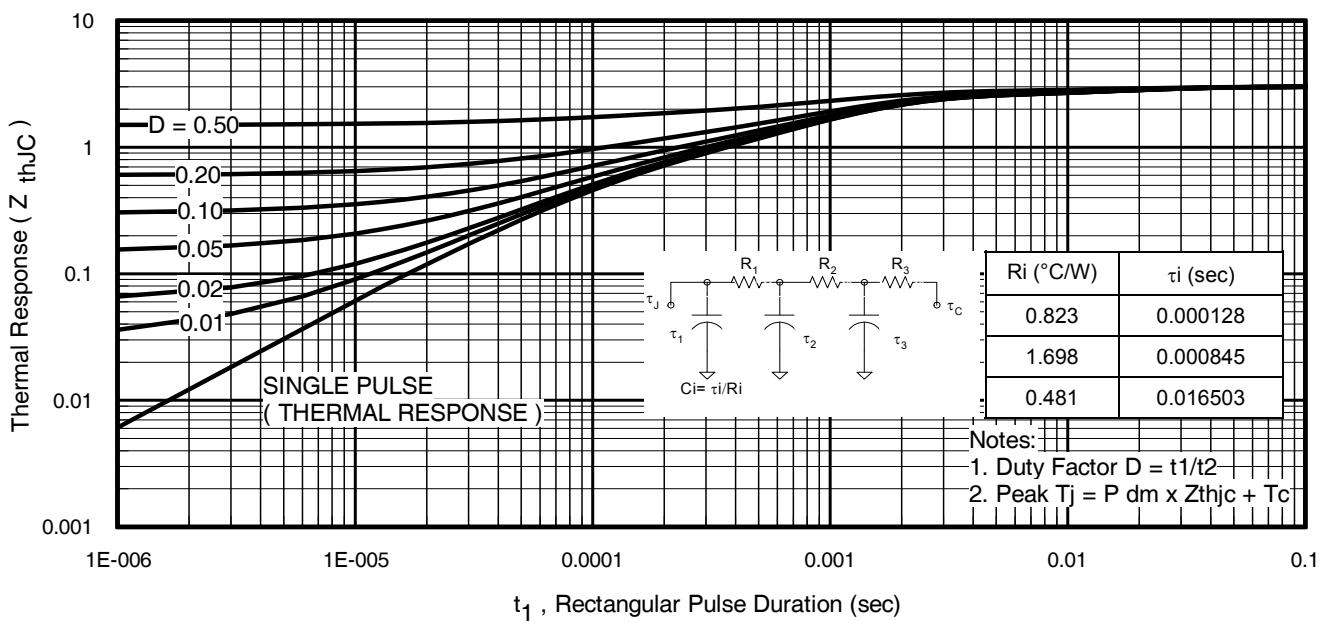
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
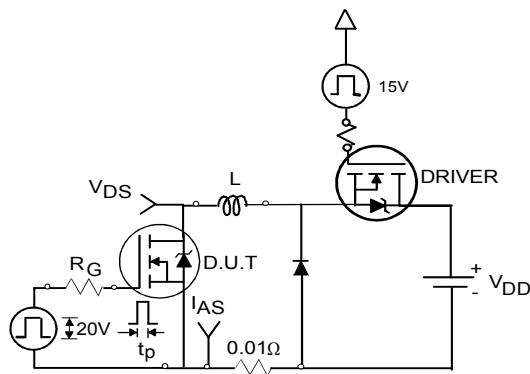
Fig 12a. Unclamped Inductive Test Circuit
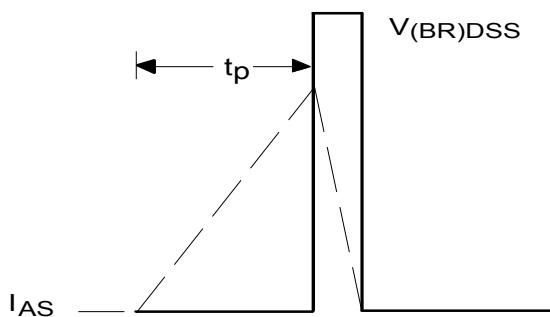
Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform
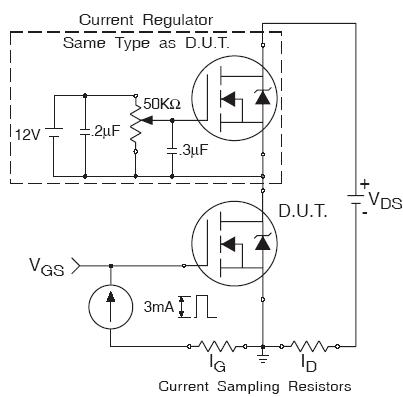
Fig 13b. Gate Charge Test Circuit

**Fig 12c.** Maximum Avalanche Energy
vs. Drain Current
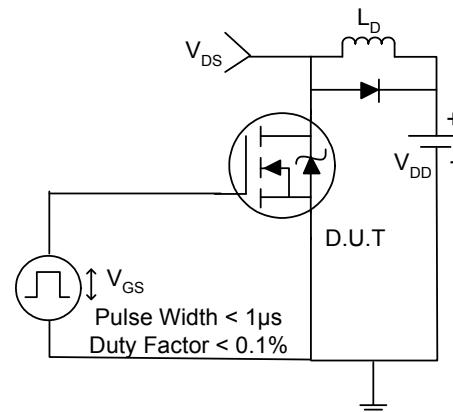
Fig 14a. Switching Time Test Circuit
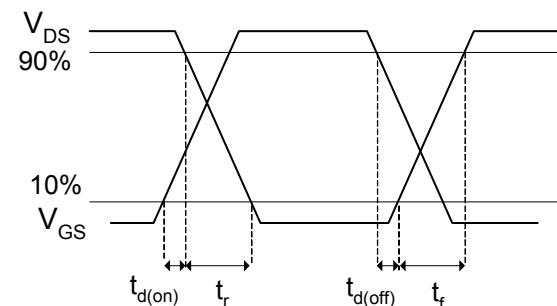
Fig 14b. Switching Time Waveforms

2016-5-31

Peak Diode Recovery dv/dt Test Circuit

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

③

②

④

R_G

+ V_{DD} -

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

① Driver Gate Drive

P.W. — Period — $D = \dfrac{P.W.}{Period}$

$V_{GS}=10V^*$

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current
di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right)$$
$$+ \left(Q_g \times V_g \times f\right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a subelement of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to Id max at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependent (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$
$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right)$$
$$+ \left(Q_g \times V_g \times f\right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control I_C so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to $C_{dv/dt}$ turn on.
The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and Vin. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitive coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for $C_{dv/dt}$ turn on.
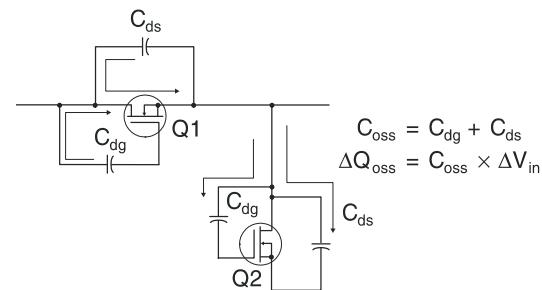

Figure A: Q_{oss} Characteristic

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))
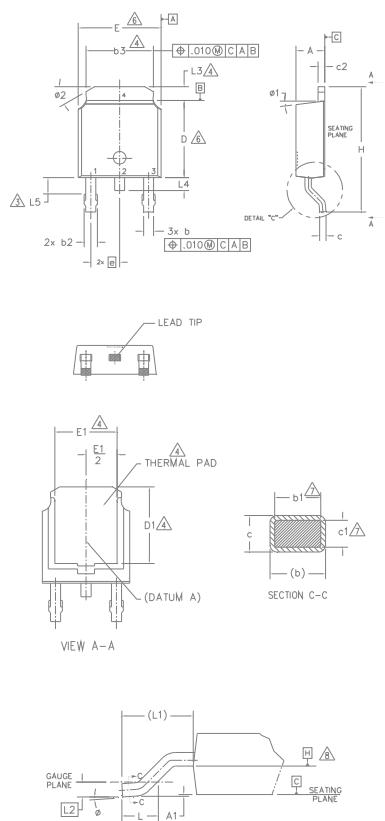
NOTES:
1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION UNCONTROLLED IN L5.
4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBT & CoPAK
1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

"P̄" in assembly line position indicates
"Lead-Free" qualification to the consumer-level

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 1 = 2001
WEEK 16
LINE A

ASSEMBLY LOT CODE

OR

INTERNATIONAL RECTIFIER LOGO

ASSEMBLY LOT CODE

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)

P̄ = DESIGNATES LEAD-FREE PRODUCT QUALIFIED TO THE CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001
WEEK 16
A = ASSEMBLY SITE CODE
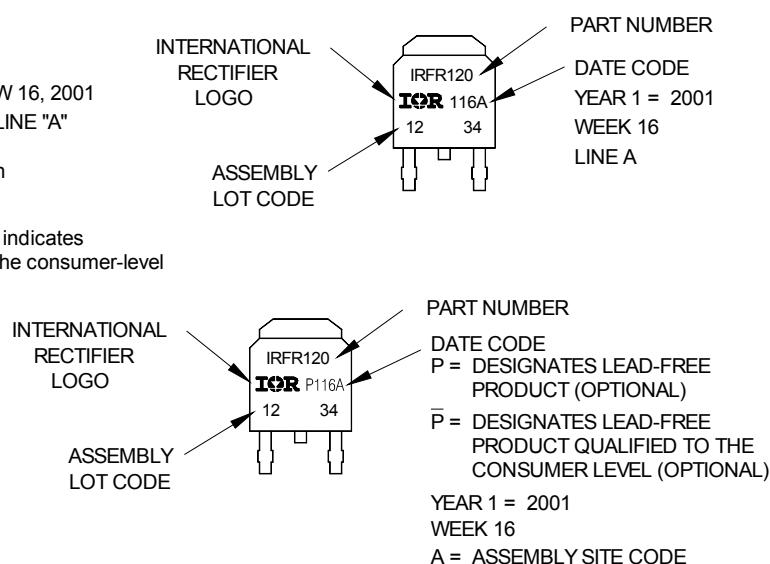
Note: For the most current drawing please refer to Infineon's web site www.infineon.com

I-Pak (TO-251AA) Package Outline Dimensions are shown in millimeters (inches)
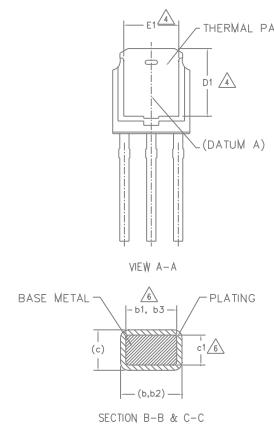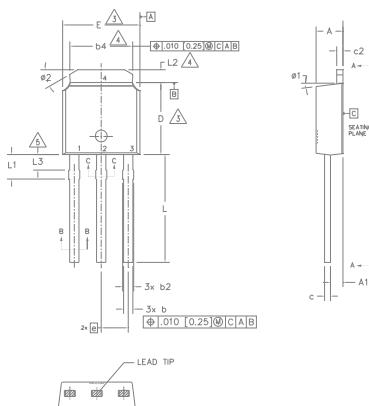
NOTES:

1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

5.- LEAD DIMENSION UNCONTROLLED IN L3.

6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).

8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	3
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	0.89	1.52	.035	.060	5
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates Lead-Free"

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 1 = 2001
WEEK 19
LINE A

ASSEMBLY LOT CODE

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 1 = 2001
WEEK 19
A = ASSEMBLY SITE CODE

ASSEMBLY LOT CODE
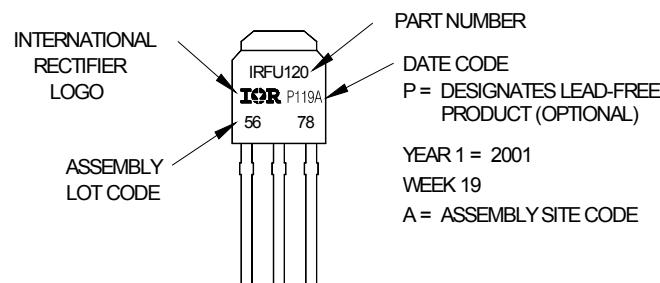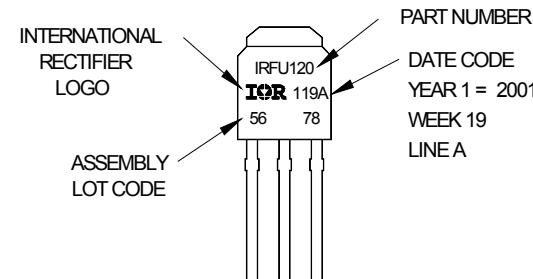
Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)

TR

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

TRR   TRL

16.3 (.641)
15.7 (.619)

8.1 (.318)
7.9 (.312)

FEED DIRECTION
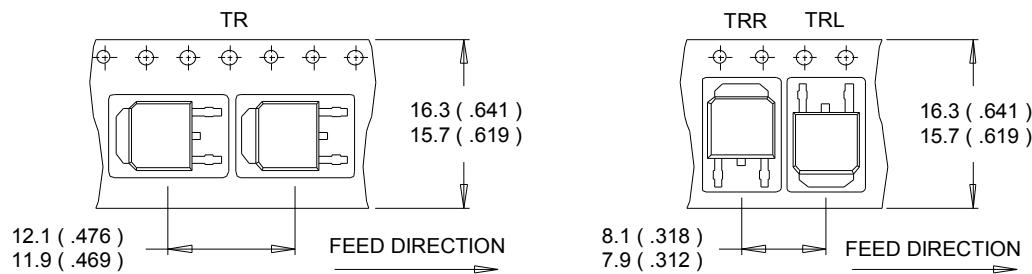
NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

⌀ 13 INCH

16 mm
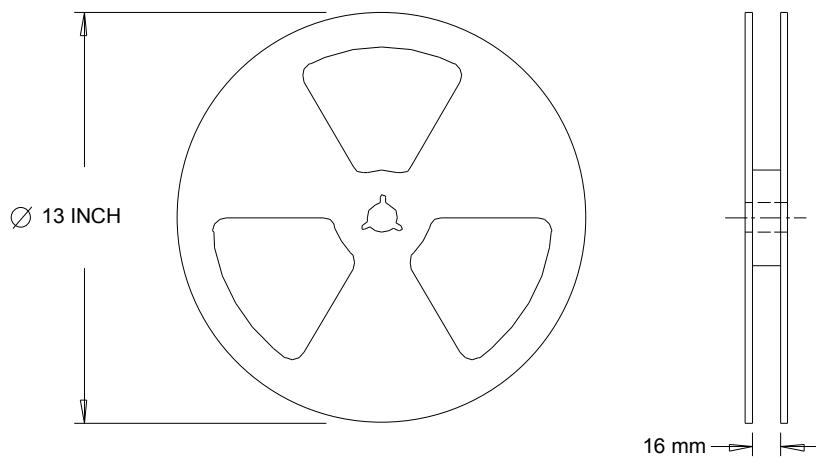
NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

2016-5-31

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D-Pak	MSL1
	I-Pak	(per JEDEC J-STD-020D) ††
RoHS Compliant	Yes	

†   Qualification standards can be found at Infineon's web site www.infineon.com

††   Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
5/31/2016	• Updated datasheet with corporate template. • Added disclaimer on last page.

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Trademarks updated November 2015

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