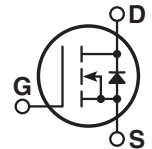
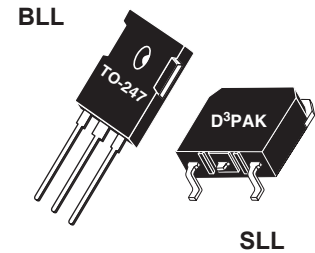


POWER MOS 7 MOSFET

Power MOS 7[®] is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7[®] by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7[®] combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT10090	UNIT
V_{DSS}	Drain-Source Voltage	1000	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	12	Amps
I_{DM}	Pulsed Drain Current ¹	48	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	298	Watts
	Linear Derating Factor	2.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ¹ (Repetitive and Non-Repetitive)	12	Amps
E_{AR}	Repetitive Avalanche Energy ¹	30	mJ
E_{AS}	Single Pulse Avalanche Energy ⁴	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	1000			Volts
$I_{D(on)}$	On State Drain Current ² ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	12			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ² ($V_{GS} = 10V, 6A$)			0.95	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1000V, V_{GS} = 0V$)			100	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 800V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT10090BLL - SLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		1969		pF
C _{oss}	Output Capacitance			332		
C _{rss}	Reverse Transfer Capacitance			55		
Q _g	Total Gate Charge ³	V _{GS} = 10V V _{DD} = 500V I _D = 12A @ 25°C		71		nC
Q _{gs}	Gate-Source Charge			12		
Q _{gd}	Gate-Drain ("Miller") Charge			47		
t _{d(on)}	Turn-on Delay Time	RESISTIVE SWITCHING V _{GS} = 15V V _{DD} = 500V I _D = 12A @ 25°C R _G = .6Ω		9		ns
t _r	Rise Time			5		
t _{d(off)}	Turn-off Delay Time			23		
t _f	Fall Time ≤			4		
E _{on}	Turn-on Switching Energy ⁶	INDUCTIVE SWITCHING @ 25°C V _{DD} = 670V, V _{GS} = 15V I _D = 12A, R _G = 5Ω		334		μJ
E _{off}	Turn-off Switching Energy			77		
E _{on}	Turn-on Switching Energy ⁶	INDUCTIVE SWITCHING @ 125°C V _{DD} = 670V, V _{GS} = 15V I _D = 12A, R _G = 5Ω		672		
E _{off}	Turn-off Switching Energy			100		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			12	Amps
I _{SM}	Pulsed Source Current ¹ (Body Diode)			48	
V _{SD}	Diode Forward Voltage ² (V _{GS} = 0V, I _S = -I _D 12A)			1.3	Volts
t _{rr}	Reverse Recovery Time (I _S = -I _D 12A, di _S /dt = 100A/μs)		700		ns
Q _{rr}	Reverse Recovery Charge (I _S = -I _D 12A, di _S /dt = 100A/μs)		9.0		μC
dv _{dt}	Peak Diode Recovery ⁵ dv _{dt}			10	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.42	°C/W
R _{θJA}	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 16.81mH, R_G = 25Ω, Peak I_L = 12A

⑤ dv_{dt} numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -I_D 12A di_S/dt ≤ 700A/μs V_R ≤ V_{DSS} T_J ≤ 150°C

⑥ Eon includes diode reverse recovery measured in accordance with JEDEC standard JESD24-1. See figures 18, 20.

Microsemi Reserves the right to change, without notice, the specifications and information contained herein.

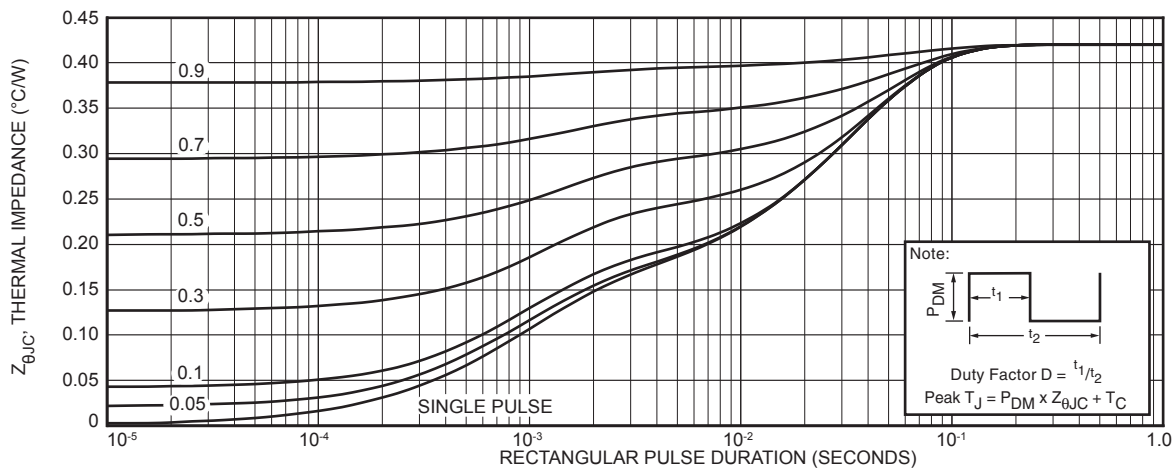
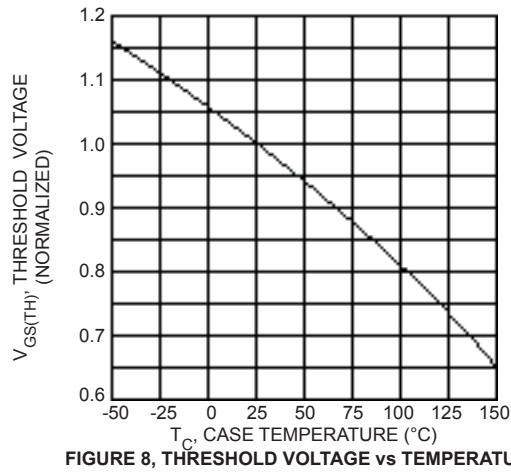
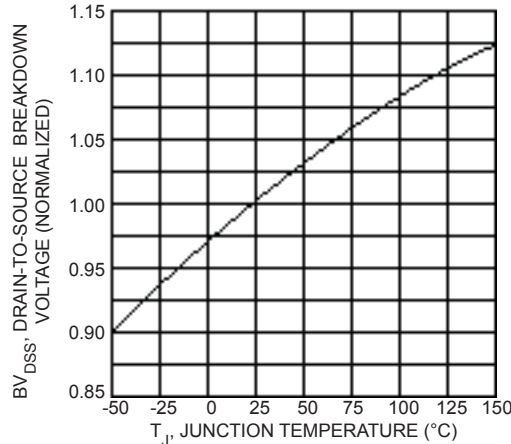
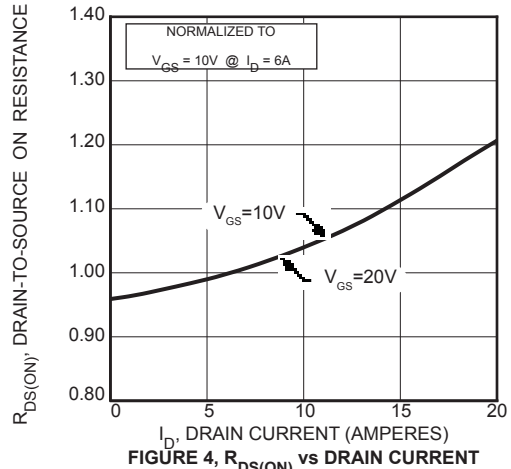
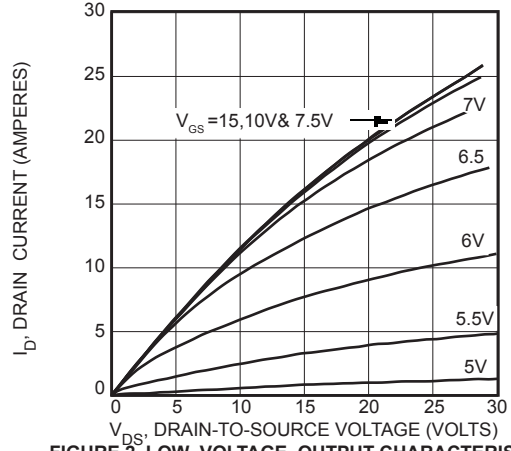
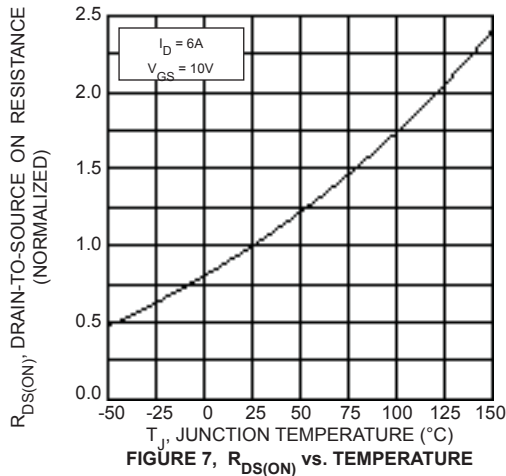
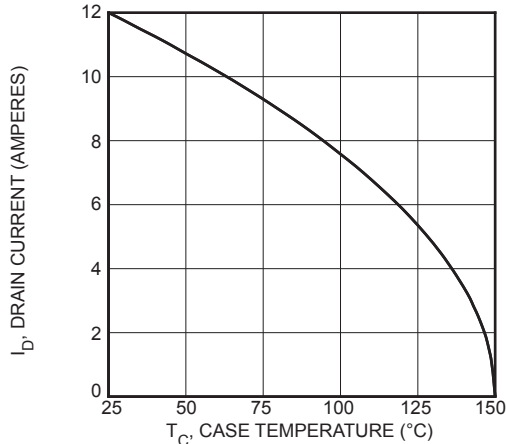
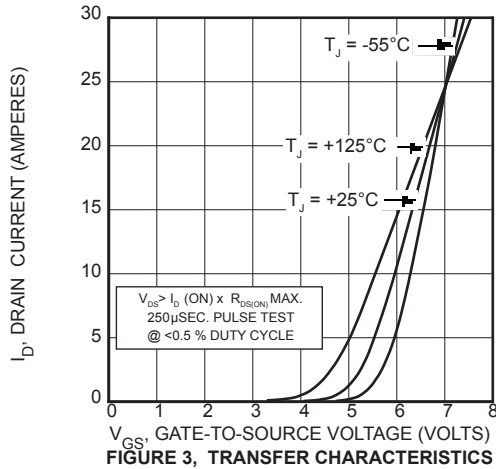


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT10090BLL - SLL



Typical Performance Curves

APT10090BLL - SLL

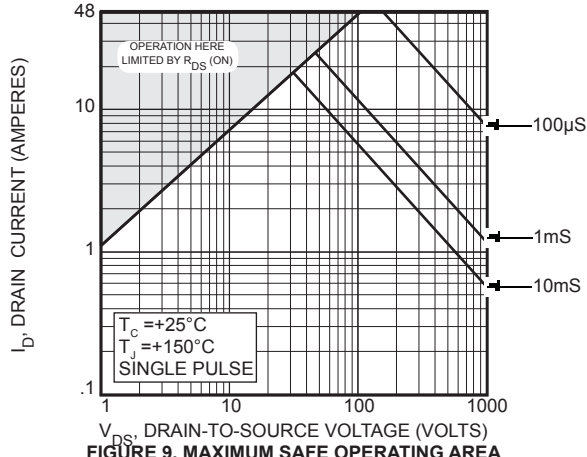


FIGURE 9, MAXIMUM SAFE OPERATING AREA

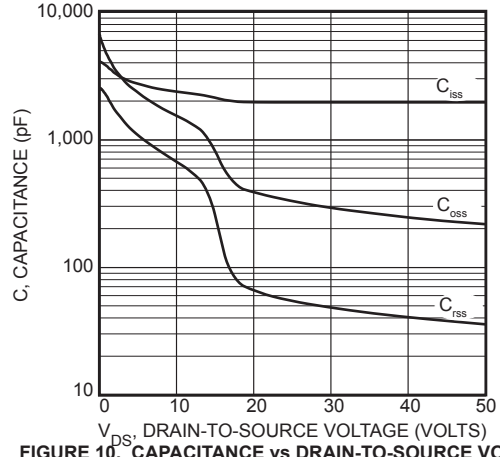


FIGURE 10, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

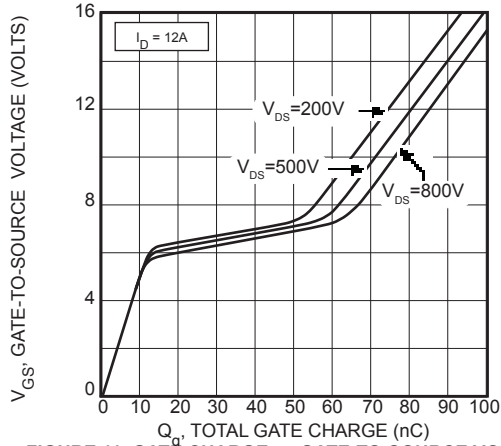


FIGURE 11, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

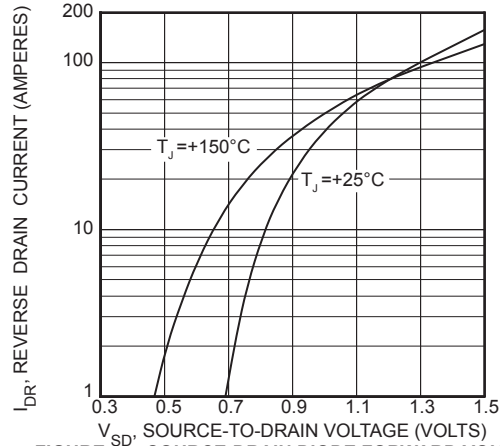


FIGURE 12, SOURCE-DRAIN DIODE FORWARD VOLTAGE

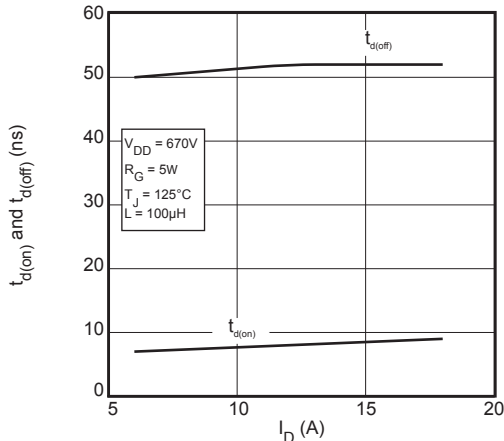


FIGURE 13, DELAY TIMES vs CURRENT

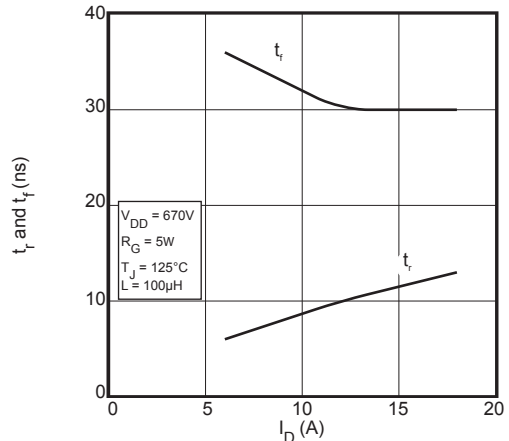


FIGURE 14, RISE AND FALL TIMES vs CURRENT

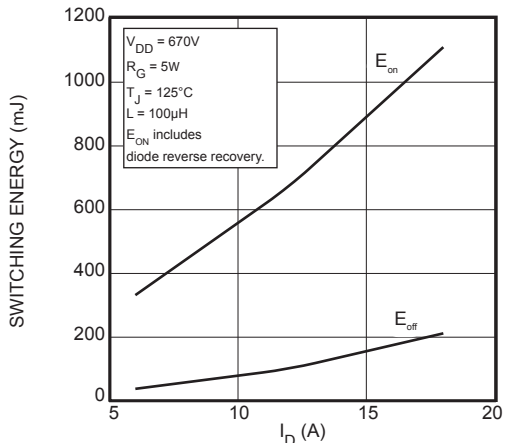


FIGURE 15, SWITCHING ENERGY vs CURRENT

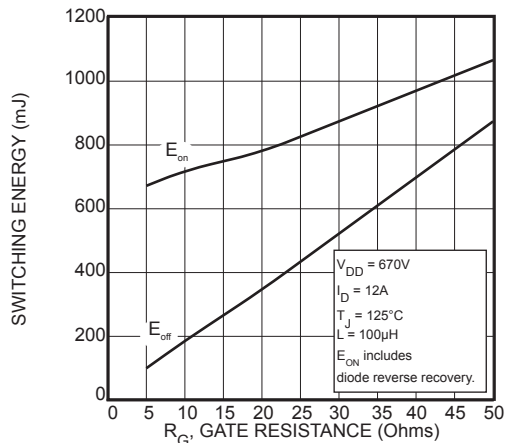


FIGURE 16, SWITCHING ENERGY vs. GATE RESISTANCE

Typical Performance Curves

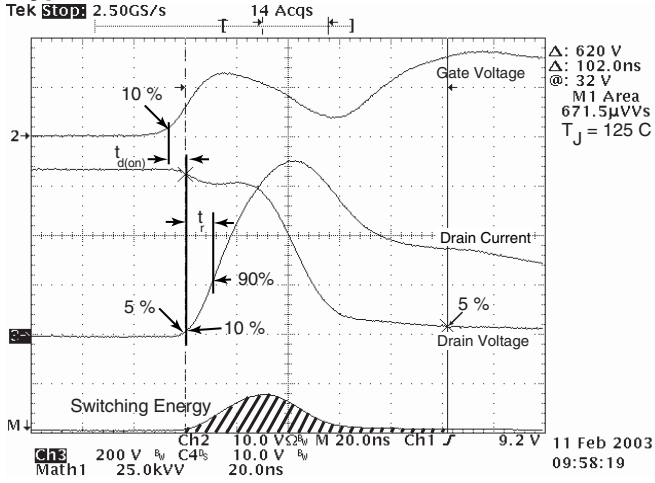


Figure 17, Turn-on Switching Waveforms and Definitions

APT10090BLL - SLL

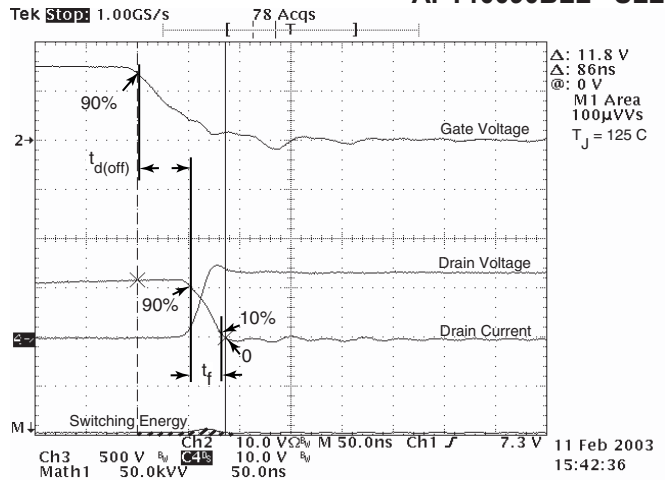


Figure 18, Turn-off Switching Waveforms and Definitions

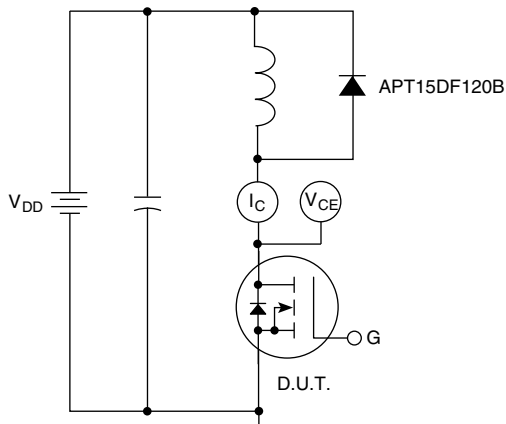
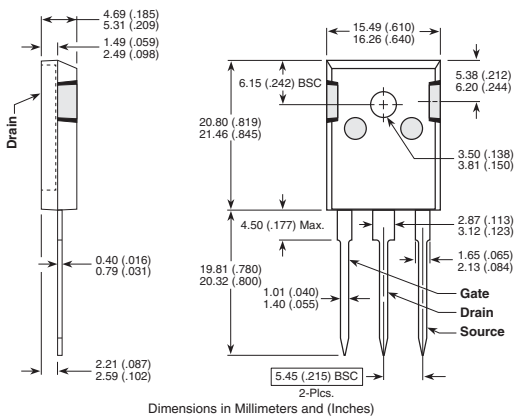


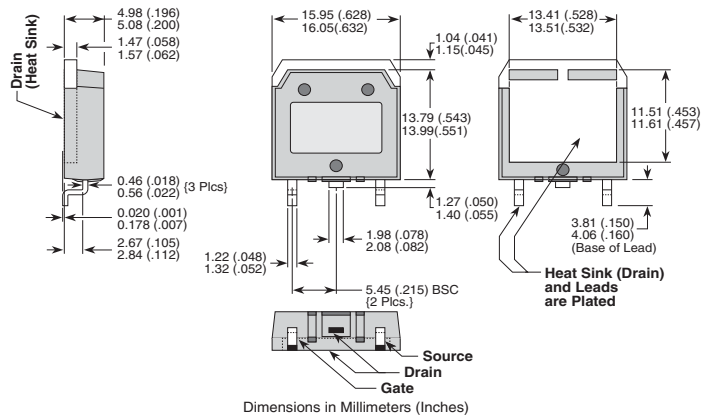
Figure 19, Inductive Switching Test Circuit

TO-247 (B) Package Outline



D³PAK Package Outline

e3 100% Sn Plated



Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 6,939,743, 7,352,045 5,283,201 5,801,417 5,648,283 7,196,634 6,664,594 7,157,886 6,939,743 7,342,262 and foreign patents. US and Foreign patents pending. All Rights Reserved.