A product Line of
Diodes Incorporated

PI7C9X794

High Performance 1.62V To 3.6V Quad Uart with 64-Byte FIFO

Features

- 1.62V to 3.6V with 5V Tolerant Serial Inputs
- Single Interrupt output for all 4 UARTs
- A Global Interrupt Source Register for all 4 UARTs
- 5G "Flat" UART Registers for easier programming
- Simultaneous Initialization of all UART channels
- A General Purpose Command-driven 16-bit Timer/counter
- Sleep Mode with Wake-up Indication
- Highly Integrated Device for Space Saving
- Each UART is independently controlled with:
  - 16C550 Compatible 5G Register Set
  - 64-byte Transmit and Receive FIFOs
  - Transmit and Receive FIFO Level Counters
  - Programmable TX and RX FIFO Trigger Level
  - Automatic RTS/CTS or DTR/DSR Flow Control
  - Automatic Xon/Xoff Software Flow Control
  - RS485 HDX Control Output
  - RS485 auto address detection
  - Infrared (IrDA 1.0/1.1) Data Encoder/Decoder
  - Programmable Data Rate with Prescaler
- Up to 8 Mbps Serial Data Rate with 64MHz external clock input
- Crystal oscillator(up to 24MHz) or external clock(up to 80MHz) input
- Built in Power-On-Reset circuit

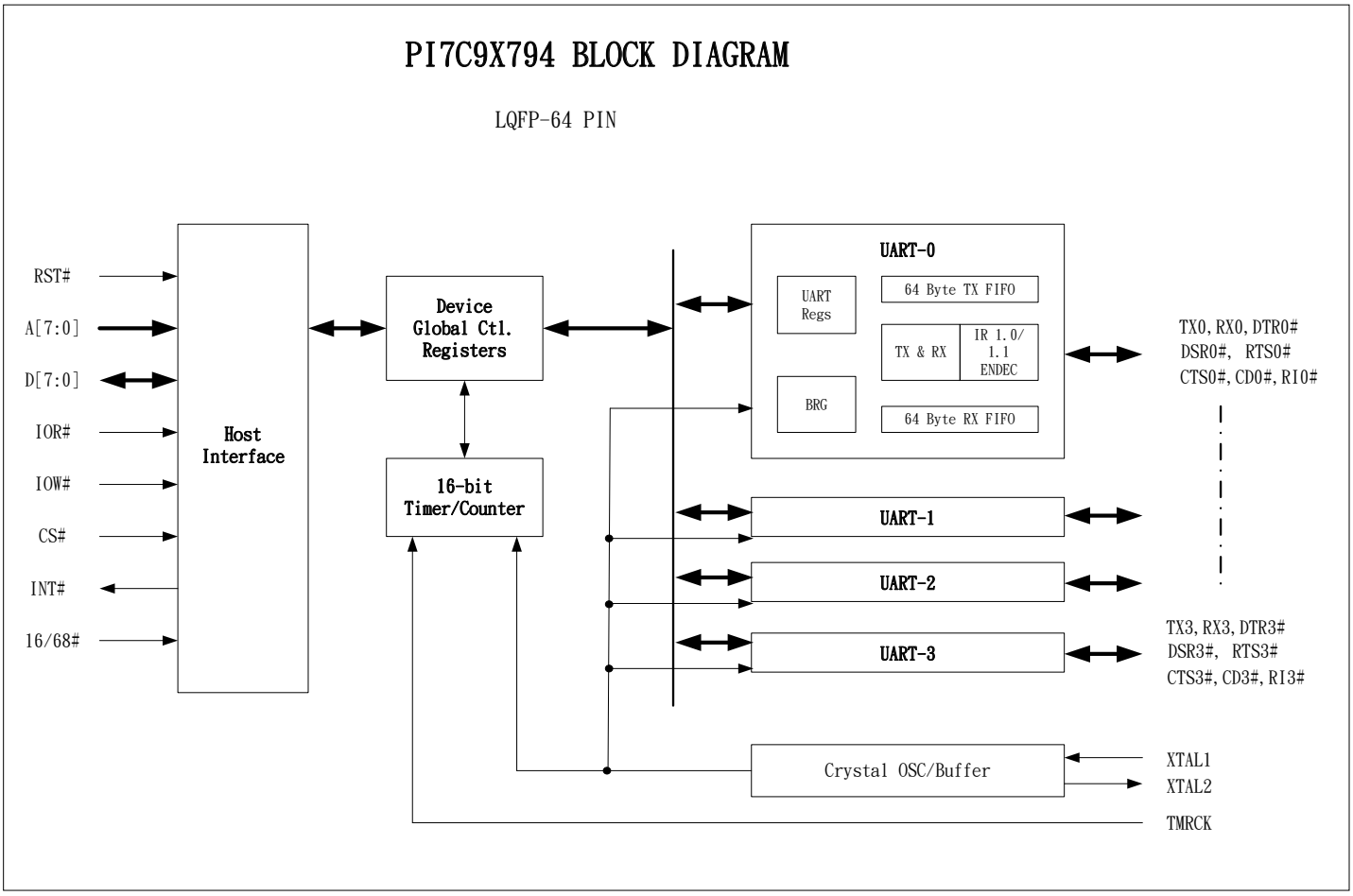
Application

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

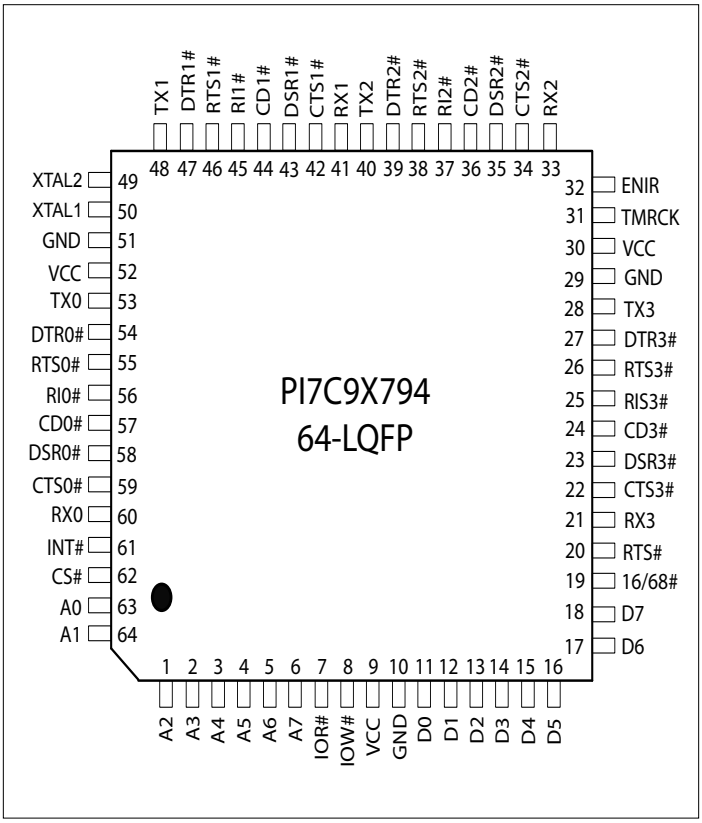
Description

The PI7C9X794 (794), is a 1.62V to 3.6V Quad Universal Asynchronous Receiver and Transmitter (UART) with 5V tolerant serial (modem) inputs. The highly integrated device is designed for high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 8 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, TX and RX FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, TX and RX FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, RS-485 half-duplex direction control, and auto address detection, Intel or Motorola bus interface and sleep mode with a wake-up indicator.

Block Diagram



Pin Configuration 64-LQFP



Pin Description

Pin Name	64-LQFP Pin#	Type	Description
Data Bus Interface			
A7-A0	6-1, 64, 63	I	Address data lines [7:0]. A0:A3 selects individual UART's 16 configuration registers, A4:A6 selects UART channel 0 to 3, and A7 selects the global device configuration registers.
D7:D0	18-11	IO	Data bus lines [7:0] (bidirectional).
IOR#		I	When 16/68# pin is HIGH, it selects Intel bus interface and this input is read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A7:A0], puts it on the data bus to allow the host processor to read it on the leading edge. When 16/68# pin is LOW, it selects Motorola bus interface and this input should be connected to VCC.
IOW# (R/W#)	8	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the leading edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, it selects Motorola bus interface and this input becomes read (logic 1) and write (logic 0) signal.
CS#	62	I	When 16/68# pin is HIGH, this input is chip select (active low) to enable the XR16V794 device. When 16/68# pin is LOW, this input becomes the read and write strobe (active low) for the Motorola bus interface.
INT#	61	OD	Global interrupt output from XR16V794 (open drain, active low). This output requires an external pull-up resistor (47K-100K ohms) to operate properly. It may be shared with other devices in the system to form a single interrupt line to the host processor and have the software driver polls each device for the interrupt status.
Modem Or Serial I/O Interface			
TX0	53	O	UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX0	60	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS0#	55	O	UART channel 0 Request to Send or general purpose output (active low). This port must be asserted prior using for one of two functions: 1) auto RTS flow control, see EFR bit-6, MCR bits-1 & 2, FCTR bits 0-3 and IER bit-6 2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bits 4-7.
CTS0#	59	I	UART channel 0 Clear to Send or general purpose input (active low). It can be used for auto CTS flow control, see EFR bit-7, MCR bit-2 and IER bit-7.

Pin Name	64-LQFP Pin#	Type	Description
DTR0#	54	O	UART channel 0 Data Terminal Ready or general purpose output (active low). This port must be asserted prior using for one of two functions: 1) auto DTR flow control, see EFR bit-6, FCTR bits-0 to 3, MCR bits-0 & 2, and IER bit-6 2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bit 4-7.
DSR0#	58	I	UART channel 0 Data Set Ready or general purpose input (active low). It can be used for auto DSR flow control, see EFR bit-7, MCR bit-2 and IER bit-7.
CD0#	57	I	UART channel 0 Carrier Detect or general purpose input (active LOW).
RI0#	56	I	UART channel 0 Ring Indicator or general purpose input (active LOW).
TX1	48	O	UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX1	41	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS1#	46	O	UART channel 1 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS1#	42	I	UART channel 1 Clear to Send or general purpose input (active low). See description of CTS0# pin.
DTR1#	47	O	UART channel 1 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.
DSR1#	43	I	UART channel 1 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD1#	44	I	UART channel 1 Carrier Detect or general purpose input (active LOW).
RI1#	45	I	UART channel 1 Ring Indicator or general purpose input (active LOW).
TX2	40	O	UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX2	33	I	UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS2#	38	O	UART channel 2 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS2#	34	I	UART channel 2 Clear to Send or general purpose input (active low). See description of CTS0# pin.
DTR2#	39	O	UART channel 2 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.

Pin Name	64-LQFP Pin#	Type	Description
DSR2#	35	I	UART channel 2 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD2#	36	I	UART channel 2 Carrier Detect or general purpose input (active LOW).
RI2#	37	I	UART channel 2 Ring Indicator or general purpose input (active LOW).
TX3	28	O	UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX3	21	I	UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS3#	26	O	UART channel 3 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS3#	22	I	UART channel 3 Clear to Send or general purpose input (active low).d. See description of CTS0# pin.
DTR3#	27	O	UART channel 3 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.
DSR3#	23	I	UART channel 3 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD3#	24	I	UART channel 3 Carrier Detect or general purpose input (active LOW).
RI3#	25	I	UART channel 3 Ring Indicator or general purpose input (active LOW).
Ancillary Signals			
XTAL1	50	I	Crystal or external clock input. Caution: this input is not 5V tolerant.
XTAL2	49	O	Crystal or buffered clock output.
TMRCK	31	I	16-bit timer/counter external clock input.
ENIR	32	I	Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART.
RESET#	20	I	Reset (active low). The configuration and UART registers are reset to default values, see Table 19.
16/68#	12	I	Intel or Motorola data bus interface select. HIGH selects Intel bus interface and LOW selects Motorola interface. This input affects the functionality of IOR#, IOW# and CS# pins.
VCC	9, 30, 52		+2.25V to 3.6V supply with 5V tolerant serial (modem) inputs.
GND	10, 29, 51		Power supply common, ground.

NOTE: Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

Functional Description

The PI7C9X794 integrates the functions of 8 enhanced 16550 UARTs, a general purpose 16-bit timer/counter and an on-chip oscillator. The device configuration registers include a set of four consecutive interrupt source registers that provides interrupt-status for all 4 UARTs, timer/counter and a sleep wake up indicator.

Each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and data transfer. Additionally, each UART channel has 64-byte of transmit and receive FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver. 1.0 and 1.1), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 8Mbps with 8X sampling clock or 4Mbps with 16X sampling clock. The PI7C9X794 is a 1.62-3.6V device with 5 volt tolerant inputs (except XTAL1).

1. Trigger levels

The PI7C9X794 provides independent selectable and programmable trigger levels for both Receiver and transmitter interrupt generation. After reset, both transmitter and receiver FIFOs are disabled and so, in effect, the trigger level is the default value of one character. The selectable trigger levels are controlled via FIFO Control Register(FCR) and Feature Control

Register(FCTR). Refer to Table 1

Table 1. Transmit and Receive FIFO Trigger Table and Level Selection

Trigger	FCTR BIT-7	FCTR BIT-6	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	Receive Trigger Level	Transmit Trigger Level
Table-A	0	0			0	0		1(Default)
			0	0			1(Default)	
			0	1			4	
			1	0			8	
			1	1			14	
Table-B	0	1			0	0		16
					0	1		8
					1	0		24
					1	1		30
			0	0			8	
			0	1			16	
			1	0			24	
			1	1			28	
Table-C	1	0			0	0		8
					0	1		16
					1	0		32
					1	1		56
			0	0			8	
			0	1			16	
			1	0			56	
			1	1			60	
Table-D	1	1	X	X	X	X	Programmable via RX-TRG register	Programmable via TX-TRG register

2. Hardware flow control

Hardware flow control is comprised of Auto-$\overline{\text{CTS}}$ and Auto-RTS (see Figure 1). Auto-$\overline{\text{CTS}}$ and Auto-$\overline{\text{RTS}}$ can be enabled/disabled independently by programming EFR[7:6].

With Auto-$\overline{\text{CTS}}$, $\overline{\text{CTS}}$ must be active before the UART can transmit data.

Auto-$\overline{\text{RTS}}$ only activates the $\overline{\text{RTS}}$ output when there is enough room in the FIFO to receive data and de-activates the $\overline{\text{RTS}}$ output when the RX FIFO is sufficiently full. The halt and resume trigger levels is controlled by FCR and FCTR bits.

If both Auto-$\overline{\text{CTS}}$ and Auto-$\overline{\text{RTS}}$ are enabled, when $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If not enabled, overrun errors occur if the transmit data rate exceeds the receive FIFO servicing latency.

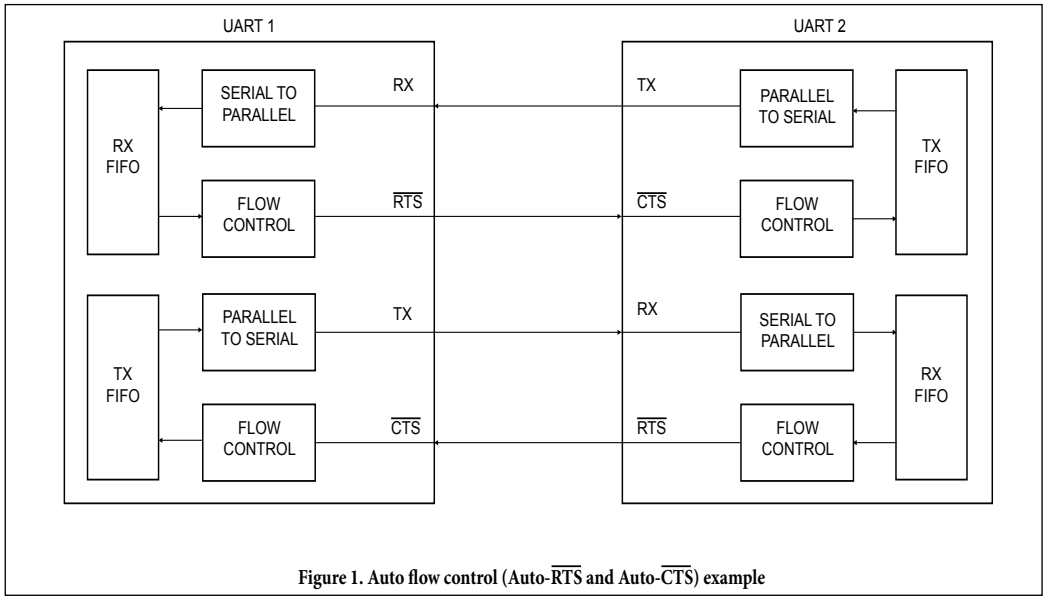


Figure 1. Auto flow control (Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$) example

2.1 Auto RTS/DTR Hardware Flow Control Operation

Figure 2 shows RTS#/DTR# functional timing. The RTS#/DTR# output pin is used to request remote unit to suspend/resume data transmission. The flow control features are individually selected to fit specific application requirement:

•Select RTS (and CTS) or DTR (and DSR) through MCR bit-2.

•Enable auto RTS/DTR flow control using EFR bit-6.

•The auto RTS or auto DTR function must be started by asserting the RTS# or DTR# output pin (MCR bit-1 or bit-0 to a logic 1, respectively) after it is enabled.

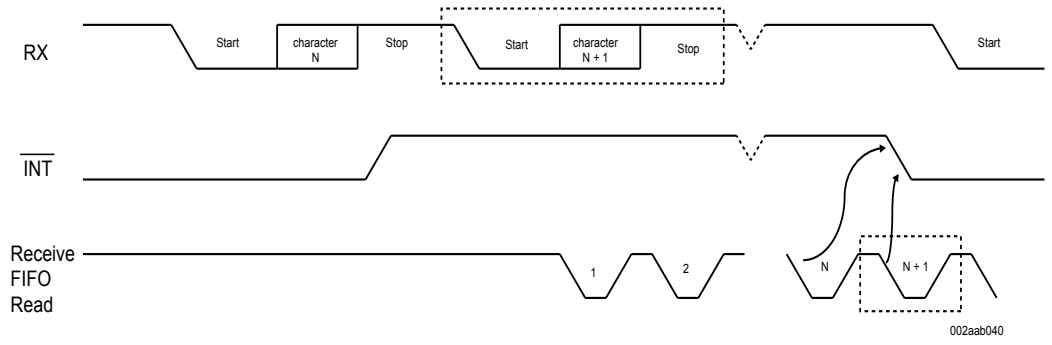
•If using programmable RX FIFO trigger levels, hysteresis levels can be selected via FCTR bits 3-0.

With the Auto RTS function enabled, the RTS# output pin will not be de-asserted (HIGH) when the receive FIFO reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level for Trigger Tables A-C (See Table 1). The RTS# output pin will be asserted (LOW) again after the FIFO is unloaded to the next trigger level below the programmed trigger level.

For Trigger Table D (or programmable trigger levels), the RTS# output pin is de-asserted when the the RX FIFO level reaches the RX trigger level plus the hysteresis level and is asserted when the RX FIFO level falls below the RX trigger level minus the hysteresis level.

However, even under these conditions, the 794 will continue to accept data until the receive FIFO is full if the remote UART transmitter continues to send data.

•If used, enable RTS/DTR interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS#/DTR# pin makes a transition: ISR bit-5 will be set to 1.



(1) N = receiver FIFO trigger level.
(2) The two blocks in dashed lines cover the case where an additional character is sent.

Figure 2. RTS functional timing

2.2 Auto CTS/DSR Flow Control

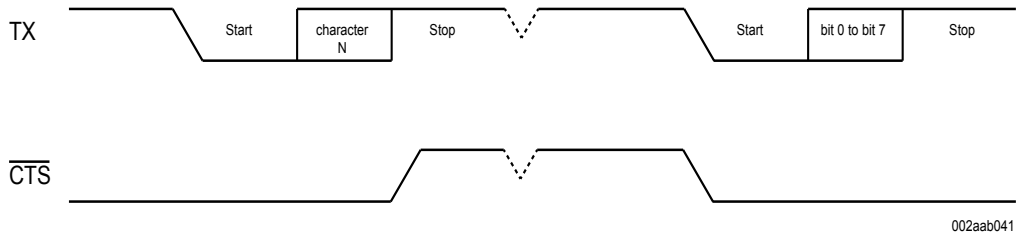
The CTS/DSR pin is monitored to suspend/restart local transmitter. The flow control features are individually selected to fit specific application requirement:

•Select CTS (and RTS) or DSR (and DTR) through MCR bit-2.

•Enable auto CTS/DSR flow control using EFR bit-7.

With the Auto CTS or Auto DTR function enabled, the UART will suspend transmission as soon as the stop bit of the character in the Transmit Shift Register has been shifted out. Transmission is resumed after the CTS#/DTR# input is re-asserted (LOW), indicating more data may be sent.

If used, enable CTS/DSR interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS#/DSR# pin makes a transition: ISR bit-5 will be set to a logic 1, and UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS#/DSR# input returns LOW, indicating more data may be sent.



(1) When $\overline{CTS}$ is LOW, the transmitter keeps sending serial data out.
(2) When $\overline{CTS}$ goes HIGH before the middle of the last stop bit of the current character, the transmitter finishes sending the current
character, but it does not send the next character.
(3) When $\overline{CTS}$ goes from HIGH to LOW, the transmitter begins sending data again.

Figure 3. $\overline{CTS}$ functional timing

3 Software flow control

Software flow control is enabled through the Enhanced Features Register and the Modem Control Register. Different combinations of software flow control can be enabled by setting different combinations of EFR[3:0]. Table 1 shows software flow control options.

Table 2. Software flow control options (EFR[3:0])

EFR[3]	EFR[2]	EFR[1]	EFR[0]	TX, RX software flow control
0	0	x	x	no transmit flow control
1	0	x	x	transmit Xon1, Xoff1
0	1	x	x	transmit Xon2, Xoff2
1	1	x	x	transmit Xon1 and Xon2, Xoff1 and Xoff2
x	x	0	0	no receive flow control
x	x	1	0	receiver compares Xon1, Xoff1
x	x	0	1	receiver compares Xon2, Xoff2
1	0	1	1	transmit Xon1, Xoff1 receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	transmit Xon2, Xoff2 receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	transmit Xon1 and Xon2, Xoff1 and Xoff2 receiver compares Xon1 and Xon2, Xoff1 and Xoff2

There are two other enhanced features relating to software flow control:

• Xon Any function (MCR[5]): Receiving any character will resume operation after recognizing the Xoff character. It is possible that an Xon1 character is recognized as an Xon Any character, which could cause an Xon2 character to be written to the RX FIFO.

• Special character (EFR[5]): Incoming data is compared to Xoff2. Detection of the special character sets the Xoff interrupt (IIR[4]) but does not halt transmission. The Xoff interrupt is cleared by a read of the Interrupt Identification Register (IIR). The special character is transferred to the RX FIFO.

3.1 Receive flow control

When software flow control operation is enabled, UART will compare incoming data with Xoff1/Xoff2 programmed characters (in certain cases, Xoff1 and Xoff2 must be received sequentially). When the correct Xoff characters are received, transmission is halted after completing transmission of the current character. Xoff detection also sets IIR[4] (if enabled via IER[5]) and causes $\overline{\text{INT}}$ to go LOW.

To resume transmission, an Xon1/Xon2 character must be received (in certain cases Xon1 and Xon2 must be received sequentially). When the correct Xon characters are received, IIR[4] is cleared, and the Xoff interrupt disappears.

3.2 Transmit flow control

Xoff1/Xoff2 character is transmitted after the receive FIFO crosses the programmed receiver trigger level (for all trigger tables A-D). Xon1/Xon2 character is transmitted as soon as receive FIFO is less than one trigger level below the programmed receiver trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS/DTR Hysteresis value in Table 3.

The transmission of Xoff/Xon(s) follows the exact same protocol as transmission of an ordinary character from the FIFO. This means that even if the word length is set to be 5, 6, or 7 bits, then the 5, 6, or 7 least significant bits of Xoff1/Xoff2, Xon1/Xon2 will be transmitted. (Note that the transmission of 5, 6, or 7 bits of a character is seldom done, but this functionality is included to maintain compatibility with earlier designs.)

It is assumed that software flow control and hardware flow control will never be enabled simultaneously. Figure 4 shows an example of software flow control.

Table 3. SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED

FCTR BIT-3	FCTR BIT-2	FCTR BIT-1	FCTR BIT-0	RTS/DTR Hysteresis (Characters)
0	0	0	0	0
0	0	0	1	+/- 4
0	0	1	0	+/- 6
0	0	1	1	+/- 8
0	1	0	0	+/- 8
0	1	0	1	+/- 16
0	1	1	0	+/- 24
0	1	1	1	+/- 32
1	1	0	0	+/- 12
1	1	0	1	+/- 20
1	1	1	0	+/- 28
1	1	1	1	+/- 36
1	0	0	0	+/- 40
1	0	0	1	+/- 44
1	0	1	0	+/- 48
1	0	1	1	+/- 52

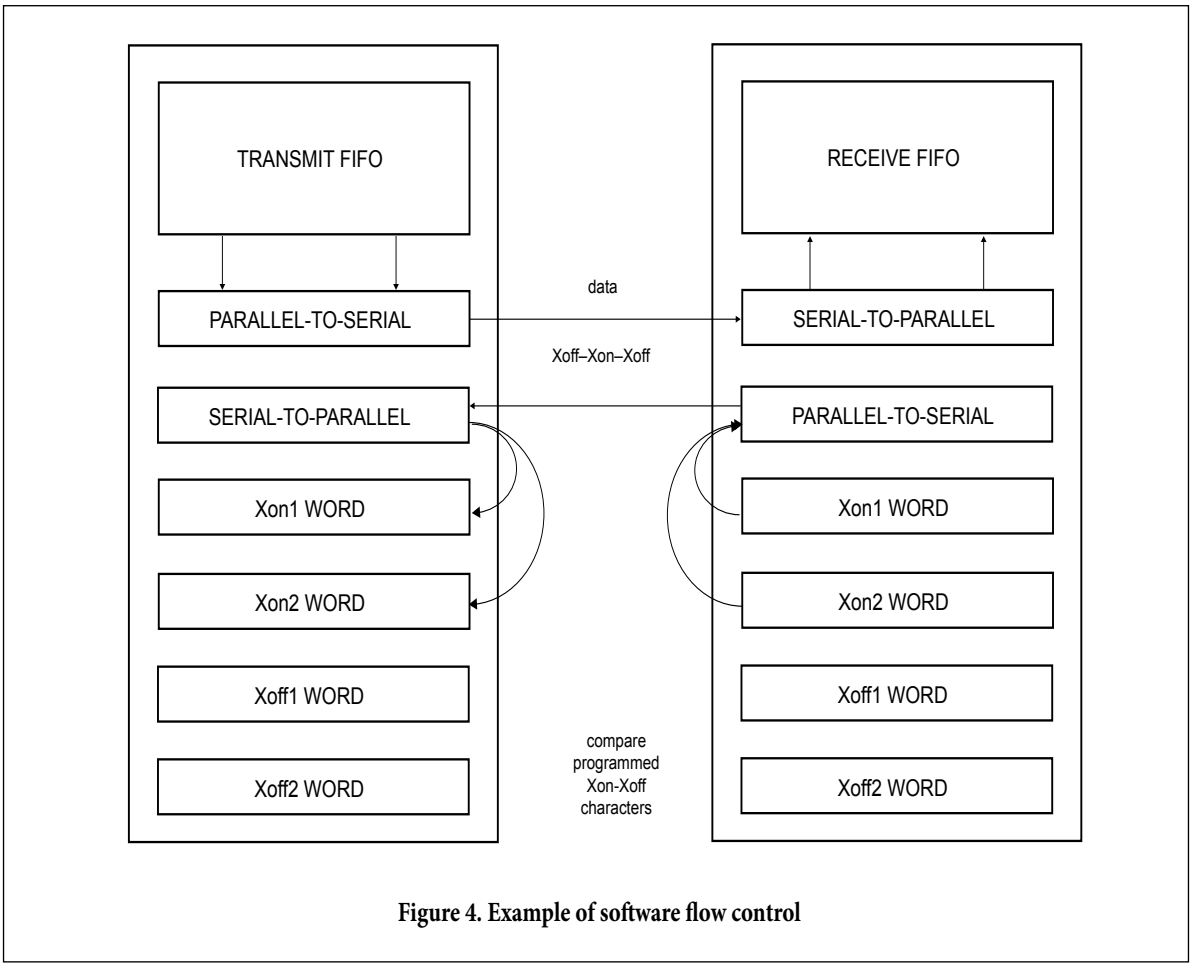


Figure 4. Example of software flow control

4. Hardware Reset, Power-On Reset (POR) and Software Reset

These three reset methods are identical and will reset the internal registers as indicated in Table 4.

Table 2 summarizes the state of register after reset.

Table 4. UART Reset Conditions

Register	Reset state
DLL	Bits 7-0 = 0x01
DLM	Bits 7-0 = 0x00
DLD	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = logic 0 Bits 7-4 = logic level of the inputs
SPR	Bits 7-0 = 0xFF
FCTR	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
TFCNT	Bits 7-0 = 0x00
TFTRG	Bits 7-0 = 0x00
RFCNT	Bits 7-0 = 0x00
RFTRG	Bits 7-0 = 0x00
XCHAR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00

Table 5. Output signals after reset

Signal	Reset state
TX	HIGH
$\overline{\text{RTS}}$/$\overline{\text{DTR}}$	HIGH
$\overline{\text{INT}}$	HIGH by external pull-up

5 Interrupts

The UART has interrupt generation and prioritization (seven prioritized levels of interrupts) capability. The interrupt enable registers (IER and IOIntEna) enable each of the seven types of interrupts and the INT signal in response to an interrupt generation. When an interrupt is generated, the IIR indicates that an interrupt is pending and provides the type of interrupt through IIR[5:0]. Table 4 summarizes the interrupt control functions.

Table 6. Interrupt Source and Priority Level

IIR[5:0]	Priority level	Interrupt type	Interrupt source
00 0001	none	none	None
00 0110	1	receiver line status	Overrun Error (OE), Framing Error (FE), Parity Error (PE), or Break Interrupt (BI) errors occur in characters in the RX FIFO
00 1100	3	RX time-out	Stale data in RX FIFO
00 0100	2	RHR interrupt	Receive data ready (FIFO disable) or RX FIFO above trigger level (FIFO enable)
00 0010	4	THR interrupt	Transmit FIFO empty (FIFO disable) or TX FIFO passes above trigger level (FIFO enable)
00 0000	5	modem status	Change of state of modem input pins
01 0000	6	Xoff interrupt	Receive Xoff character(s)/special character
10 0000	7	$\overline{\text{CTS}}$, $\overline{\text{RTS}}$	$\overline{\text{RTS}}$ pin or $\overline{\text{CTS}}$ pin change state from active (LOW) to inactive (HIGH)

It is important to note that for the framing error, parity error, and break conditions, Line Status Register bit 7 (LSR[7]) generates the interrupt. LSR[7] is set when there is an error anywhere in the RX FIFO, and is cleared only when there are no more errors remaining in the FIFO. LSR[4:2] always represent the error status for the received character at the top of the RX FIFO. Reading the RX FIFO updates LSR[4:2] to the appropriate status for the new character at the top of the FIFO. If the RX FIFO is empty, then LSR[4:2] are all zeros.

For the Xoff interrupt, if an Xoff flow character detection caused the interrupt, the interrupt is cleared by an Xon flow character detection. If a special character detection caused the interrupt, the interrupt is cleared by a read of the IIR.

5.1 Interrupts Generation

- LSR is by any of the LSR bits 1, 2, 3, 4 and 7.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

5.2 Interrupts Clearing

- LSR interrupt is cleared by reading all characters with errors out of the RX FIFO if it is Frame/Parity/Break Error, and is cleared by reading LSR if it is Overrun Error.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared when Xon character(s) is received or reading ISR.
- Special character interrupt is cleared by a read to ISR or after next character is received
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register

5.3 Interrupt mode operation

In Interrupt mode (if any bit of IER[3:0] is 1) the host is informed of the status of the receiver and transmitter by an interrupt signal, $\overline{INT}$. Therefore, it is not necessary to continuously poll the Line Status Register (LSR) to see if any interrupt needs to be serviced. Figure 5 shows Interrupt mode operation.

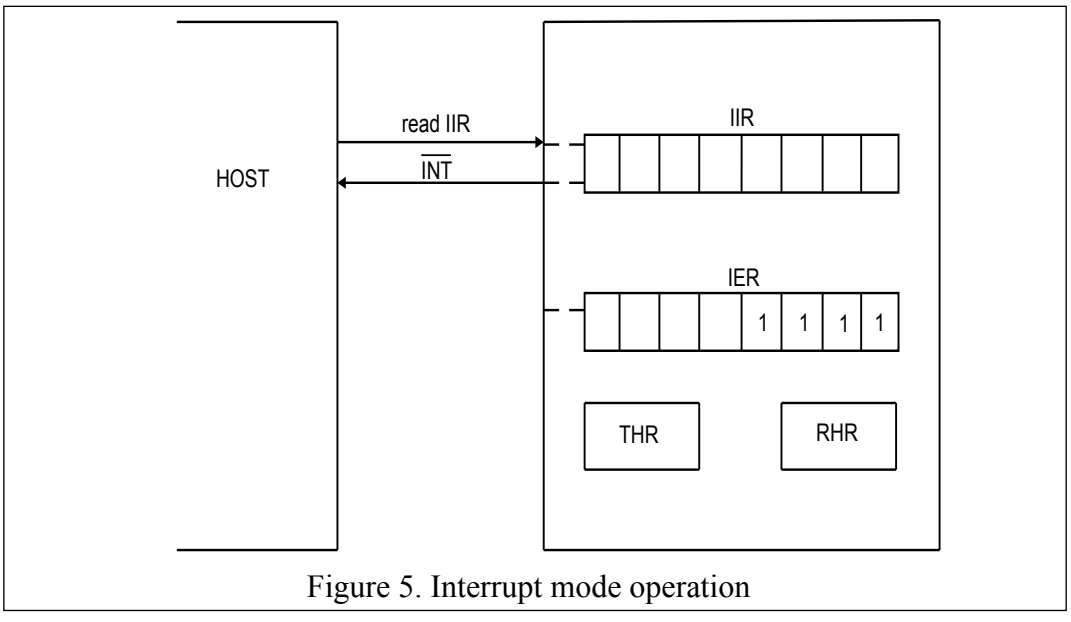


Figure 5. Interrupt mode operation

5.4 Polled mode operation

In Polled mode (IER[3:0] = 0000) the status of the receiver and transmitter can be checked by polling the Line Status Register (LSR). This mode is an alternative to the FIFO Interrupt mode of operation where the status of the receiver and transmitter is automatically known by means of interrupts sent to the CPU. Figure 6 shows FIFO Polled mode operation.

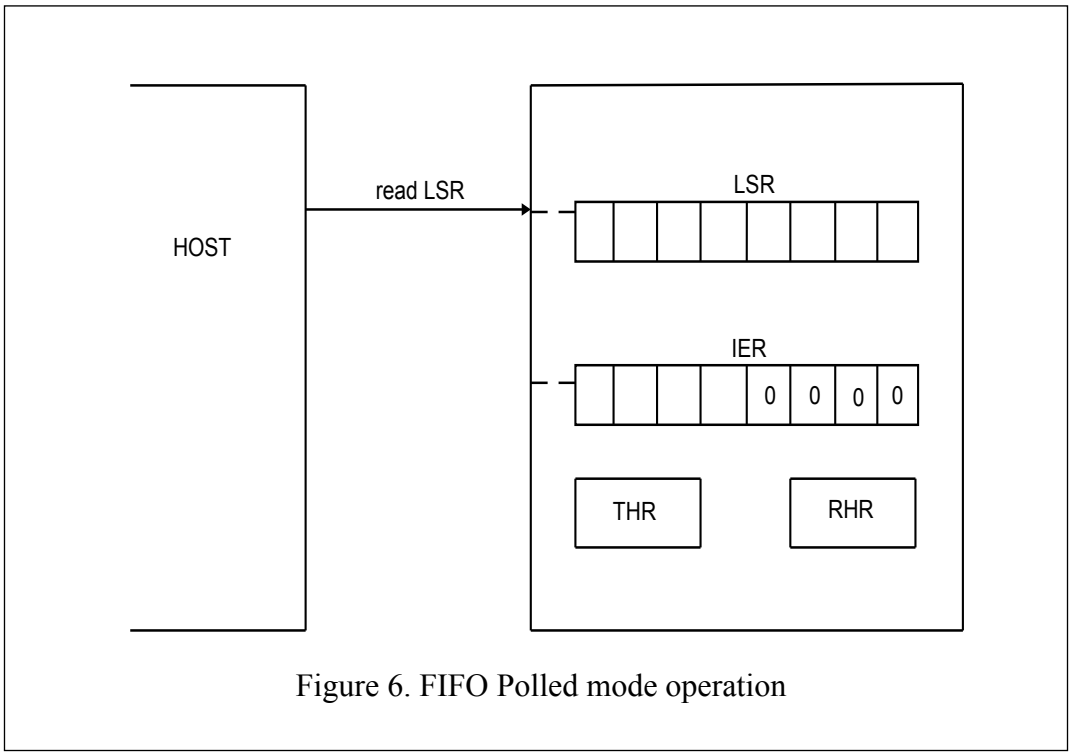


Figure 6. FIFO Polled mode operation

6 Sleep mode

Sleep mode is an enhanced feature of the UART. It is enabled when EFR[4], the enhanced functions bit, is set and when IER[4] is set. Sleep mode is entered when:

- The serial data input line, RX, is idle (see Section 7 “Break and time-out conditions”).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending except THR.
- Sleep register = 0 xFF
- Modem inputs are not toggling

Remark: Sleep mode will not be entered if there is data in the RX FIFO.

In Sleep mode, the clock to the UART is stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced. The UART will wake up when any change is detected on the RX line, when there is any change in the state of the

modem input pins, or if data is written to the TX FIFO.

Remark: Writing to the divisor latches DLL and DLH to set the baud clock must not be done during Sleep mode. Therefore, it is advisable to disable Sleep mode using IER[4] before writing to DLL or DLH.

7 Break and time-out conditions

When the UART receives a number of characters and these data are not enough to set off the receive interrupt (because they do not reach the receive trigger level), the UART will generate a time-out interrupt instead, 4 character times after the last character is received. The time-out counter will be reset at the center of each stop bit received or each time the receive FIFO is read.

A break condition is detected when the RX pin is pulled LOW for a duration longer than the time it takes to send a complete character plus start, stop and parity bits. A break condition can be sent by setting LCR[6], when this happens the TX pin will be pulled LOW until LSR[6] is cleared by the software.

8 Programmable baud rate generator

The UART contains a programmable baud rate generator that takes any clock input and divides it by a divisor in the range between 1 and (2^{16} - 1). An additional divide-by-4 prescaler is also available and can be selected by MCR[7], as shown in Figure 7. The formula for the baud rate is:

$$\text{Baud rate} = \frac{\left(\frac{\text{XTAL1 crystal input frequency}}{\text{prescaler}}\right)}{\text{divisor x sample rate}}$$

where:

prescaler = 1, when MCR[7] is set to logic 0 after reset (divide-by-1 clock selected)

prescaler = 4, when MCR[7] is set to logic 1 after reset (divide-by-4 clock selected).

Divisor = {DLH, DLL}

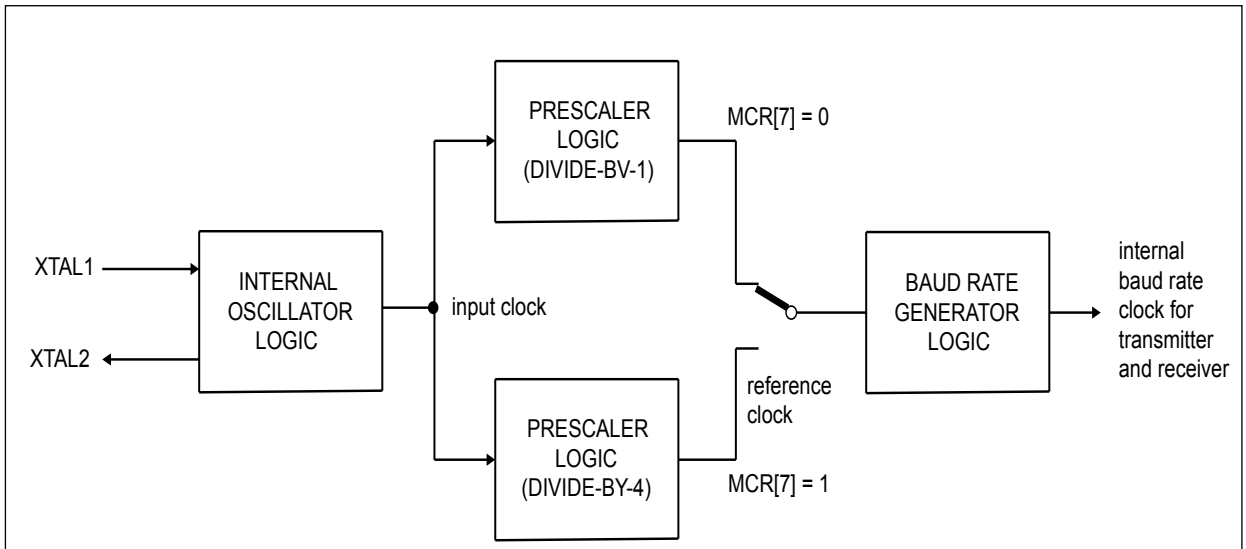


Figure 7. Prescaler and baud rate generator block diagram

Sample rate = 8 if MODE_8X = 1, ot = 16 - SCR + CPR if MODE _8X = 0

Remark: The default value of prescaler after reset is divide-by-1.

DLL and DLH must be written to in order to program the baud rate. DLL and DLH are the least significant and most significant byte of the baud rate divisor. If DLL and DLH are both zero, the UART is effectively disabled, as no baud clock will be generated.

Remark: The programmable baud rate generator is provided to select both the transmit and receive clock rates.

Table 5 to 8 show the baud rate and divisor correlation for crystal with frequency 1.8432 MHz, 3.072 MHz, 14.74926 MHz, and 24MHz respectively.

Table 7. Baud rates using a 1.8432 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
50	2304	16	0
75	1536	16	0
110	1047	16	0.026
134.5	857	16	0.058
150	768	16	0
300	384	16	0
600	192	16	0
1200	96	16	0
1800	64	16	0
2000	46	20	0.617
2400	48	16	0
3600	32	16	0
4800	24	16	0
7200	16	16	0
9600	12	16	0
19200	6	16	0
38400	3	16	0
56000	2	16	2.86

Table 8. Baud rates using a 3.072 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
50	2304	16	0
75	2560	16	0
110	1745	16	0.026
134.5	1428	16	0.034
150	1280	16	0
300	640	16	0
600	320	16	0
1200	160	16	0
1800	90	19	0.195
2000	96	16	0
2400	80	16	0
3600	45	19	0.195
4800	40	16	0
7200	25	17	0.392
9600	20	16	0
19200	10	16	0
38400	5	16	0

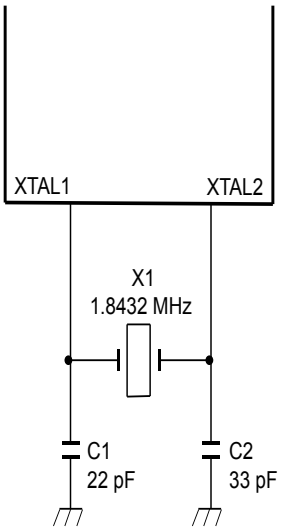


Figure 8. Crystal oscillator circuit reference

Table 9. Baud rates using a 14.74926 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
38400	24	16	0.025
56000	11	24	0.235
57600	16	16	0.025
115200	8	16	0.025
153600	6	16	0.025
921600	1	16	0.025

Table 10. Baud rates using a 24 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
4800	250	20	0
7200	159	21	0.17
25000	48	20	0
38400	25	25	0
57600	22	19	0.32
115200	8	26	0.16
225000	6	18	1.2
400000	3	20	0
921600	1	26	0.16
1000000	1	24	0

9. RS-485 features

9.1 Auto RS-485 $\overline{\text{RTS}}$ control

Normally the $\overline{\text{RTS}}$ pin is controlled by MCR bit 1, or if hardware flow control is enabled, the logic state of the $\overline{\text{RTS}}$ pin is controlled by the hardware flow control circuitry. FCTR register bit 5 will take the precedence over the other two modes; once this bit is set, the transmitter will control the state of the $\overline{\text{RTS}}$ pin. The transmitter automatically de-asserts the $\overline{\text{RTS}}$ pin (logic 1) once the host writes data to the transmit FIFO, and asserts $\overline{\text{RTS}}$ pin (logic 0) once the last bit of the data has been transmitted.

To use the auto RS-485 $\overline{\text{RTS}}$ mode the software would have to disable the hardware flow control function.

9.2 RS-485 $\overline{\text{RTS}}$ output inversion

RS485 register bit 5 reverses the polarity of the $\overline{\text{RTS}}$ pin if the UART is in auto RS-485 $\overline{\text{RTS}}$ mode. If RS485 bit 5 is and when the transmitter has data to be sent it asserts the $\overline{\text{RTS}}$ pin (logic 0), and when the last bit of the data has been sent out the transmitter de-asserts the $\overline{\text{RTS}}$ pin (logic 1).

9.3 Auto RS-485

RS458 register bit 0 is used to enable the RS-485 mode (multidrop or 9-bit mode). In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' stations. The slave stations examine the received data and interrupt the controller if the received character is an address character (parity bit = 1).

To use the auto RS-485 RTS mode the software would have to disable the hardware flow control function.

9.3.1 Normal multidrop mode

The 9-bit mode in RS458 register bit 0 is enabled, but not Special Character Detect (EFR bit 5). The receiver is set to Force Parity 0 (LCR[5:3] = 111) in order to detect address bytes.

With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate a line status interrupt (IER bit 2 must be set to '1' at this time), and at the same time puts this address byte in the RX FIFO. After the controller examines the byte it must make a decision whether or not to enable the receiver; it should enable the receiver if the address byte addresses its ID address, and must not enable the receiver if the address byte does not address its ID address.

If the controller enables the receiver, the receiver will receive the subsequent data until being disabled by the controller after the controller has received a complete message from the 'master' station. If the controller does not disable the receiver after receiving a message from the 'master' station, the receiver will generate a parity error upon receiving another address byte. The controller then determines if the address byte addresses its ID address, if it is not, the controller then can disable the receiver. If the address byte addresses the 'slave' ID address, the controller take no further action; the receiver will receive the subsequent data.

9.3.2 Auto address detection

If Special Character Detect is enabled (EFR[5] is set and XOFF2 contains the address byte) the receiver will try to detect an address byte that matches the programmed character in XOFF2. If the received byte is a data byte or an address byte that does not match the programmed character in XOFF2, the receiver will discard these data. Upon receiving an address byte that matches the XOFF2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates a line status interrupt (IER bit 2 must be set to 1 at this time). The receiver will then receive the subsequent data from the 'master' station until being disabled by the controller after having received a message from the 'master' station.

If another address byte is received and this address byte does not match XOFF2 character, the receiver will be automatically disabled and the address byte is ignored. If the address byte matches XOFF2 character, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit (LSR[2]).

10. Host interface

The host interface is 8 data bits wide with 8 address lines and control signals to execute data bus read and write transactions. The PI7C9X794 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required for a data bus transaction. Each bus cycle is asynchronous using CS# IOR# and IOW# or CS#, R/W#, All four UART channels share the same data bus for host operations. Please refer to pin description and host interface read/write timing(Figure 10 and Figure 11).

10.1 UART Channel Selection

A LOW on the chip select pin, CS#, allows the user to select one of the UART channels to configure, send transmit data and/or unload receive data to/from the UART. When address line A7 = 0, address lines A6:A4 are used to select one of the four channels, while A3:A0 are used to select one of the register in one channel. See Table 11 below for UART channel selection.

Table 11. UART Channel Selection

A7	A6	A5	A4	Function
0	0	0	0	Channel 0 Selected
0	0	0	1	Channel 1 Selected
0	0	1	0	Channel 2 Selected
0	0	1	1	Channel 3 Selected

When A7=1, Uart device configuration registers are selected.These registers provide global controls and status of all 8 channel UARTs that include interrupt status, 16-bit general purpose timer control and status, 8X or 16X sampling clock, sleep mode control, soft-reset control, simultaneous UART initialization, and device identification and revision.

10.2 Simultaneous Write to All Channels

During a write cycle, the setting of the Device Configuration register REGB bit-0 to a logic 1 will override the channel selection of address A6:A4 and allow a simultaneous write to all 4 UART channels when any channel is written to. This functional capability allow the registers in all 4 UART channels to be modified concurrently, saving individual channel initialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode. Also, REGB bit-0 should be reset to a logic 0 before attempting to read from the UART

11. Infrared Mode

The UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0 and 1.1. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream with a data rate up to 115.2 Kbps. For the IrDA 1.1 standard, the infrared encoder sends out a 1/4 of a bit time wide HIGH-pulse for each "0" bit in the transmit data stream with a data rate up to 1.152 Mbps. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 9 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. With this bit enabled, the infrared encoder and decoder is compatible to the IrDA 1.0 standard. For the infrared encoder and decoder to be compatible to the IrDA 1.1 standard, ASR bit-4 will also need to be set to a ’1’. When the infrared feature is enabled, the transmit data output, TX, idles LOW. Likewise, the RX input also idles LOW, see Figure 9.

The wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

The UART can be in the infrared mode upon power-up following a hardware reset (RESET#) or soft-reset if the ENIR pin is HIGH. After power-up, the infrared mode can be controlled via MCR bit-6.

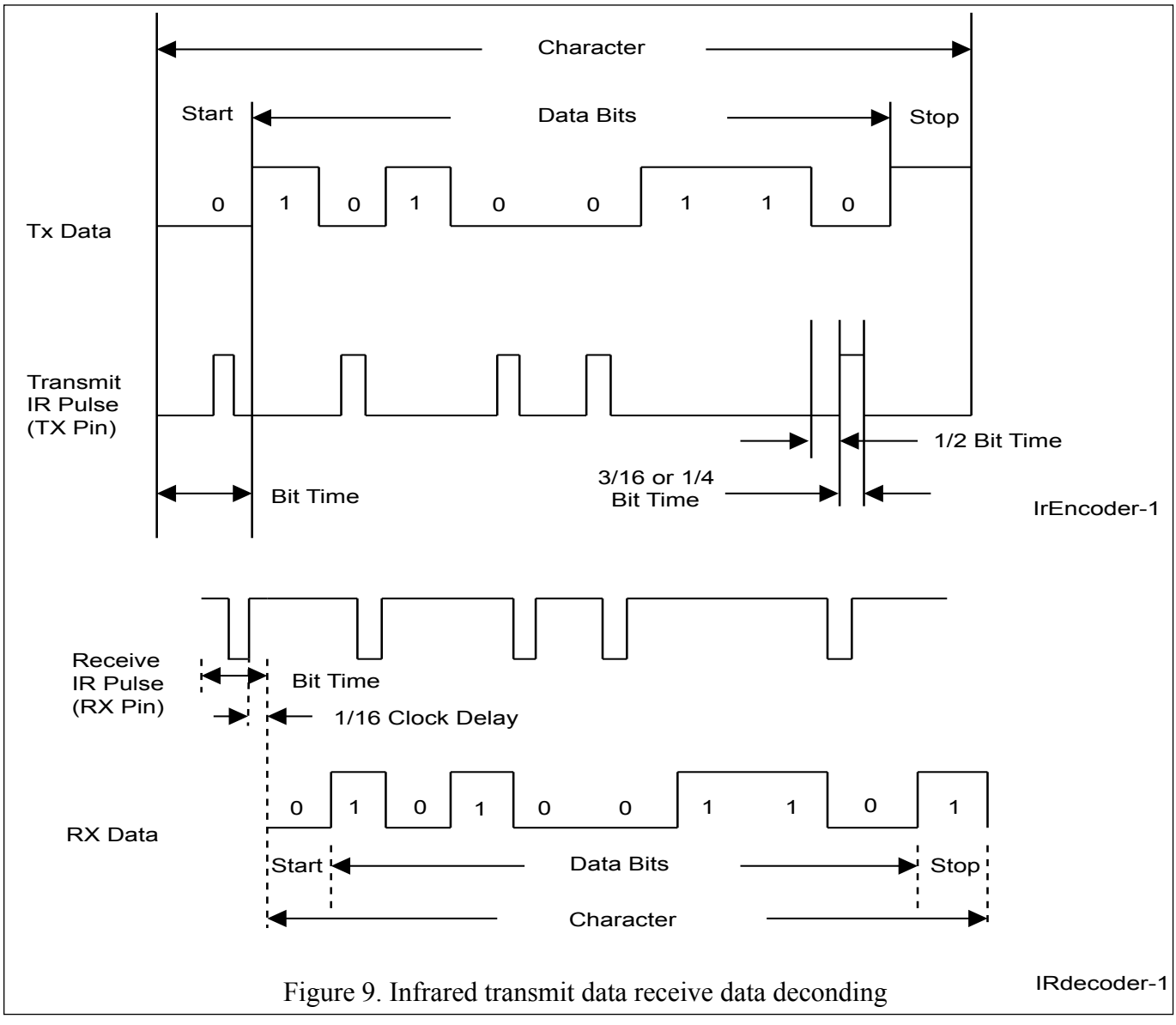


Figure 9. Infrared transmit data receive data deconding

12. Configuration Registers

UART Channel Configuration Registers

Offset 00H(default=xxH)---Receiver Holding Register (RHR). Accessable when LCR[7]=0.		
Bit	**Type**	**Description**
[7:0]	RO	Rx Holding - When data are read from the RHR,they are removed from the top of the receiver's FIFO. Data read from the RHR when FIFO is empty are invalid. The Line Status Register(LSR) indicates the full or empty status of the FIFOs.
Offset 00H(default=xxH)---Transmitter Holding Register (THR). Accessable when LCR[7]=0		
Bit	**Type**	**Description**
[7:0]	WO	Tx Holding - When data are written to the THR,they are written to the bottom of the transmitter's FIFO. Data written to the THR when FIFO is full are lost. The Line Status Register(LSR) indicates the full or empty status of the FIFOs.
Offset 01H(default=00H)---Interrupt Enable Register (IER). Accessable when LCR[7]=0.		
Bit	**Type**	**Description**
7	RW	CTS interrupt - "1": enable CTS interrupt
6	RW	RTS interrupt - "1": enable RTS interrupt
5	RW	Xoff/Special charatcter interrupt - "1": enable the Software Flow Control interrupt
4	RO	Reserved
3	RW	Modem Status interrupt - "1": enable Modem Status interrupt
2	RW	Receiver Line Status interrupt - "1": enable Receiver Line Status interrupt
1	RW	Tx Ready interrupt - "1": enable THR Ready interrupt 1 = Interrupt is issued whenever the THR becomes empty in non-FIFO mode or when spaces in the FIFO is above the trigger level in the FIFO mode.
0	RW	Rx Data Ready interrupt - "1": enable Data Ready interrupt

Note: IER[7:5] can only be modified if EFR[4]=1.

Offset 02H(default=01H)---Interrupt Status Register (ISR). Accessable when LCR[7]=0		
Bit	**Type**	**Description**
[7:6]	RO	Mirror the content of FCR[0]
[5:1]	RO	5-bit encoded interrupt.
0	RO	Interrupt status. "1": No interrupt is pending. "0": An interrupt is pending.

Priority Level	IIR[5]	IIR[4]	IIR[3]	IIR[2]	IIR[1]	IIR[0]	Source of Interrupt
1	0	0	0	1	1	0	Receive Line Status Error
2	0	0	0	1	0	0	RHR ready interrupt
3	0	0	1	1	0	0	Receiver timeout
4	0	0	0	0	1	0	THR ready interrupt
5	0	0	0	0	0	0	modem status register interrupt
6	0	1	0	0	0	0	Rx Xon/Xoff signal/special character
7	1	0	0	0	0	0	CTS,RTS change from active to inactiove
-	0	0	0	0	0	1	None (default)

Note: ISR[4] is cleared by Xon detection if the interrupt is caused by Xoff detection, or cleared by a read of the IIR if it is caused by special char detection.

Offset 02H(default=00H)--- FIFO Control Register (FCR). Accessable when LCR[7]=0

Bit	Type	Description
[7:6]	WO	RX trigger. Sets the trigger level for the RX FIFO
[5:4]	WO	TX trigger. Sets the trigger level for the TX FIFO

Trigger Table	FCTR[7]	FCTR[6]	FCR[7]	FCR[6]	FCR[5]	FCE[4]	RXTGL	TXTGL
Table-A	0	0	0	0	0	0	1	1
			0	1			4	
			1	0			8	
			1	1			14	
Table-B	0	1	0	0	0	0	16	16
			0	1	0	1	8	8
			1	0	1	0	16	24
			1	1	1	1	24	30
			1				28	
Table-C	1	0	0	0	0	0	8	8
			0	1	0	1	16	16
			1	0	1	0	32	32
			1	1	1	1	56	56
			1				60	
Table-D	1	1	X	X	X	X	RXTRG	TXTGL

3	WO	DMA mode enabled when set
2	WOS	Reset TX FIFO. 0 = no FIFO transmit reset 1 = clears the contents of Tx FIFO and resets the FIFO level logic. TSR is not cleared. This bit will return to logic 0 after clearing the FIFO
1	WOS	Reset RX FIFO. 0 = no FIFO receive reset 1 = clears the contents of Rx FIFO and resets the FIFO level logic. RSR is not cleared. This bit will return to logic 0 after clearing the FIFO
0	WO	FIFO enable 0 = disable the transmit and receive FIFO. and TX/RX can only hold one character at a time. other FCR bits are not programmable. and the trigger level is set to one character. 1 = enable the transmit and receive FIFO. and TX/RX FIFO can hold 64 characters.

Note: FCR[5:4] can only be modified and enabled if EFR[4]=1. Table-D see below FCTR description for the detail

Offset 03H(default=00H)--- Line Control Register (LCR).		
Bit	**Type**	**Description**
7	RW	Divisor latch enabled when set
6	RW	Break control bit. 0 = no TX break condition 1 = forces TX to logic 0 to alert a line break condition
5	RW	Set forced parity format(if LCR[3]=1) 0 = parity is not forced. 1 = parity bit is forced to high if LCR[4]=0,or low if LCR[4]=1.
4	RW	Parity type select. 0 = odd parity is generated(if LCR[3]=1) 1 = even parity is generated(if LCR[3]=1)
3	RW	Parity enable when set
2	RW	Number of Stop bits 0 = 1 stop bit. 1 = 1.5 stop bits for word length=5, or 2 stop bits for word length=6,7,8
[1:0]	RW	Word length bits: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits
Offset 04H(default=00H)--- Modem Control Register (MCR).		
Bit	Type	Description
7	RW	Clock pre-scaler select. 0 = divide-by-1 clock input 1 = divide-by-4 clock input
6	RW	IrDA mode enable when set
5	RW	when set,Xon Any function is enabled and receiving any character will resume transmit operation. the RX character will be loaded into the RX FIFO. unless the RX character is an Xon/Xoff character and receiver software flow control is enabled.
4	RW	when set, internal loopback mode is enabled and TX output is loope back to the RX input internally, and MCR[1:0] signals are looped back into MSR[4:5]
3	RW	when set, send char immediately and then self clearing or OP2. Internal Loopback Mode(MCR[4]=1) is outputed to CD internally
2	RW	DTR# or RTS# for auto hardware flow control select 0 = RTS# and CTS# pins for auto hardware flow control 1 = DTR# and DSR# pins for auto hardware flow control OP1. Internal Loopback Mode(MCR[4]=1) is outputed to RI internally
1	RW	RTS pin control. 0 = force RTS pin High 1 = force RTS pin Low

0	RW	DTR pin control. 0 = force DTR pin High 1 = force DTR pin Low

Note: MCR[7:5,3:2] can only be modified if EFR[4]=1.

Offset 05H(default=60H)--- Line Status Register (LSR).		
Bit	Type	Description
7	RO	Receiver FIFO Data Error Flag. 0 = No FIFO Error 1 = a flag for the sum of all error bits(parity error, framing error, or break)in the RX FIFO. this bit clears when there is no more error in any of the bytes in the RX FIFO
6	RO	THR and TSR Empty Flag This bit is set whenever the transmitter goes idle, it clears whenever either the THR or TSR contains a data character.
5	RO	THR Empty Flag This bit is set when the last data byte is transferred from THR to TSR.
4	RO	Receiver Break Error Flag 0 = No Break Error 1 = break condition occurred in data to be read from RX FIFO(RX was LOW for at least one character frame time).
3	RO	Receiver Data Framing Error Flag 0 = No Data Framing Error 1 = framing error occurred in data to be read from RX FIFO (The receive character did not have a valid stop bits).
2	RO	Receiver Data Parity Error Flag 0 = No Data Parity Error 1 = parity error in data to be read from RX FIFO
1	RO	Receiver Overrun Error 0 = No verrun Error 1 = additional data received while the RX FIFO is full. This data should not be transferred into FIFO.
0	RO	Receiver Data Ready Indicator 0 = No data in received in RX FIFO 1 = Data has been received and saved in the RX FIFO
Offset 06H(default=x0H)--- Modem Status Register (MSR).		
Bit	Type	Description
7	RO	CD input satus Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to MCR[3].
6	RO	RI input satus Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to MCR[2]
5	RO	DSR input satus Normally this bit is the complement of the DSR# input. In the loopback mode this bit is equivalent to MCR[0]

4	RO	CTS input satus Normally this bit is the complement of the CTS# input. In the loopback mode this bit is equivalent to MCR[1]
3	RO	Read delta CD# input flag 0 = No change on CD# input 1 = The CD# input has changed state. A modem status interrupt status interrupt will be generated if MSR interrupt is enabled. when set, disable transmitter.
2	RO	Read delta RI# input flag 0 = No change on RI# input 1 = The RI# input has changed from a LOW to HIGH. A modem status interrupt will be generated if MSR interrupt is enabled. when set, disable receiver.
1	RO	Delta DSR# input flag 0 = No change on DSR# input 1 = The DSR# input has changed state. A modem status interrupt will be generated if MSR interrupt is enabled.
0	RO	Delta CTS# input flag 0 = No change on CTS# input 1 = The CTS# input has changed state. A modem status interrupt will be generated if MSR interrupt is enabled.

Note: The default of MSR[7:4]= logic levels of the inputs inverted. MSR[3:2] can only be modified if EFR[4]=1.

Offset 07H(default=FFH)--- Scratch Pad Register (SPR).		
Bit	**Type**	**Description**
[7:0]	RW	This is 8-bit general purpose register for the user to store temporary data. the content is preserved during sleep mode.
Offset 00H(default=01H)---Divisor Latch LSB(DLL). Accessable when LCR[7]=1		
Bit	**Type**	**Description**
[7:0]	RW	LSB bits of divisor for baud rate generator.
Offset 01H(default=00H)---Divisor Latch MSB(DLM). Accessable when LCR[7]=1		
Bit	**Type**	**Description**
[7:0]	RW	MSB bits of divisor for baud rate generator.

Note:Pre_Scaler = 2**(2*MCR[7]) Baud Rate = XIN /((256*DLM+DLL)*Pre_Scaler*(16-8*MODE_8X[i])) or Baud_Rate = XIN /((256*DLM+DLL)*Pre_Scaler*(16-SCR+CPR)), when MODE_8X[i]=0

Offset 08H(default=00H)--- Feature Control Register (FCTR).		
Bit	**Type**	**Description**
[7:6]	RW	Select the transmit and receive FIFO trigger lavel table A-D See above FCR register description for the detail.

5	RW	RS-485 half-duplex control 0 = transmitter does not control PTS# pin 1 = Transmitter controls RTS# pin
4	RW	Infranred RX input logic select 0 = RX input as active HIGH, normal 1 = RX input as active LOW, inverted
[3:0]	RW	Auto RTS/DTR flow control hysteresis select

Note: Auto RTS/DTR flow control hysteresis select for receiver FIFO trigger level table D only

FCTR[3]	FCTR[2]	FCTR[1]	FCTR[0]	RTS/DTR Hysteresis
				(Characters)
0	0	0	0	0
0	0	0	1	+/- 4
0	0	1	0	+/- 6
0	0	1	1	+/- 8
0	1	0	0	+/- 8
0	1	0	1	+/- 16
0	1	1	0	+/- 24
0	1	1	1	+/- 32
1	1	0	0	+/- 12
1	1	0	1	+/- 20
1	1	1	0	+/- 28
1	1	1	1	+/- 36
1	0	0	0	+/- 40
1	0	0	1	+/- 44
1	0	1	0	+/- 48
1	0	1	1	+/- 52

Offset 09H(default=00H)--- Enhanced Feature Register (EFR).

Bit	Type	Description
7	RW	Auto CTS/DSR Flow Control Enable 0 = Automatic CTS/DSR flow control is disabled. 1 = Automatic CTS/DSR flow control is enabled. The selection for CTS# or DSR# is through MCR[2].
6	RW	Auto RTS/DTR Flow Control Enable 0 = Automatic RTS/DTR flow control is disabled. 1 = Automatic RTS/DTR flow control is enabled. The selection for CTS# or DSR# is through MCR[2].
5	RW	Special character detect 0 = Special character detect is disabled. 1 = Special character detect is enabled. If received data matchs Xoff2 data, the received data is transferred to RX FIFO and ISR[4] is set to high to indicate a special character detection. However,if flow control is set for comparing Xoff2,then flow control works normally and Xoff2 will not go to the FIFO and will generate an Xoff interrupt and a special character interrupt.
4	RW	Enhanced Function Bits Enable This bit enables IER[7:5],ISR[5:4],FCR[5:4],MCR[7:5][3:2],MSR[3:2], and ASR[7:0] to be modified and enable sleep mode

[3:0]	RW	Software Flow Control Select: 00xx = No TX flow control 10xx = Transmit Xon1,Xoff1 01xx = Transmit Xon2,Xoff2 11xx = Transmit Xon1 and Xon2,Xoff1 and Xoff2 xx00 = No RX flow control xx10 = Receiver compares Xon1,Xoff1 xx01 = Receiver compares Xon2,Xoff2 1011 = Transmit Xon1,Xoff1; Receiver compares Xon1 or Xon2,Xoff1 or Xoff2 0111 = Transmit Xon2,Xoff2; Receiver compares Xon1 or Xon2,Xoff1 or Xoff2 1111 = Transmit Xon1 and Xon2,Xoff1 and Xoff2; Receiver compares Xon1 and Xon2,Xoff1 and Xoff2 0011 = No transmit flow control; Receiver compares Xon1 and Xon2,Xoff1 and Xoff2

Offset 0AH(default=00H)--- Transmit FIFO Level Counter Register (TXCNT).

Bit	Type	Description
[7:0]	RO	Indication of the number of characters in TX FIFO

Offset 0AH(default=00H)--- Transmit FIFO Trigger Level Register (TXTRG).

Bit	Type	Description
[7:0]	WO	Set TX FIFO trigger level from 0x00 to 0x40

Offset 0BH(default=00H)--- Receive FIFO Level Counter Register (RXCNT).

Bit	Type	Description
[7:0]	RO	Indication of the number of characters in RX FIFO

Offset 0BH(default=00H)--- Receive FIFO Trigger Level Register (RXTRG).

Bit	Type	Description
[7:0]	WO	Set RX FIFO trigger level from 0x00 to 0x40

Offset 0CH(default=00H)--- XOFF1 character Register (XOFF1).

Bit	Type	Description
[7:0]	WO	Set XOFF1 character

Offset 0CH(default=00H)--- XCHAR Register (XCHAR).

Bit	Type	Description
[7:4]	RO	Reserved
3	RO	Transmit Xon indicator
2	RO	Transmit Xoff indicator
1	RO	Transmit Xon indicator
0	RO	Transmit Xoff indicator

Offset 0DH(default=00H)--- XOFF2 character Register (XOFF2).		
Bit	**Type**	**Description**
[7:0]	WO	Set XOFF2 character
Offset 0EH(default=00H)--- XON1 character Register (XON1).		
Bit	**Type**	**Description**
[7:0]	WO	Set XON1 character
Offset 0FH(default=00H)--- XON2 character Register (XON2).		
Bit	**Type**	**Description**
[7:0]	WO	Set XON2 character
Offset 02H(default=00)--- Advance Special Register (ASR). Accessable when LCR[7]=1 and EFR[4]=1.		
Bit	**Type**	**Description**
7	RW	When set, RS-485 control register access enable
6	RO	Reserved
5	RO	Reserved
4	RW	IrDA slow/fast mode contro 0 = IrDA version 1.0, 3/16 pulse ratio,data rate up to 115.2 Kbps 1 = IrDA version 1.1, 1/4 pulse ratio,data rate up to 1.152 Mbps
3	RO	Reserved
2	RW	When set, sample clock register enable
[1:0]	RO	Reserved
Offset 05H(default=00)--- Sample Clock Register (SNR). Accessable when LCR[7]=1 and ASR[2]=1		
Bit	**Type**	**Description**
[7:4]	RW	SCR - Sample clock value, which is used to baud rate generate
[3:0]	RW	CPR - N number in calculating, which is used to baud rate generate

Note: 16-SCR+CPR>1, when set SNR to control the baud rate, MODE_8X[i] should be keep the default logic 0

Offset 06H(default=00)--- RS-485 Mode Control Register (RS485). Accessable when LCR[7]=1 and ASR[7]=1		
Bit	**Type**	**Description**
[7:6]	RO	Reserved
5	RW	Auto RS-485 Polarity Inversion This bit changes the polarity of the Auto RS-485 Direction Control output pin (RTS#). It will only affect the behavior of RTS# if RS485[4]=1 0 = RTS# output is HIGH when transmitting and LOW when receiving 1 = RTS# output is LOW when transmitting and HIGH when receiving

4	RW	Auto RS-485 direction control This bit enables the transmitter to control RTS# pin 0 = transmitter does not control RTS# pin 1 = transmitter controls RTS# pin
[3:1]	RO	Reserved
0	RW	When set, wnable RS-485 9-bit mode

UART Device Configuration Registers

Offset 80H(default=00H)--- Global Interrupt Register 0 (INT0).		
Bit	**Type**	**Description**
[7:0]	RO	Reserved

INT0[7]	INT0[6]	INT0[5]	INT0[4]	INT0[3]	INT0[2]	INT0[1]	INT0[0]
Reserved	Reserved	Reserved	Reserved	CH-3	CH-2	CH-1	CH-0

Offset 81H(default=00H)--- Global Interrupt Register 1 (INT1).		
Bit	**Type**	**Description**
[7:0]	RO	Encoded interruput indicator (3-bits per channel)
Offset 82H(default=00H)--- Global Interrupt Register 2 (INT2).		
Bit	**Type**	**Description**
[7:0]	RO	Reserved
Offset 83H(default=00H)--- Global Interrupt Register 3 (INT3).		
Bit	**Type**	**Description**
[7:0]	RO	Reserved

INT3[7]	INT3[6]	INT3[5]	INT3[4]	INT3[3]	INT3[2]	INT3[1]	INT3[0]	INT2[7]	INT2[6]	INT2[5]	INT2[4]
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

INT2[3]	INT2[2]	INT2[1]	INT2[0]	INT1[7]	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]
CH-3[2]	CH-3[1]	CH-3[0]	CH-2[2]	CH-2[1]	CH-2[0]	CH-1[2]	CH-1[1]	CH-1[0]	CH-0[2]	CH-0[1]	CH-0[0]

Priority	Bit[2]	Bit[1]	Bit[0]	Interrupt Source and Clearing
X	0	0	0	none or wake-up indicator
1	0	0	1	RXRDY and RX line status
2	0	1	0	RXRDY time-out
3	0	1	1	TXRDY, THR or TSR empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR or Xoff/Xon or special character detected
5	1	0	1	Reserved
6	1	1	0	Reserved
7	1	1	1	TIMER time-out, shows up on channel 0 only

Note: time-out interrupt clear by read global register TIMER_CTL

Offset 84H(default=00H)--- Timer Control Register (TIMER_CTL).		
Bit	**Type**	**Description**
[7:4]	RO	Reserved
3	RW	Clock source select
2	RW	Function select
1	RW	Start timer
0	RW	Enable timer interrupt

TIMER_CTL[3:0]	Timer control commands decode
0001	enable timer interrupt
0010	disable timer interrupt
0011	select one-shot mode
0100	select re-trigger mode
0101	select internalclock source for the timer
0110	select external clock source for the timer
0111	reserved
1000	reserved
1001	start timer
1010	stop timer
1011	reset timer

Note: TIMER_CTL[3:0]=1100~1111 are reserved

Offset 89H(default=00H)--- Reserved		
Offset 8AH(default=00H)--- Software Reset Register (SF_RESET)		
Bit	**Type**	**Description**
[7:0]	WOS	Individula UART channel reset enable
Offset 8BH(default=00H)--- Sleep Mode Control Register (SLEEP)		
Bit	**Type**	**Description**
[7:0]	RW	Individula UART channel sleep enable
Offset 8CH(default=00H)--- Device Revision Register (DREV)		
Bit	**Type**	**Description**
[7:0]	RO	Revision number of the PSC794
Offset 8DH(default=94H)--- Device Identification Register (DVID)		
Bit	**Type**	**Description**
[7:0]	RO	The device ID for PSC794 bonding option 0 - 1

Offset 8EH(default=00H)--- Simultaneous configuration All UART Register (REGB)		
Bit	**Type**	**Description**
[7:1]	RO	reserved
[0]	RW	when set, write to all UARTs enable

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Power Supply Range.....3.8V
Voltage IO Any Pins.....GND-0.3V to 5.5V
Storage Temperature .....–65°C to +150°C
Junction Temperature (Tj) ..... 125°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

TA = -40°C to 85°C, V_{CC} is 1.62V to 3.6V

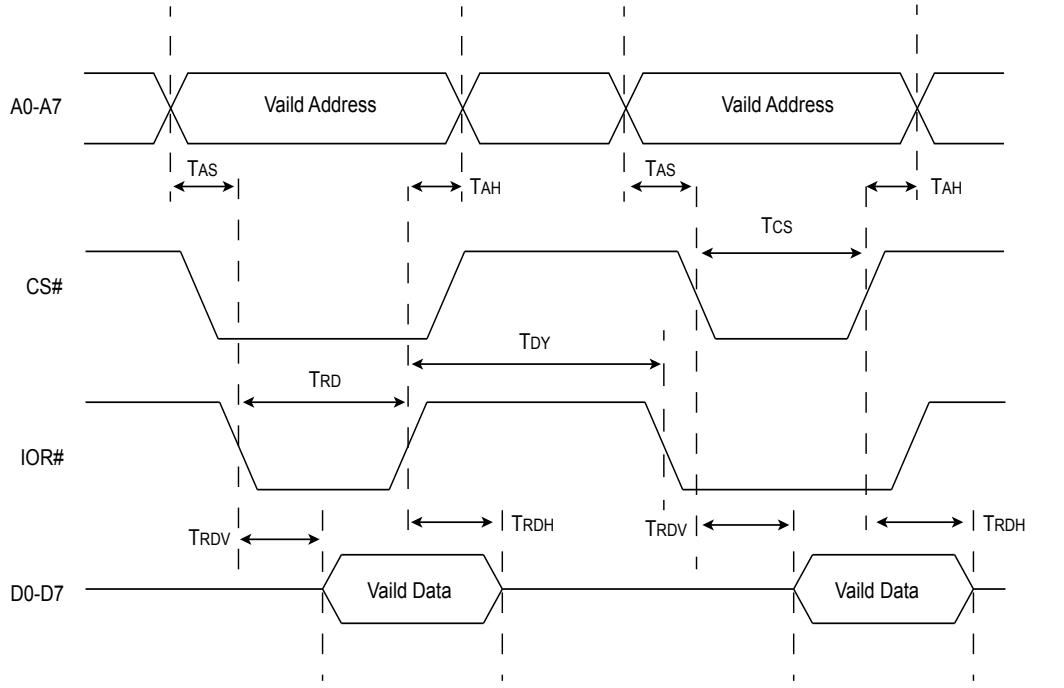
Symbol	Parameter	1.8V		2.5V		3.3V		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{ILCK}	Clock input low level	-0.3	0.3	-0.3	0.6	-0.3	0.6	V	
V_{IHCK}	Clock input high level	1.4	VCC	1.8	VCC	2.4	VCC	V	
V_{IL}	Input low voltage	-0.3	0.2	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input high voltage	1.4	5.5	1.8	5.5	2.0	5.5	V	
V_{OL}	Output low voltage						0.4	V	I_{OL} = 4 mA
					0.4			V	I_{OL} = 2 mA
			0.4					V	I_{OL} = 1.5 mA
V_{OH}	Output high voltage					2.0		V	I_{OH} = -1 mA
				1.8				V	I_{OH} = -400 uA
		1.4						V	I_{OH} = -200 uA
I_{IL}	Input low leakage current		10		-10		-10	uA	
I_{IH}	Input high leakage current		10		10		10	uA	
C_{IN}	Input pin capacitance		5		5		5	pF	
I_{CC}	Power supply current		20		20		25	mA	EXT Clock=14.75MHz All inputs at VCC or GND and outputs unloaded
I_{SLEEP}	Sleep current		300		350		400	uA	Four UARTs asleep. All inputs at VCC or GND and outputs unloaded.

Note: 5.5V steady voltage tolerance on inputs and outputs is valid only when the supply voltage is present.

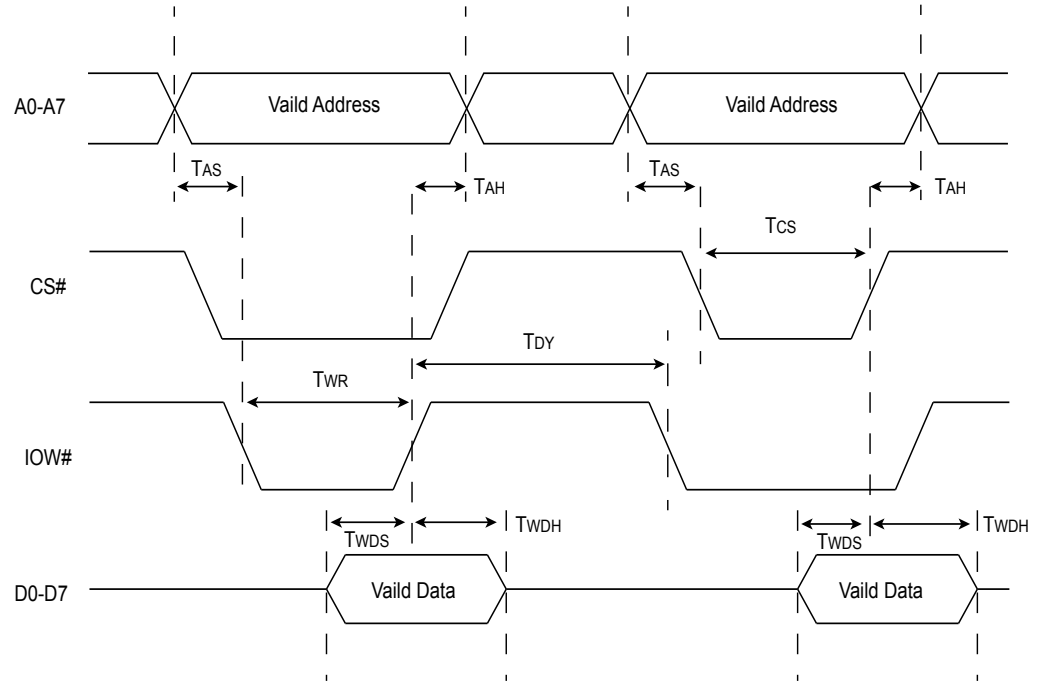
AC Electrical Characteristic

TA = -40°C to +85°C, V_{CC} is 1.62V to 3.6V, 70pF load where applicable

Symbol	Parameter	Min.	Max.	Unit
T_{C1},T_{C2}	Clock Pulse Period	6		ns
T_{OSC}	Crystal Frequency		24	MHz
T_{ECK}	External Clock Frequency		80	MHz
T_{AS}	Address Setup (16 Mode)	0		ns
T_{AH}	Address Hold (16 Mode)	0		ns
T_{CS}	Chip Select Width (16 Mode)	20		ns
T_{DY}	Delay between CS# Active Cycles (16 Mode)	20		ns
T_{RD}	Read Strobe Width (16 Mode)	20		ns
T_{WR}	Write Strobe Width (16 Mode)	20		ns
T_{RDV}	Read Data Valid (16 Mode)		30	ns
T_{WDS}	Write Data Setup (16 Mode)	10		ns
T_{RDH}	Read Data Hold (16 Mode)		10	ns
T_{WDH}	Write Data Hold (16 Mode)	5		ns
T_{ADS}	Address Setup (68 Mode)	0		ns
T_{ADH}	Address Hold (68 Mode)	0		ns
T_{RWS}	R/W# Setup to CS# (68 Mode)	0		ns
T_{RDA}	Read Data Access (68 mode)		30	ns
T_{RDH}	Read Data Hold (68 mode)		10	ns
T_{WDS}	Write Data Setup (68 mode)	10		ns
T_{WDH}	Write Data Hold (68 Mode)	5		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted (68 Mode)	1		ns
T_{CSL}	CS# Width (68 Mode)	20		ns
T_{CSD}	CS# Cycle Delay (68 Mode)	20		ns
T_{WDO}	Delay from IOW# to Modem Output		50	ns
T_{MOD}	Delay to set Interrupt from Modem Input		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45	ns
T_{SI}	Delay From Stop To Interrupt		45	ns
T_{WRI}	Delay From IOW# To Reset Interrupt		45	ns
T_{RST}	Reset Pulse	40		ns
Bclk	Baud Clock	16X or 8X of data rate		Hz

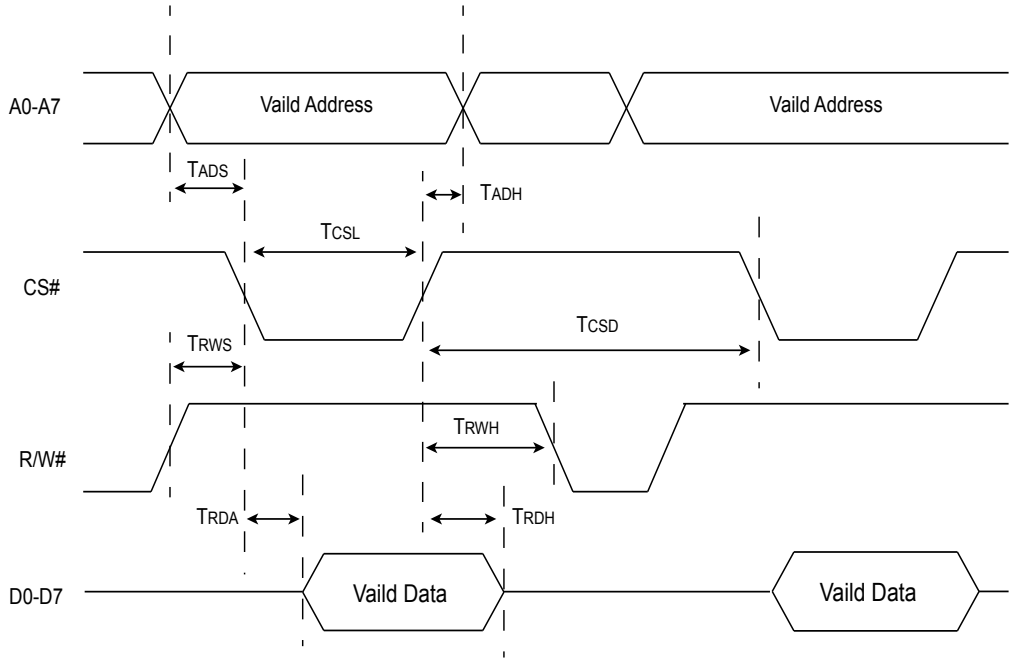


16 Mode (Intel) Data Bus Read Timing



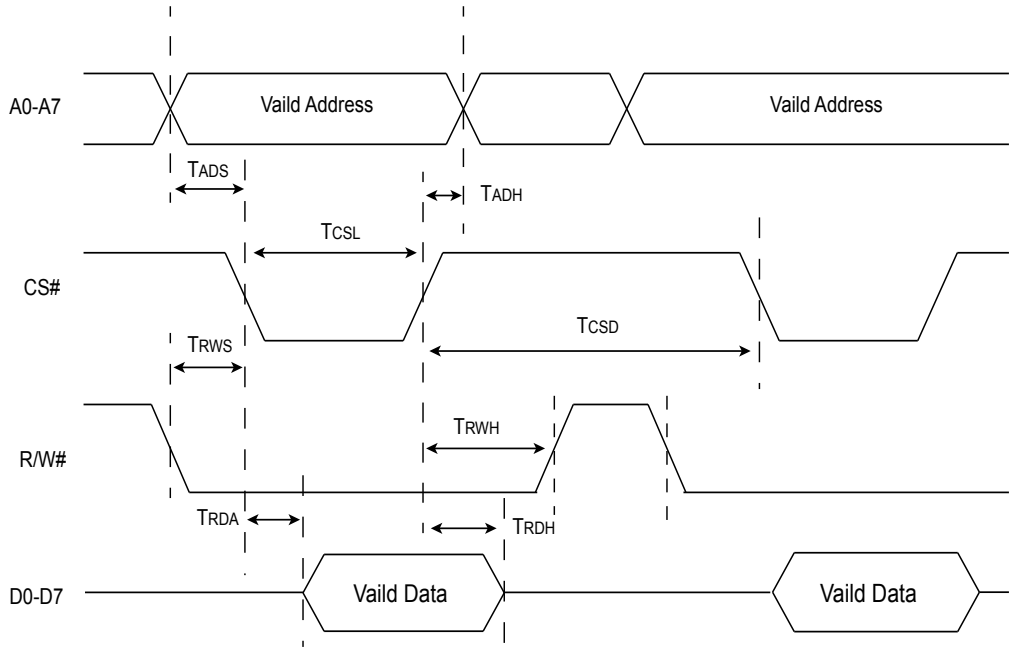
16 Mode (Intel) Data Bus Write Timing

Figure 10. 16 Mode (intel) data bus read and write timing



68Read

68 Mode (Motorola) Data Bus Read Timing



68Write

68 Mode (Motorola) Data Bus WriteTiming

Figure 11. 68 Mode (motorola) data bus read and write timing

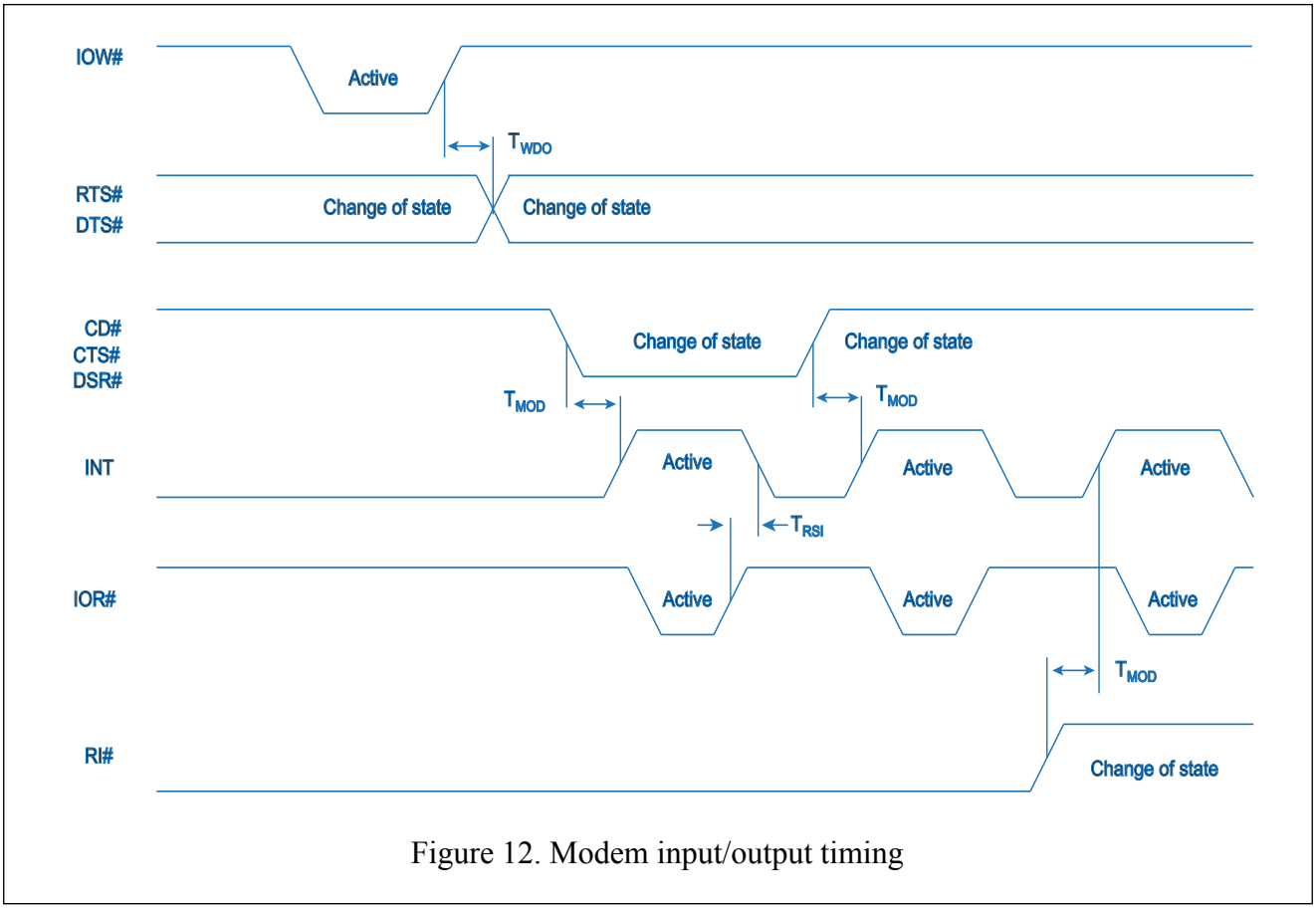


Figure 12. Modem input/output timing

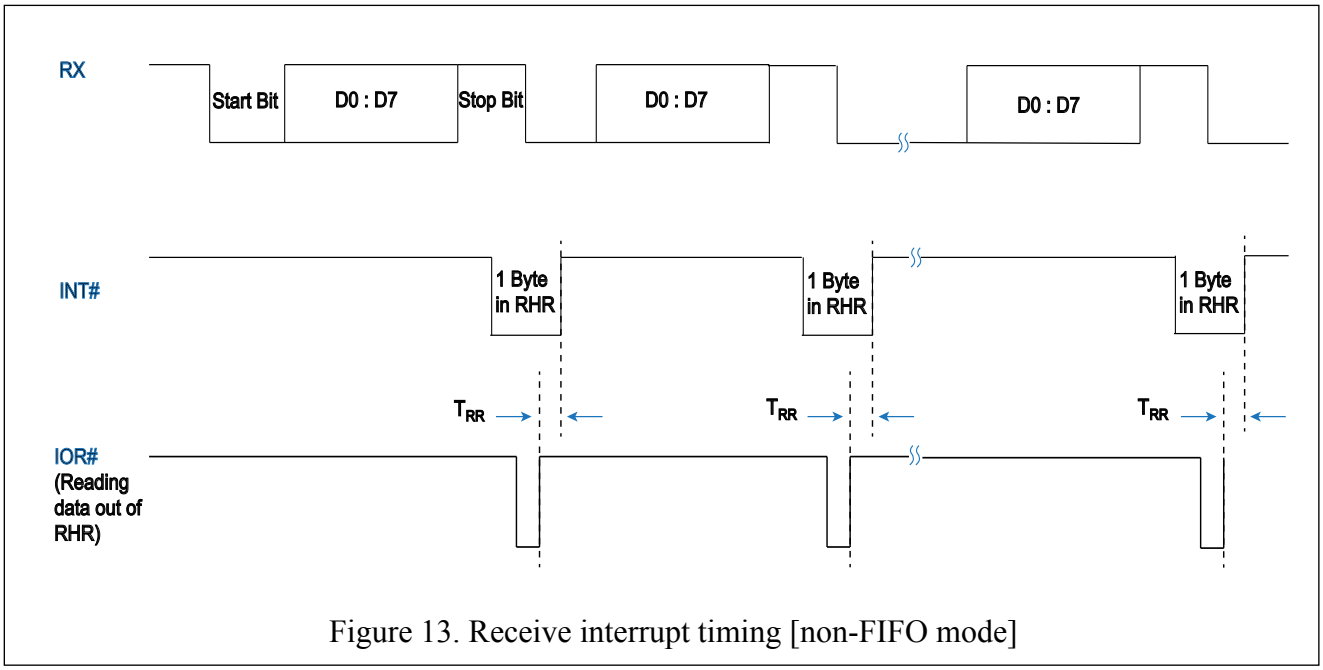


Figure 13. Receive interrupt timing [non-FIFO mode]

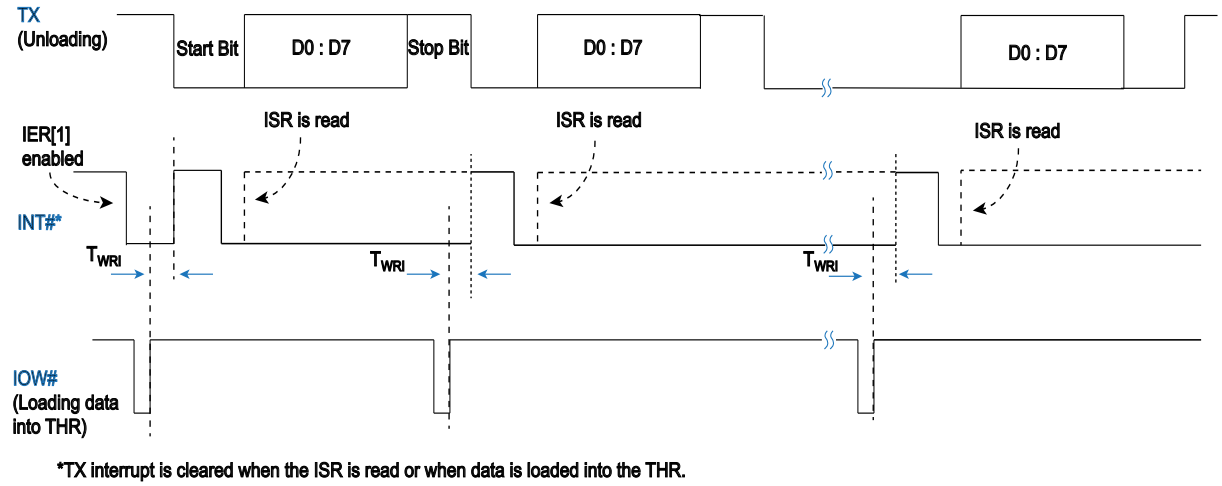


Figure 14. Transmit interrupt timing [non-FIFO mode]

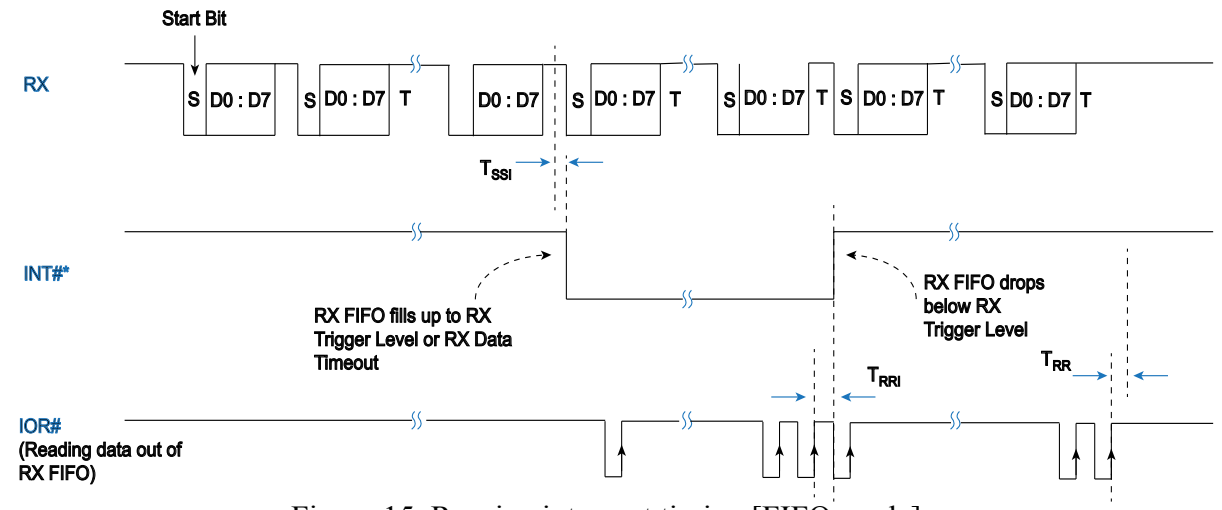


Figure 15. Receive interrupt timing [FIFO mode]

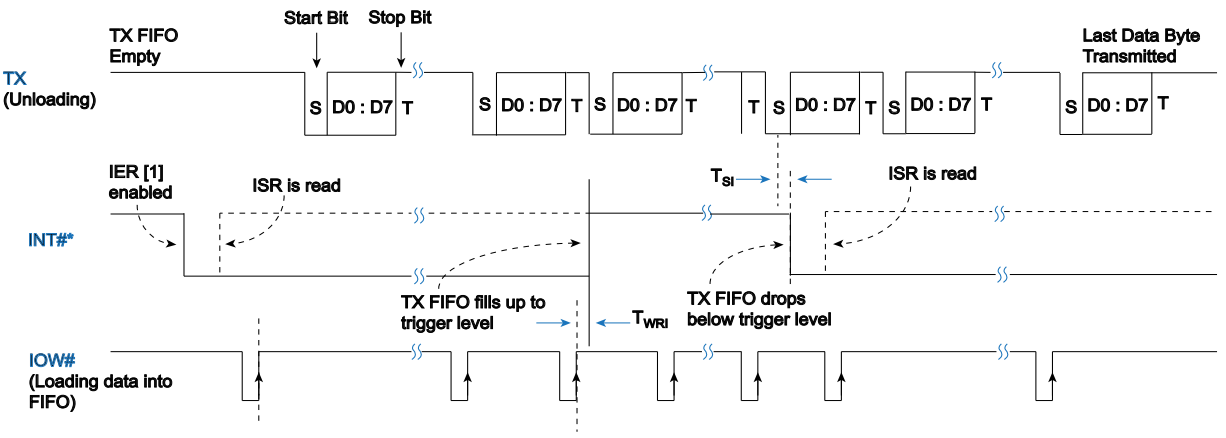
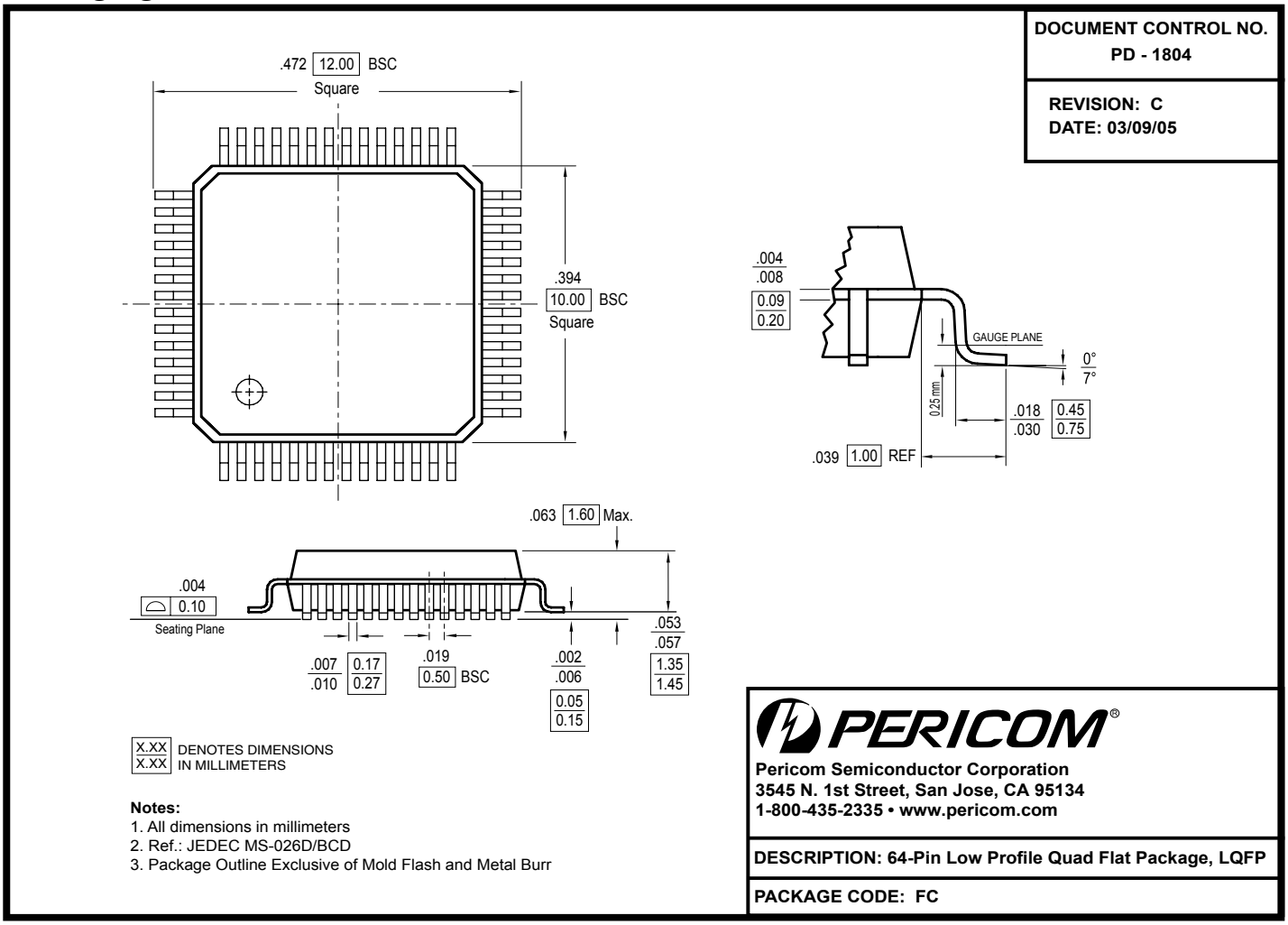


Figure 16. Transmit interrupt timing [FIFO mode]

Packaging Mechanical: 64-LQFP



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Ordering Information

Ordering Number	Package Code	Package Description
PI7C9X794FCEX	FC	64-Pin, Low Profile Quad Flat Package (LQFP)

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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Revision History

Data	Revision number	Description
10/27/2014	1.0	First Release
06/15/2017	1.1	Change Logo Updated Maximum Rating Table
10/25/2017	2	Revision numbering system changed to whole number