Continuous-Time Bipolar Switch

FEATURES AND BENEFITS

- Ideal for applications that require pulsing V_{CC} to conserve power
- Continuous-time operation
  - □ Fast power-on time
  - □ Low noise
- Stable operation over full operating temperature range
- Reverse battery protection
- Solid-state reliability
- Factory-programmed at end-of-line for optimum performance
- Robust EMC performance
- High ESD rating
- Regulator stability without a bypass capacitor

PACKAGES:

Not to scale

3-pin SOT23W
(suffix LH)

3-pin SIP,
matrix HD style
(suffix UA)

3-pin SIP,
chopper style
(suffix UA)

DESCRIPTION

The Allegro™ A1205 Hall-effect bipolar switch is a next-generation replacement and extension of the popular Allegro A3134 bipolar switch. The A1205 has identical specifications as the A1201 but is recommended for applications that require pulsing V_{CC} to conserve power. For standard applications, where V_{CC} is constant, please refer to the A1201 through A1204 devices.

Overall, the A120x family, produced with BiCMOS technology, consists of continuous-time devices that feature fast power-on time and low-noise operation. Device programming is performed after packaging to ensure increased switchpoint accuracy by eliminating offsets that can be induced by package stress. Unique Hall element geometries and low-offset amplifiers help to minimize noise and to reduce the residual offset voltage normally caused by device overmolding, temperature excursions, and thermal stress.

The A120x Hall-effect bipolar switches include the following on a single silicon chip: voltage regulator, Hall-voltage generator, small-signal amplifier, Schmitt trigger, and NMOS output transistor. The integrated voltage regulator permits operation from 3.8 to 24 V. The extensive on-board protection circuitry makes possible a ±30 V absolute maximum voltage rating for superior protection in automotive and motor commutation applications, without adding external components.

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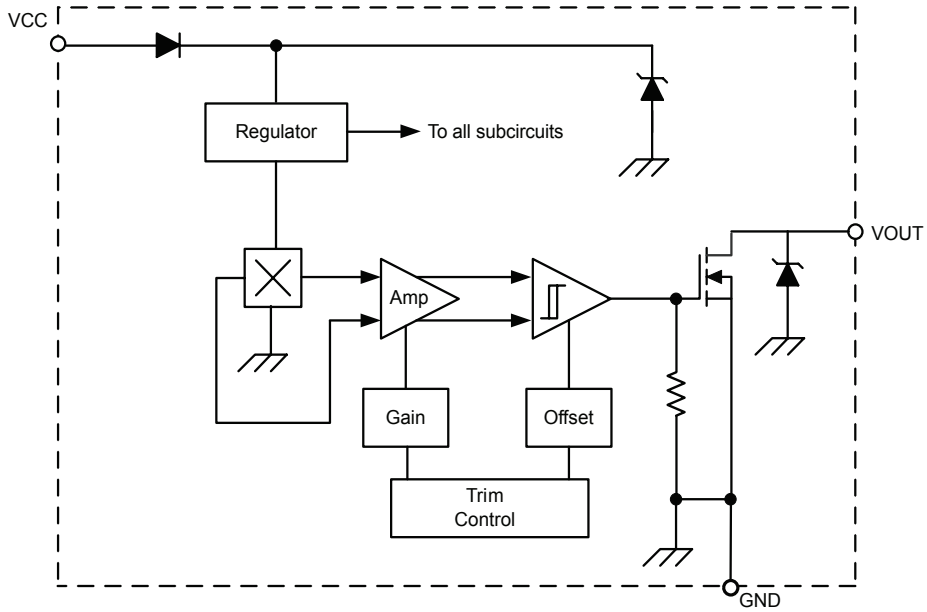


Functional Block Diagram

DESCRIPTION (continued)

The small geometries of the BiCMOS process allow these devices to be provided in ultrasmall packages. The package styles available provide magnetically optimized solutions for most applications. Package LH is a SOT23W miniature thin-profile surface-mount package, while package UA is a three-lead ultramini SIP for through-hole mounting. Each package is lead (Pb) free, with 100% matte-tin-plated leadframes.

SPECIFICATIONS

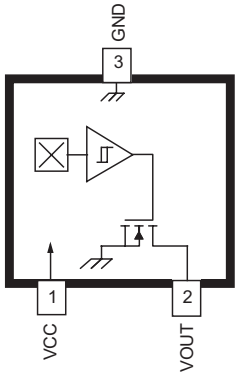
SELECTION GUIDE

Part Number	Packing [1]	Mounting	Ambient, T_A	B_{RP} (Min)	B_{OP} (Max)
A1205LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40°C to 150°C	–50 G	50 G
A1205LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1205LUA-T [2]	Bulk, 500 pieces/bag	3-pin SIP through hole			

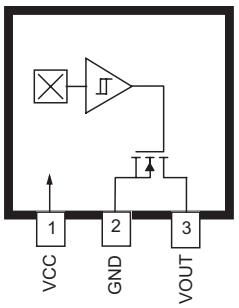
[1] Contact Allegro for additional packing options.
[2] The chopper-style UA package is not for new design; the matrix HD style UA package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		–30	V
Output Off Voltage	V_{OUT}		30	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Current Sink	$I_{OUTSINK}$		25	mA
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C



Package LH Pin-out Diagram



Package UA Pin-out Diagram

Terminal List

Number		Name	Description
Package LH	Package UA		
1	1	VCC	Connects power supply to chip
2	3	VOUT	Output from circuit
3	2	GND	Ground

OPERATING CHARACTERISTICS: over full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}	Operating, T_J < 165°C	3.8	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RP}	–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	215	400	mV
Power-On Time [2]	t_{PO}	Slew rate (dV_{CC}/dt) < 2.5 V/µs, B > B_{OP} + 5 G or B < B_{RP} – 5 G	–	–	4	µs
Output Rise Time [3]	t_r	V_{CC} = 12 V, R_{LOAD} = 820 Ω, C_S = 12 pF	–	–	2	µs
Output Fall Time [3]	t_f	V_{CC} = 12 V, R_{LOAD} = 820 Ω, C_S = 12 pF	–	–	2	µs
Supply Current	I_{CCON}	B > B_{OP}	–	3.8	7.5	mA
	I_{CCOFF}	B < B_{RP}	–	3.5	7.5	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –30 V	–	–	–10	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 30 mA; T_A = 25°C	32	–	40	V
Supply Zener Current	I_Z	V_Z = 32 V; T_A = 25°C	–	–	30	mA
MAGNETIC CHARACTERISTICS [4]						
Operate Point	B_{OP}	South pole adjacent to branded face of device	–40	15	50	G
Release Point	B_{RP}	North pole adjacent to branded face of device	–50	–15	40	G
Hysteresis	B_{HYS}	B_{OP} – B_{RP}	5	30	55	G

[1] Maximum voltage must be adjusted for power dissipation and junction temperature, see *Power Derating* section.
[2] For V_{CC} slew rates greater than 2.5 V/µs, and T_A = 150°C, the Power-On Time can reach its maximum value.
[3] C_S =oscilloscope probe capacitance.
[4] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity). Reference to the magnetic field polarity is with respect to the beveled face of the device.

DEVICE QUALIFICATION PROGRAM

Contact Allegro for information.

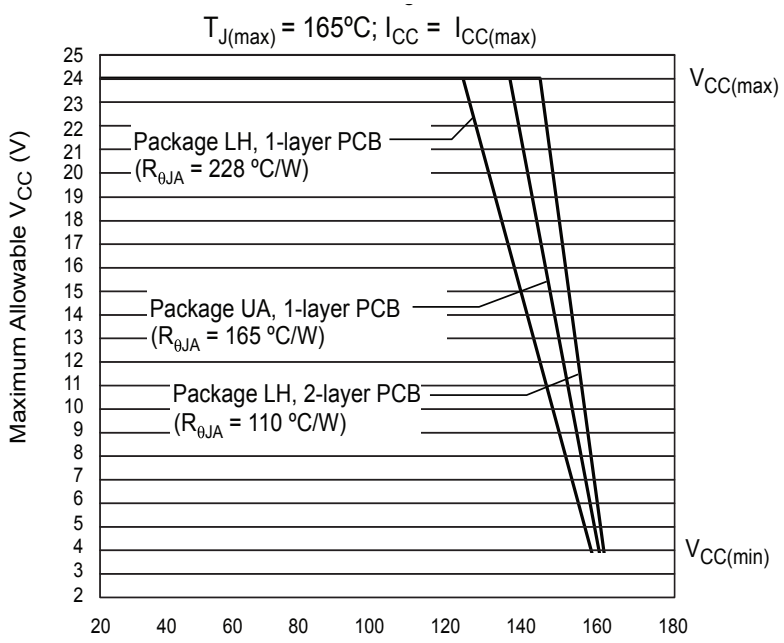
EMC (ELECTROMAGNETIC COMPATABILITY) REQUIREMENTS

Contact Allegro for information.

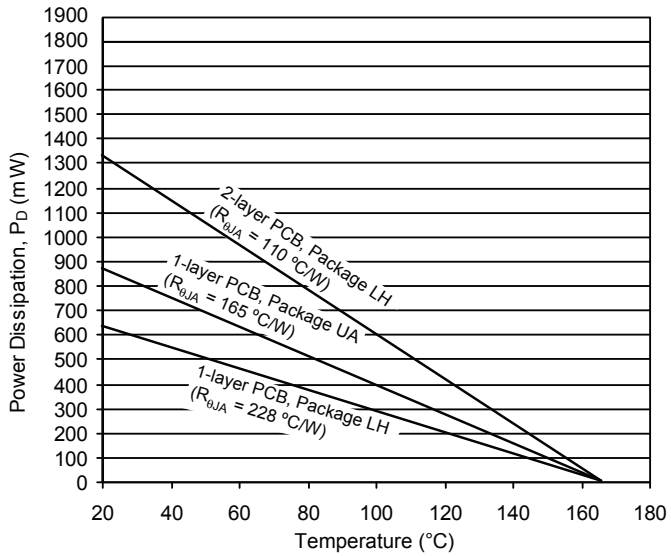
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on Allegro Web site.

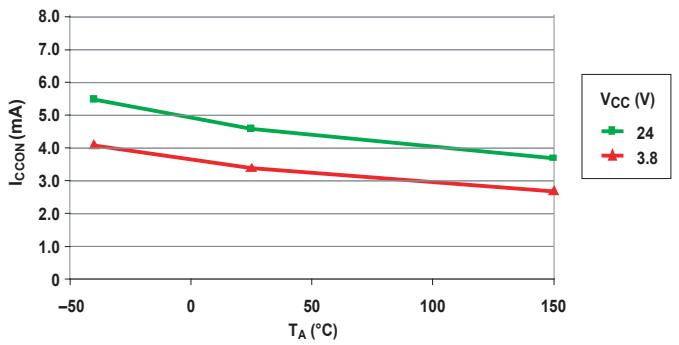


Power Dissipation versus Ambient Temperature

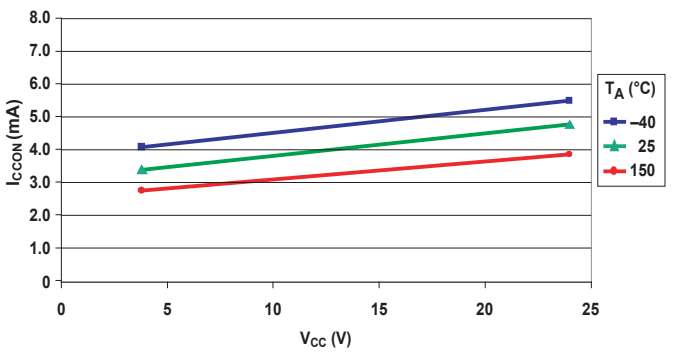


CHARACTERISTIC DATA

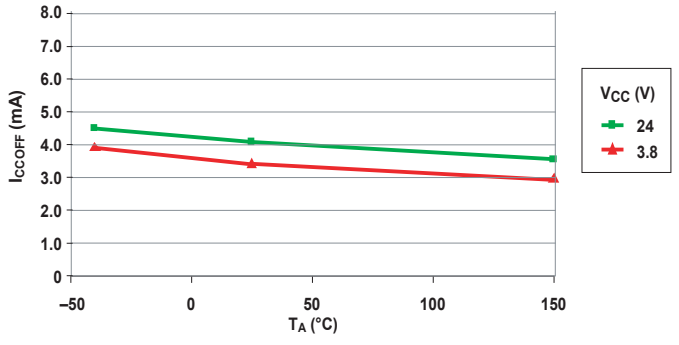
Supply Current (On) versus Ambient Temperature



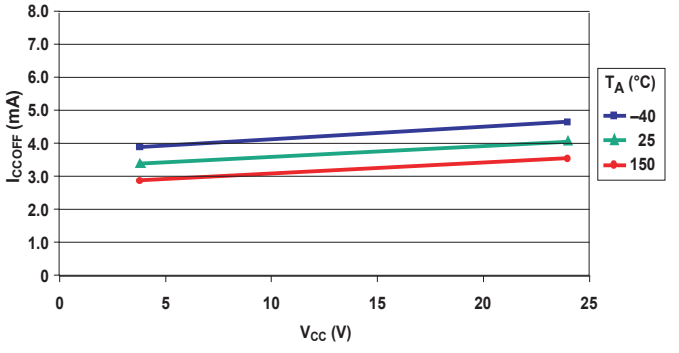
Supply Current (On) versus Supply Voltage



Supply Current (Off) versus Ambient Temperature

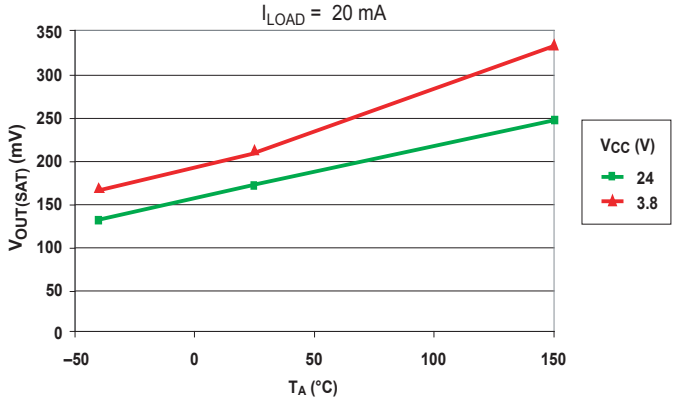


Supply Current (Off) versus Supply Voltage



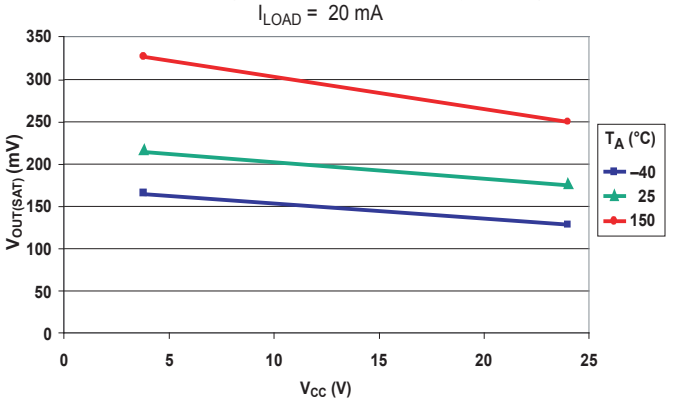
Output Voltage (On) versus Ambient Temperature

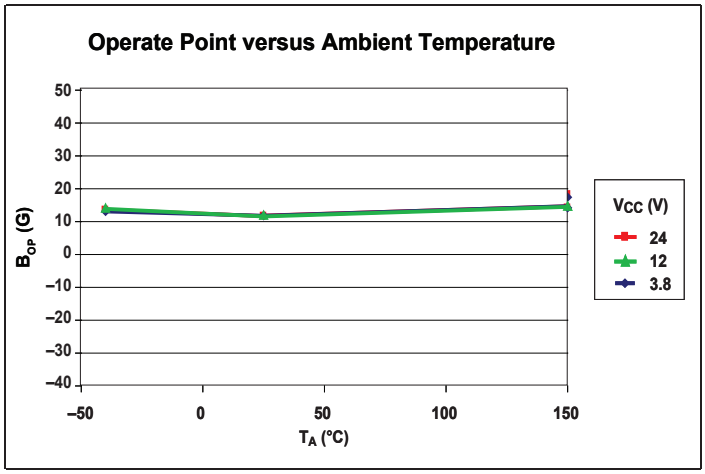
I_{LOAD} = 20 mA

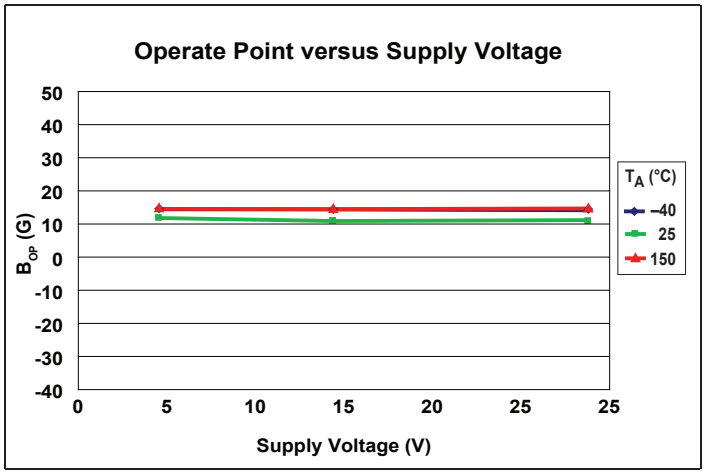


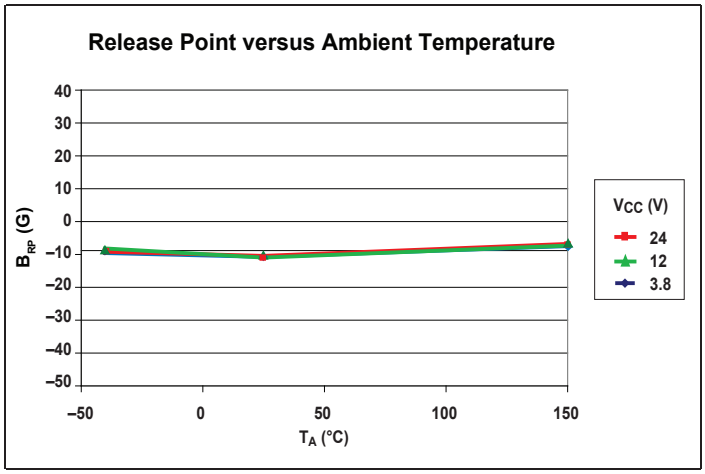
Output Voltage (On) versus Supply Voltage

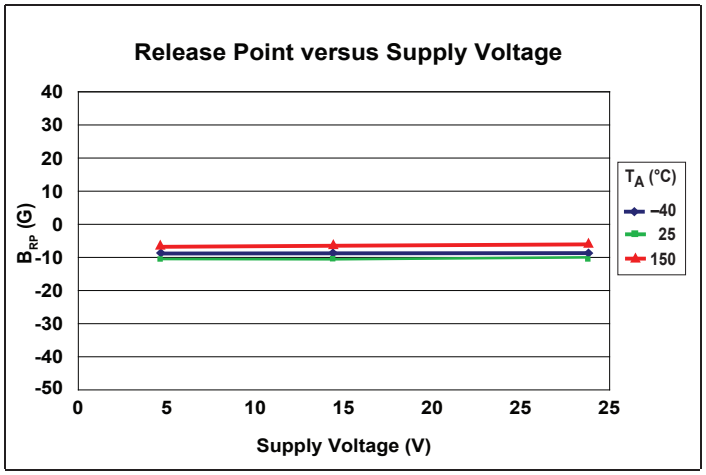
I_{LOAD} = 20 mA




Operate Point versus Ambient Temperature
B_{OP} (G)
50
40
30
20
10
0
–10
–20
–30
–40
–50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.8


Operate Point versus Supply Voltage
B_{OP} (G)
50
40
30
20
10
0
–10
–20
–30
–40
0
5
10
15
20
25
25
Supply Voltage (V)
T_A (°C)
–40
25
150


Release Point versus Ambient Temperature
B_{RP} (G)
40
30
20
10
0
–10
–20
–30
–40
–50
–50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.8


Release Point versus Supply Voltage
B_{RP} (G)
40
30
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0
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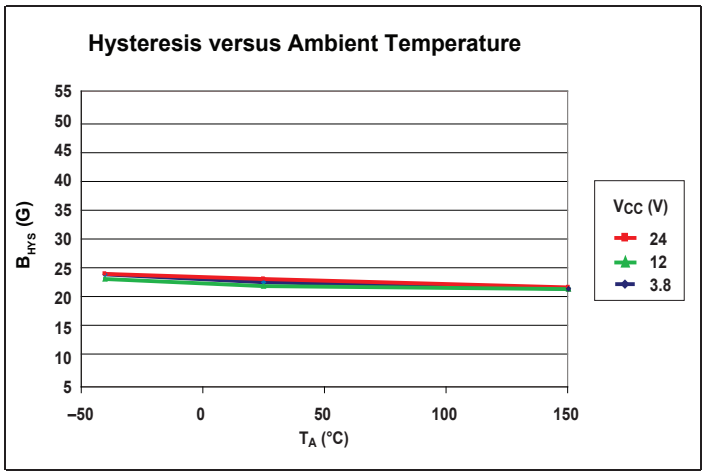
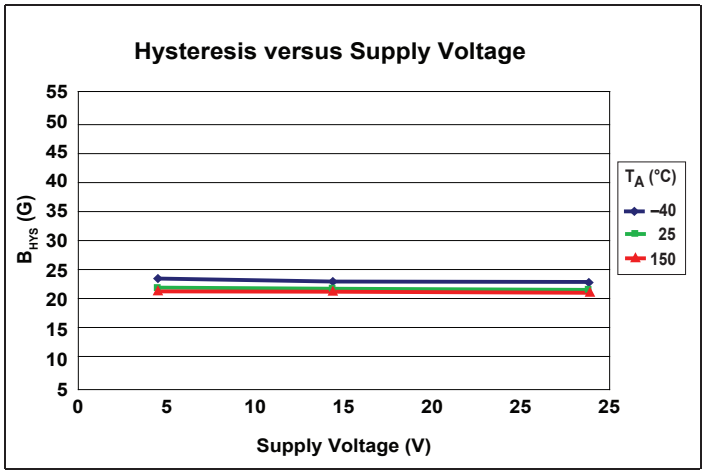
15
20
25
25
Supply Voltage (V)
T_A (°C)
–40
25
150


Hysteresis versus Ambient Temperature
B_{HYS} (G)
55
50
45
40
35
30
25
20
15
10
5
–50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.8


Hysteresis versus Supply Voltage
B_{HYS} (G)
55
50
45
40
35
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15
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5
0
5
10
15
20
25
25
Supply Voltage (V)
T_A (°C)
–40
25
150

FUNCTIONAL DESCRIPTION

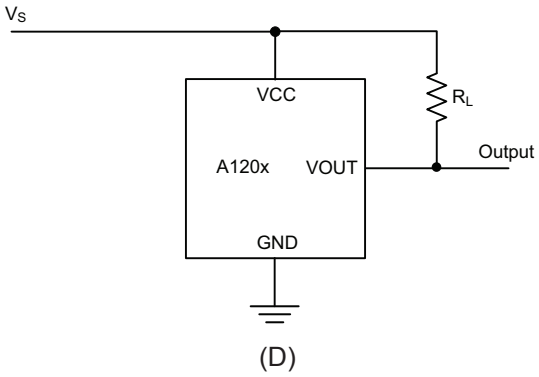
Bipolar Device Switching

The devices of the A120X family provide highly sensitive switching for applications using magnetic fields of alternating polarities, such as ring magnets. There are three switching modes for bipolar devices, referred to as *latch*, *unipolar switch*, and *negative switch*. Mode is determined by the switchpoint characteristics of the individual device. The characteristic hysteresis, B_{HYS}, of the device, is the difference in the relative magnetic strength and polarity of the switchpoints of the device. (Note that, in the following descriptions, a negative magnetic value indicates a north polarity field, and a positive magnetic value indicates a south polarity field. For a given value of magnetic strength, B_X, the values $-B_X$ and B_X indicate two fields of equal strength, but opposite polarity. B = 0 indicates the absence of a magnetic field.)

Bipolar devices typically behave as latches. In this mode, magnetic fields of opposite polarity and equivalent strengths are needed to switch the output. When the magnetic fields are removed ($B \rightarrow 0$) the device remains in the same state until a magnetic field of the opposite polarity and of sufficient strength causes it to switch. The hysteresis of latch mode behavior is shown in panel A of Figure 1.

In contrast to latching, when a device exhibits unipolar switching, it only responds to a south magnetic field. The field must be of sufficient strength, > B_{OP}, for the device to operate. When the field is reduced beyond the B_{RP} level, the device switches back to the high state, as shown in panel B of Figure 1. Devices exhibiting negative switch behavior operate in a similar but opposite manner. A north polarity field of sufficient strength, > B_{RP}, (more north than B_{RP}) is required for operation, although the result is that V_{OUT} switches high, as shown in panel C. When the field is reduced beyond the B_{OP} level, the device switches back to the low state.

The typical output behavior of the A120x devices is latching. However, the A120x family is designed to attain a small hysteresis, and thereby provide more sensitive switching. Although this means that true latching behavior cannot be guaranteed in all cases, proper switching can be ensured by use of both south and north magnetic fields, as in a ring magnet. The hysteresis of the A120x family allows clean switching of the output, even in the presence of external mechanical vibration and electrical noise.



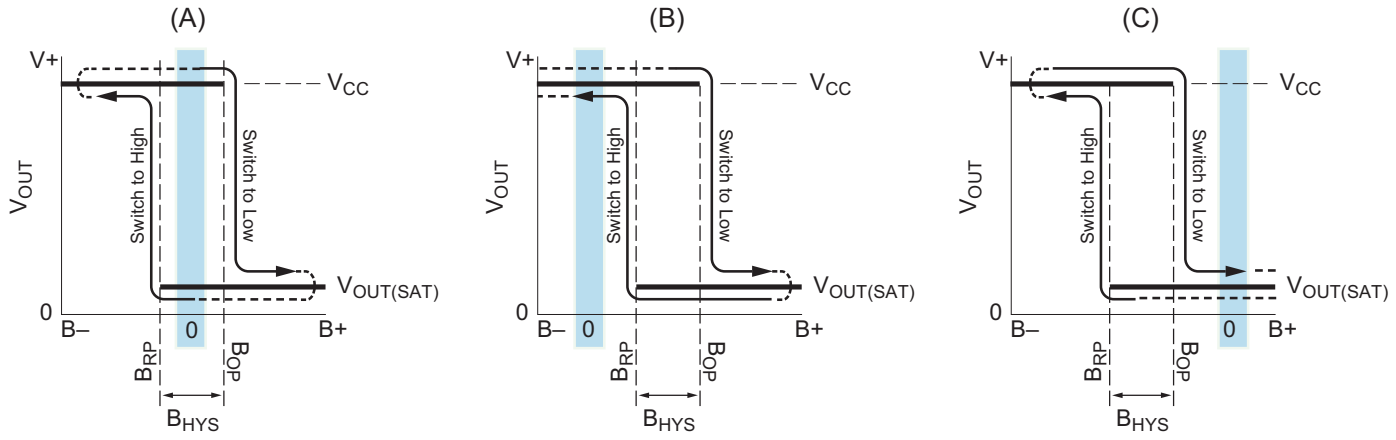


Figure 1: Bipolar Device Output Switching Modes

These behaviors can be exhibited when using a circuit such as that shown in panel D. Panel A displays the hysteresis when a device exhibits latch mode (note that the B_{HYS} band incorporates B= 0), panel B shows unipolar switch behavior (the B_{HYS} band is more positive than B = 0), and panel C shows negative switch behavior (the B_{HYS} band is more negative than B = 0). Bipolar devices, such as the 120x family, can operate in any of the three modes.

Bipolar devices adopt an indeterminate output state when powered-on in the absence of a magnetic field or in a field that lies within the hysteresis band of the device.

For more information on Bipolar switches, refer to Application Note 27705, *Understanding Bipolar Hall Effect Sensor ICs*.

CONTINUOUS-TIME BENEFITS

Continuous-time devices, such as the A120x family, offer the fastest available power-on settling time and frequency response. Due to offsets generated during the IC packaging process, continuous-time devices typically require programming after packaging to tighten magnetic parameter distributions. In contrast, chopper-stabilized switches employ an offset cancellation technique on the chip that eliminates these offsets without the need for after-packaging programming. The tradeoff is a longer settling time and reduced frequency response as a result of the chopper-stabilization offset cancellation algorithm.

The choice between continuous-time and chopper-stabilized designs is solely determined by the application. Battery management is an example where continuous-time is often required. In these applications, V_{CC} is chopped with a very small duty cycle in order to conserve power (refer to figure 2). The duty cycle is controlled by the power-on time, t_{PO}, of the device. Because continuous-time devices have the shorter power-on time, they are the clear choice for such applications.

For more information on the chopper stabilization technique, refer to Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers with a Track-and-Hold Signal Demodulator*.

ADDITIONAL APPLICATIONS INFORMATION

Extensive applications information for Hall-effect devices is available in:

• *Hall-Effect IC Applications Guide*, Application Note 27701

• *Hall-Effect Devices: Gluing, Potting, Encapsulating, Lead Welding and Lead Forming*, Application Note 27703.1

• *Soldering Methods for Allegro's Products – SMT and Through-Hole*, Application Note 26009

All are provided on the Allegro website, www.allegromicro.com.

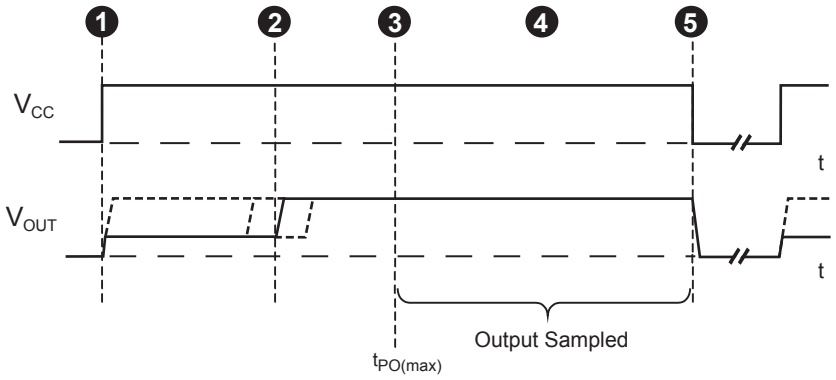


Figure 2: Continuous-Time Application, B < B_{RP}

This figure illustrates the use of a quick cycle for chopping V_{CC} in order to conserve battery power. Position 1, power is applied to the device. Position 2, the output assumes the correct state at a time prior to the maximum Power-On Time, $t_{PO(max)}$. The case shown is where the correct output state is HIGH. Position 3, $t_{PO(max)}$ has elapsed. The device output is valid. Position 4, after the output is valid, a control unit reads the output. Position 5, power is removed from the device.

POWER DERATING

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165°C/W, $T_{J(max)}$ =165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 7.5 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165°C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91\ mW \div 7.5\ mA = 12.1\ V$$

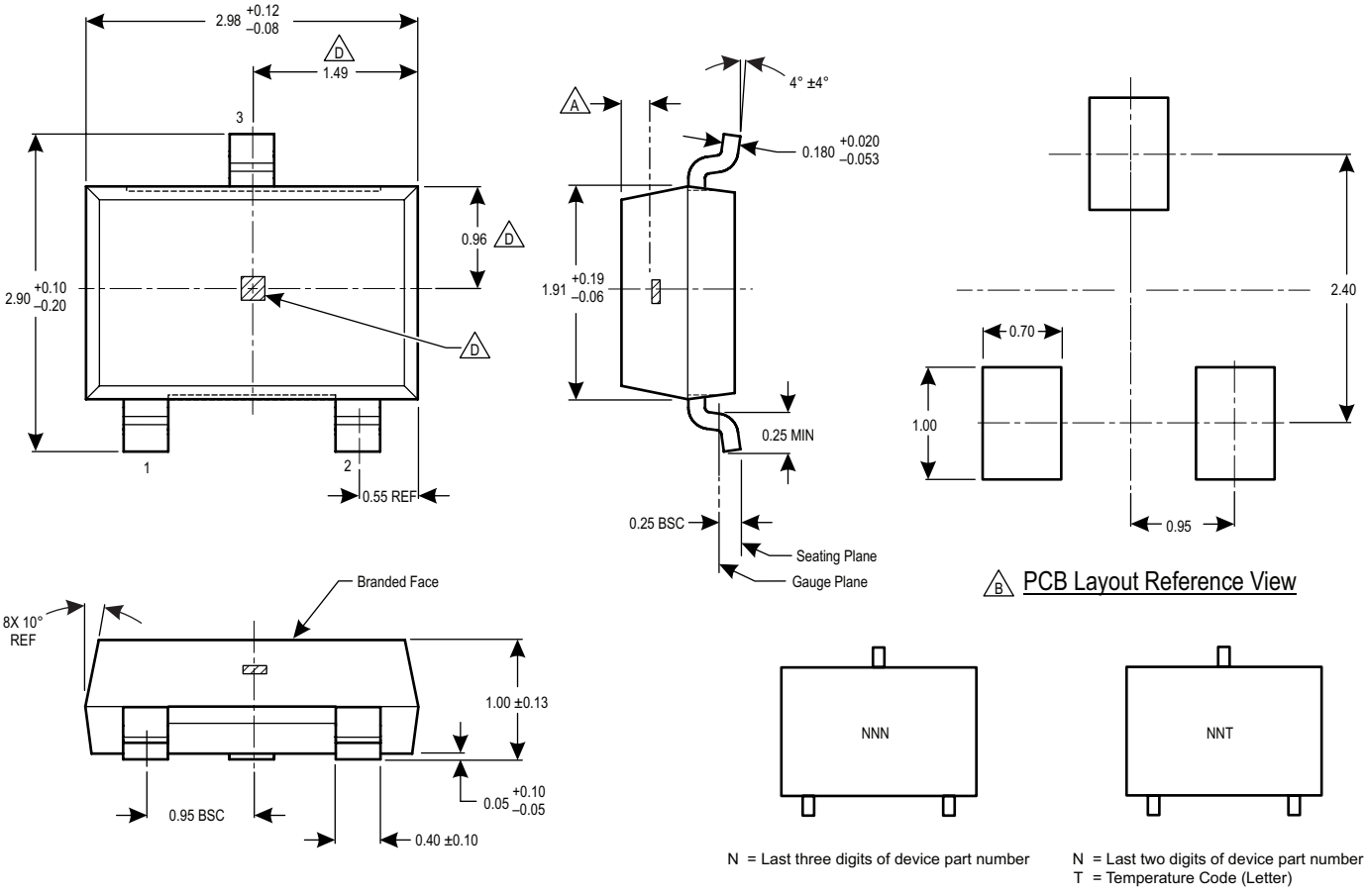
The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \le V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \ge V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

CUSTOMER PACKAGE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-2840)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.28 mm

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 3: Package LH, 3-Pin (SOT-23W)

For Reference Only – Not for Tooling Use

(Reference DWG-9049)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

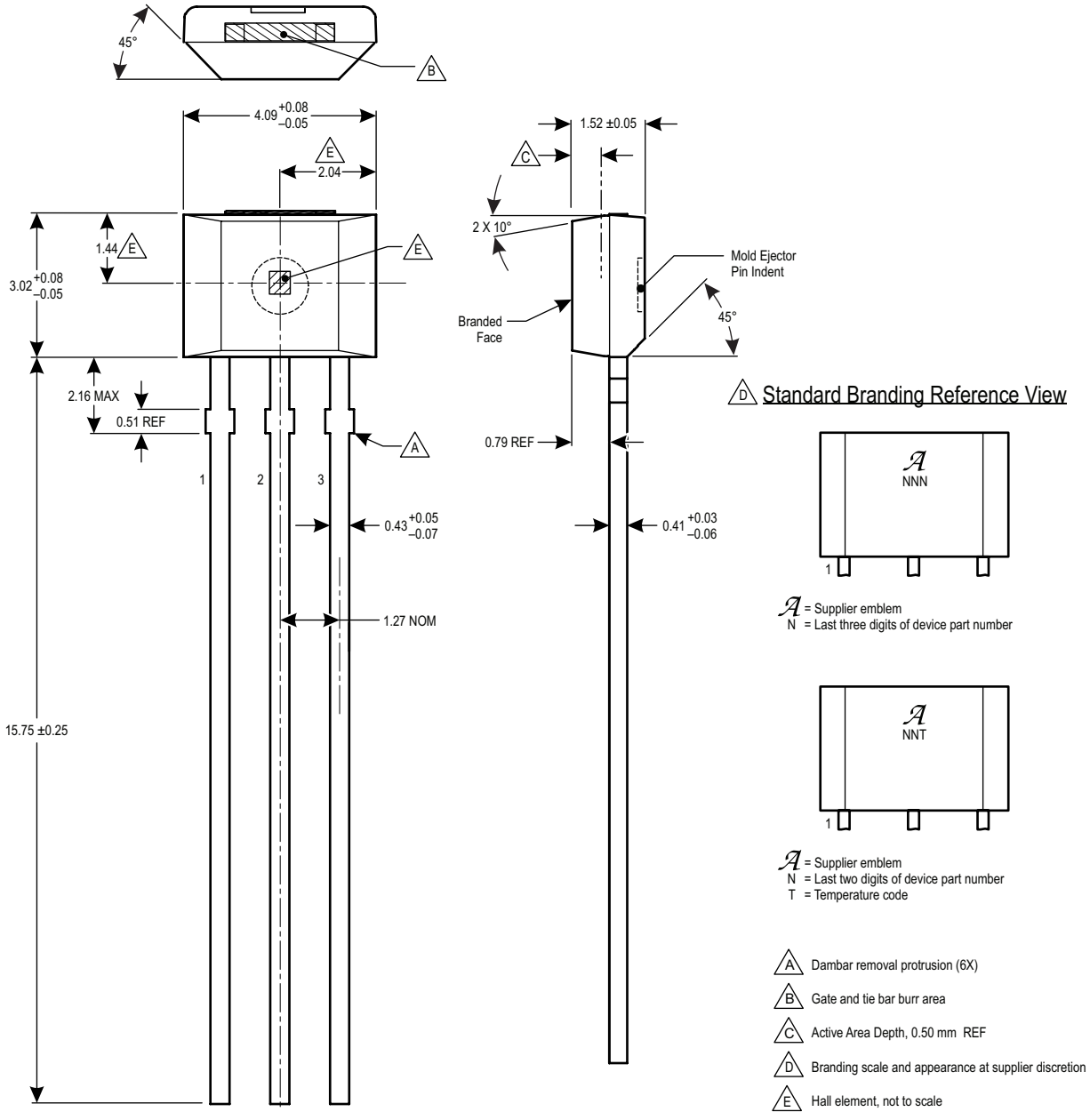


Figure 4: Package UA, 3-Pin SIP, Matrix Style

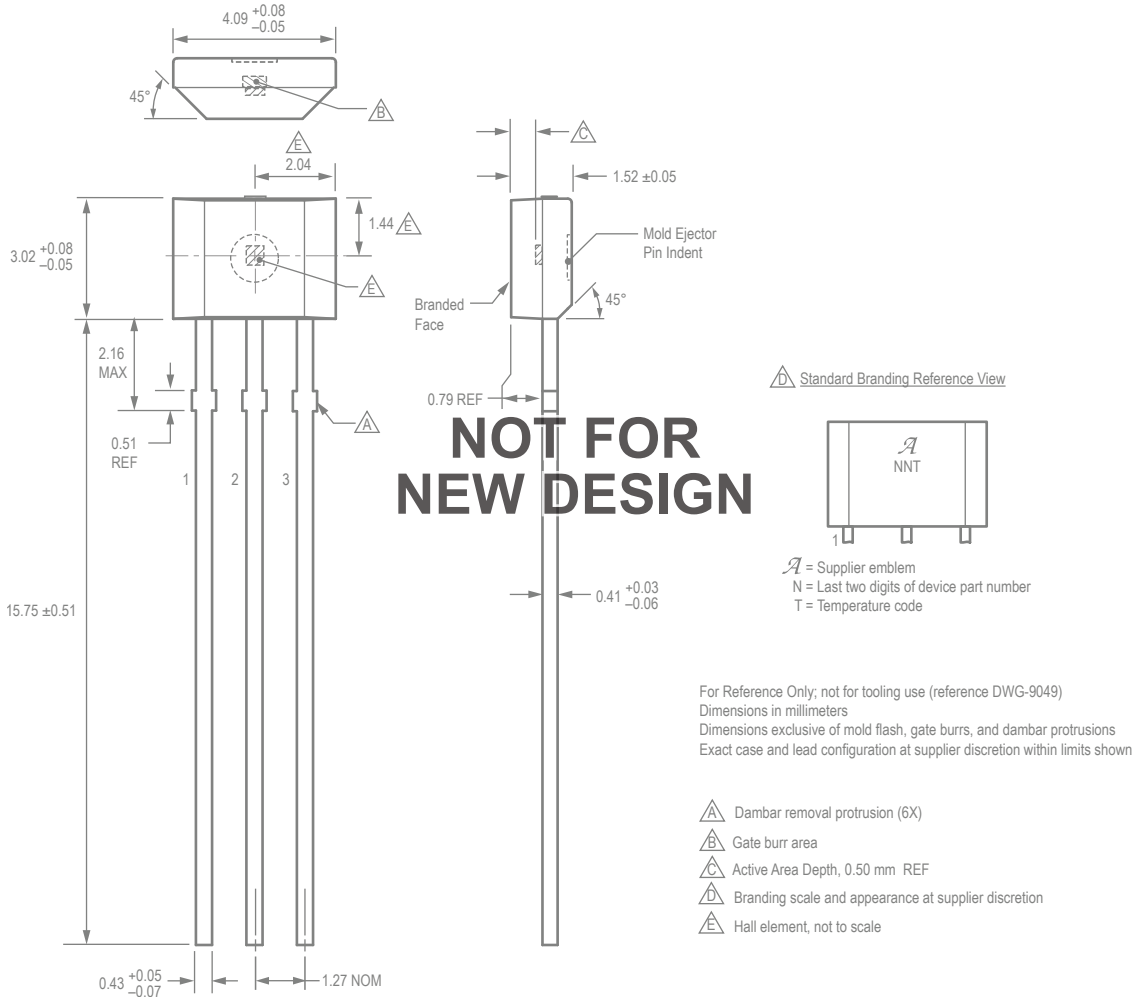


Figure 5: Package UA, 3-Pin SIP, Chopper Style

Revision History

Number	Date	Description
8	January 1, 2015	Added LX option to Selection Guide
9	July 13, 2015	Corrected LH package Active Area Depth value
10	November 4, 2016	Chopper-style UA package designated as not for new design

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