AK2330

DAC Type 8-bit 8-channel Electronic Volume

Features

□ 8-bit 8 channels of built-in multiplication D/A converters

□ Support for external one-path, internal three-path D/A converter reference voltages

□ Built-in buffer amplifier with low distortion (-60dB typ.) and rail-to-rail operation

□ Support for 3V control and 5V operation because of the three-wire serial system with separate power supplies

□ Operating voltage range: 2.6 to 5.5V

□ Operating temperature range: -40 to +85°C

□ Package： 24-pin QFNJ (4.0mm x 4.0mm x 0.75mm, 0.5-mm pitch)

Overview

   The AK2330 is an electronic volume into which 8 bit 8 channels of multiplication D/A converters are integrated on a single chip.

The reference voltage of the D/A converter can be selected from one external path (VREF pin level) and internal three paths (VSS, AVDD, AVDD/2) for each channel and it can be used as a normal D/A converter or an electronic volume that attenuates signals from input pins VIN0 to VIN7.   A buffer amplifier is incorporated as the subsequent stage of the D/A converter, which provides rail-to-rail output and a signal with a distortion of -60dB.
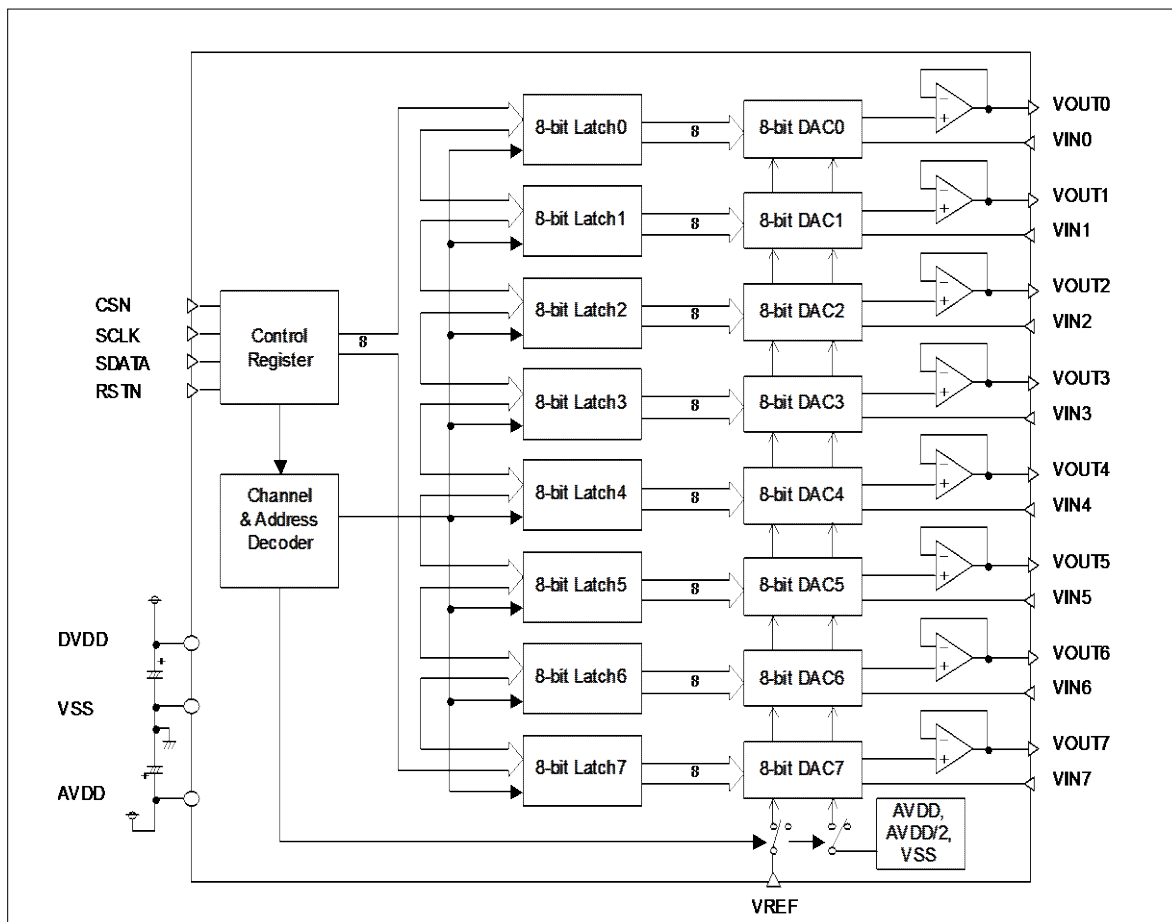
   In operational setting, the three-wire serial system, which synchronizes serial input (SDATA) consisting of a 4-bit address and 8-bit data with the CSN and SCLK signals, is adopted, a power supply (DVDD) is provided separately from the D/A converter, and 3V serial control and 5V D/A converter operation are enabled.   In addition, settings can be made so that the AVDD/2 level, which was generated internally, is output to VOUT0 to VOUT7 pins through the buffer amplifier by bypassing the D/A converter or the buffer amplifier is powered down.

   A 24-pin small and low-profile QFNJ package (4.0mm square x 0.75mm height) is employed to achieve high-density packaging.
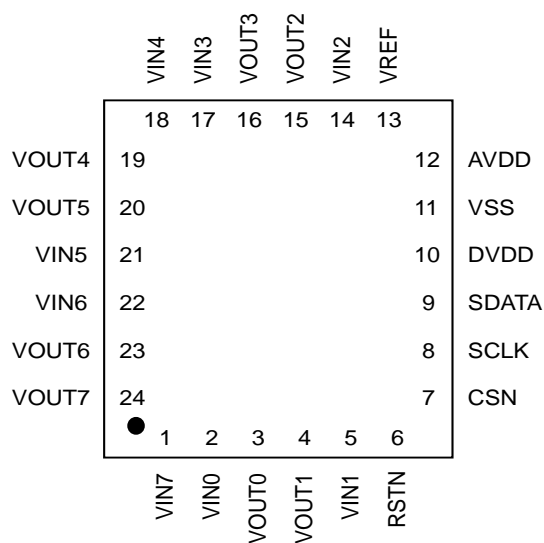
Contents

Block Diagram

Pin Assignments

Pin assignments (top view)

Block Functions

Block	Function
Control register	The control register inputs serial data (SDATA) consisting of a 4-bit address and 8-bit data in sync with the CSN and SCLK signals to set register data. When a system reset is performed through the RSTN pin on power-up, all registers are initialized. The same reset (soft reset) can also be made by the SRST register (refer to register descriptions).
Channel & address decoder	The channel & address decoder decodes the data set by the control register and sets the corresponding D/A converter and reference voltage.
8-bit Latch0 to Latch7	The 8-bit Latch0 to Latch7 store the register data of the control register.
8-bit DAC0 to DAC7	The 8-bit DAC0 to DAC7 are 8-bit D/A converters set by the data latched in the previous stage.
Buffer	The buffer is a buffer amplifier that performs rail-to-rail operation.

Pin Functions

Pin No.	Pin name	Pin type	Pin status at system reset	Function
6	RSTN	DI	Z	Reset pin
7	CSN	DI	Z	Chip select input pin for serial interface data
8	SCLK	DI	Z	Clock input pin for serial interface data
9	SDATA	DI	Z	I/O pin for serial interface data
10	DVDD	PWR	-	Digital VDD power supply pin Connect this pin to a 2.6 to 5.5V power supply. Connect a bypass capacitor of $0.1\mu F$ or greater between this pin and the VSS pin.
11	VSS	PWR	-	VSS power supply pin Always apply a voltage of 0V to this pin.
12	AVDD	PWR	-	Analog VDD power supply pin Connect this pin to a 2.6 to 5.5V power supply. Connect a bypass capacitor of $0.1\mu F$ or greater between this pin and the VSS pin. Apply a voltage so that DVDD is equal to or less than AVDD.
13	VREF	AI	Z	D/A converter reference voltage input pin
2	VIN0	AI	L	D/A converter input pin
5	VIN1	AI	L	
14	VIN2	AI	L	
17	VIN3	AI	L	
18	VIN4	AI	L	
21	VIN5	AI	L	
22	VIN6	AI	L	
1	VIN7	AI	L	
3	VOUT0	AO	Z	D/A converter/buffer amplifier output pin
4	VOUT1	AO	Z	
15	VOUT2	AO	Z	
16	VOUT3	AO	Z	
19	VOUT4	AO	Z	
20	VOUT5	AO	Z	
23	VOUT6	AO	Z	
24	VOUT7	AO	Z	

Note   **A**: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output, **Z**: High-Z, **L**: Low

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	AVDD	-0.3	6.5	V
	DVDD	-0.3	6.5	V
Ground level	VSS	0	0	V
Input voltage	V_{IN}	-0.3	AVDD+0.3 DVDD+0.3	V
Input current (excluding power pins)	I_{IN}	-10	+10	mA
Storage temperature	T_{stg}	-55	130	°C

Note   All voltages are relative to the VSS pin.

Caution   If the device is used in conditions exceeding these values, the device may be destroyed. Normal operation is not guaranteed in such extreme conditions.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature	Ta		-40		+85	°C
Operating power supply voltage	AVDD		2.6	5.0	5.5	V
	DVDD	DVDD ≤ AVDD	2.6	5.0	5.5	V
Analog output load capacity	AOC				100	pF

Note   All voltages are relative to the VSS pin.

Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	SIDD	DVDD = AVDD = 5V VIN = AVDD, DAREF:VSS (On a system reset)		1	20	µA
	IDD1	DVDD = AVDD = 5V VIN = AVDD, DAREF:VSS VOUT[7:0] = 0x80		1.2	2.4	mA
	IDD2	DVDD = AVDD = 5V VIN = AVDD, DAREF:AVDD/2 VOUT[7:0] = 0x00		1.5	3.0	mA

Note   DACREF shows the internal setting level of DAC reference voltage. Current consumption does not include VIN pins input current and output load current.

Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	CSN, SCLK, SDATA, RSTN	0.8DVDD			V
Low level input voltage	V_{IL}	CSN, SCLK, SDATA, RSTN			0.2DVDD	V
High level input current	I_{IH}	V_{IH} = DVDD CSN, SCLK, SDATA, RSTN			1	μA
Low level input current	I_{IL}	V_{IL} = 0V CSN, SCLK, SDATA, RSTN	-1			μA

System Reset

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Hardware reset signal input width	t_{RSTN}	RSTN pin	1			μs	*1)
Software reset		SRST register					*2)

*1) 35ms or more after power-on, be sure to perform a hardware reset operation (register initialization). When a low pulse is input for 1μs or more, a reset is made.   At this time, set the digital input (DI) pins: RSTN to high, CSN to high, and SCLK to low.
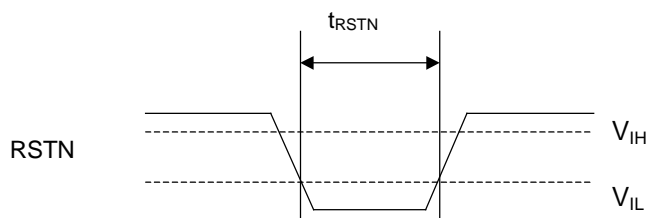
*2) When the SRST[7:0] register is set to 0xAA (10101010), a software reset is made. This setting initializes all registers. For details, refer to "Register Functions".

Analog Characteristics

Unless otherwise specified, the following apply: AVDD = 4.5 to 5.5V, VSS = 0V, AVDD $\geq$ VIN, VREF = 0V to AVDD, Ta = -40 to +85°C.

DACREF shows an internal setting level of DAC reference voltage.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VREF pin leak current	I$_{VREF}$	VIN = AVDD = 5V VREF = 0V			10	μA
VREF pin input voltage range	V$_{VREF}$	VIN = AVDD = 5V	0.2		AVDD-0.2	V
Resolution	RES			8		bit
Differential nonlinearity	DNL	VIN = AVDD = 5V DACREF: VSS |IAO| = 0μA VOUT = 0x02 to 0xFF	-1		+1	LSB
Nonlinearity *1)	INL		-1.5		+1.5	LSB
Buffer amplifier output voltage range	VAO1	|IAO| = 0μA VIN = AVDD, DACREF: VSS VOUT[7:0] = 0x00			0.1	V
		|IAO| = 0μA VIN = AVDD, DACREF:VSS VOUT[7:0] = 0xFF	AVDD-0.1			V
	VAO2	|IAO| $\leq$ 1mA VIN = AVDD, DACREF: VSS VOUT[7:0] = 0x00			0.4	V
		|IAO| $\leq$ 1mA VIN = AVDD, DACREF: VSS VOUT[7:0] = 0xFF	AVDD-0.4			V
AVDD/2 output voltage when AVDD2O[7:0] is set	VAO3	AVDD = 5V, |IAO| $\leq$ 1mA	2.45	2.5	2.55	V
Maximum input frequency	FIN	AVDD = 5V, DACREF: AVDD/2 VIN = 3Vp-p, 10kHz VOUT[7:0] = 0xFF RL = 22kΩ, CL = 100pF	2.7	3.0		Vp-p
Output distortion	SINAD	AVDD = 5V, DACREF: AVDD/2 VIN = 3Vp-p, 1kHz VOUT[7:0]=0x0A to 0xFF RL = 22kΩ, CL = 100pF 30kHz LPF used *4)	56	60		dB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DAC output settling time	t_{LDD1}	VOUT[7:0] = 0x10↔0xEF Until output reaches the half LSB of the final value. RS = 2.2kΩ, RL = 22kΩ, CL = 1000pF *3)			300	μs
VIN pin input impedance	R_{IN}			135		kΩ
VOUT pin output impedance	R_{OUT}			20		Ω

*1) Error between the I/O curve and the ideal line connecting the output voltage for the 02 setting and the output voltage for the FF setting.

Unless otherwise specified, the following apply: AVDD = 2.6 to 3.3V, VSS = 0V, AVDD ≥ VIN, VREF = 0V to AVDD, Ta = -40°C to +85°C
DACREF shows an internal setting level of DAC reference voltage.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	RES			8		bit
Differential nonlinearity	DNL	VIN = AVDD = 3V DACREF: VSS	-1		+1	LSB
Nonlinearity *2)	INL	|IAO| = 0μA VOUT = 0x02 to 0xFF	-1.5		+1.5	LSB
Buffer amplifier output voltage range	VAO4	|IAO| ≤ 600μA VIN = AVDD, DACREF: VSS VOUT[7:0] = 0x00			0.4	V
		|IAO|≤ 600μA VIN = AVDD, DACREF: VSS VOUT[7:0] = 0xFF	AVDD-0.4			V
Output distortion	DISTN	AVDD = 3V, DACREF: AVDD/2 VIN = 1.8Vp-p, 1kHz VOUT[7:0]=0x0A to 0xFF RL = 22kΩ, CL = 100pF 30kHz LPF used *4)	45	55		dB

*2) Error between the I/O curve and the ideal line connecting the output voltage for the 02 setting and the output voltage for the FF setting.

*3) Load condition when AK2330 is used as DAC
(Load condition when "DAC output settling time" is measured)

R   RS=2.2kΩ

CL=1000pF   RL=22kΩ

VOUT0...7

LSI
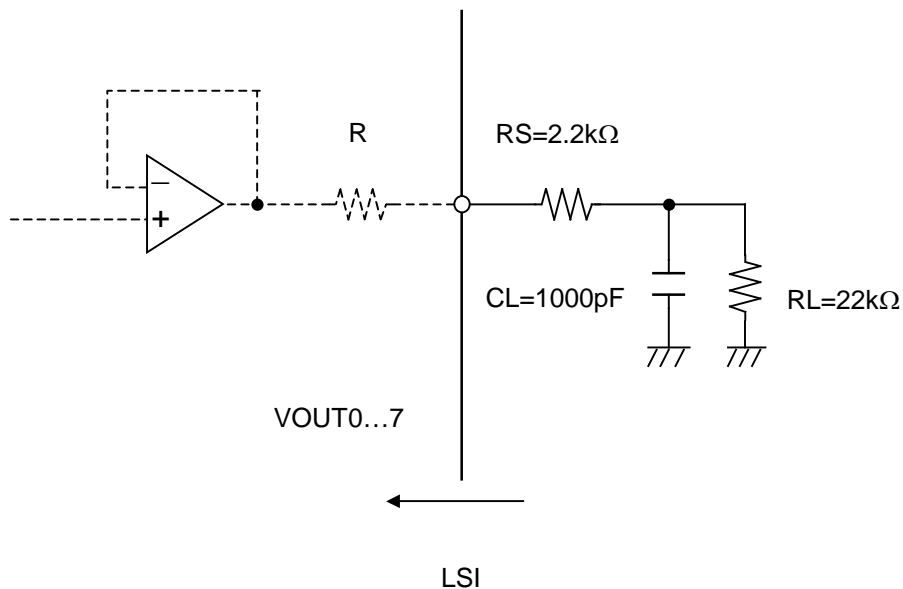
*4) Load condition when AK2330 is used as Attenuator
(Load condition when "Output distortion" is measured)

R

CL=100pF   RL=22kΩ

VOUT0...7

LSI
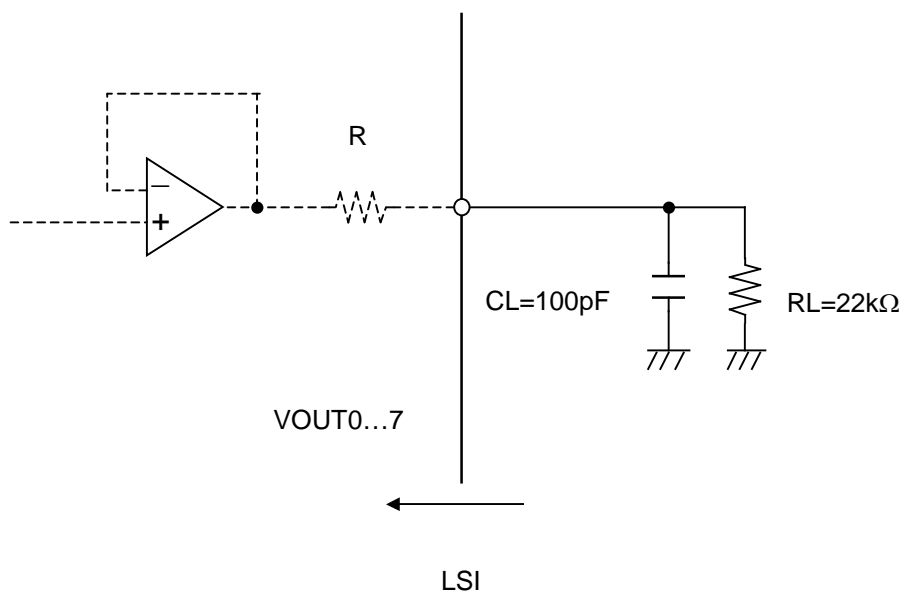
Digital AC Timing

Serial interface timing

The AK2330 writes data via the three-wire synchronous serial interface by means of CSN, SCLK, and SDATA.

SDATA (serial data) consists of a register address (starting from the MSB, A3 to A0) and control data (starting from the MSB, D7 to D0).

<1> CSN (chip select) is normally set to the high level.
When CSN is set to the low level, the serial interface becomes active.

<2> When a write operation is performed, an address and data are input in synchronization with the rising edges of 12 SCLK clock pulses while CSN is low.

<3> A write setting is made on the assumption that 12 clock pulses are input from SCLK while CSN is low.
Note that if clock pulses more than or less than 12 clock pulses are input, data cannot be set correctly.
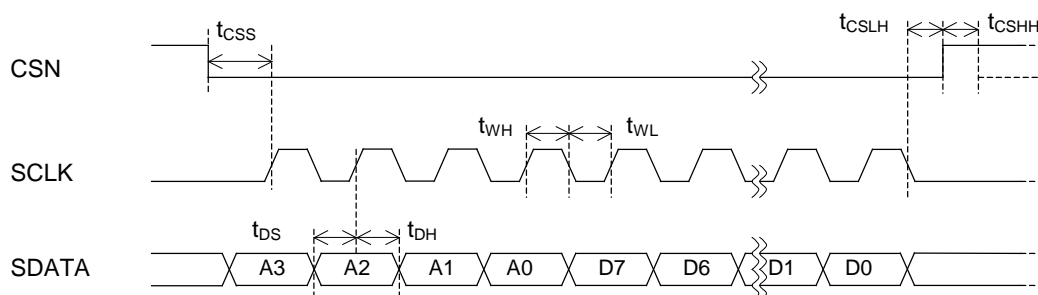
Rising and falling times
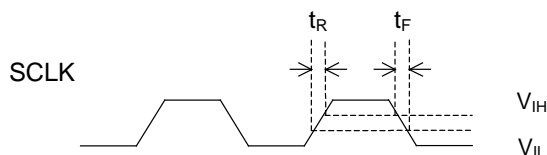
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSN setup time	t_{CSS}		100			ns
SDATA setup time	t_{DS}		100			ns
SDATA hold time	t_{DH}		100			ns
SCLK high time	t_{WH}		500			ns
SCLK low time	t_{WL}		500			ns
CSN low hold time	t_{CSLH}		100			ns
CSN high hold time	t_{CSHH}		100			ns
DAC output setting time	t_{LDD}	VOUT[7:0]= 0x10↔0xEF Until output reaches the half LSB of the final value. RS=2.2kΩ, L=22kΩ, CL=1000pF			300	μs
SCLK rising time	t_R				100	ns
SCLK falling time	t_F				100	ns

Note   Digital input timing measurements are made at 0.5DVDD for rising and falling edges.

4

Register Functions

1) Register configuration

Address				Function	Data							
A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	VOUT0 register	VOUT07	VOUT06	VOUT05	VOUT04	VOUT03	VOUT02	VOUT01	VOUT00
0	0	0	1	VOUT1 register	VOUT17	VOUT16	VOUT15	VOUT14	VOUT13	VOUT12	VOUT11	VOUT10
0	0	1	0	VOUT2 register	VOUT27	VOUT26	VOUT25	VOUT24	VOUT23	VOUT22	VOUT21	VOUT20
0	0	1	1	VOUT3 register	VOUT37	VOUT36	VOUT35	VOUT34	VOUT33	VOUT32	VOUT31	VOUT30
0	1	0	0	VOUT4 register	VOUT47	VOUT46	VOUT45	VOUT44	VOUT43	VOUT42	VOUT41	VOUT40
0	1	0	1	VOUT5 register	VOUT57	VOUT56	VOUT55	VOUT54	VOUT53	VOUT52	VOUT51	VOUT50
0	1	1	0	VOUT6 register	VOUT67	VOUT66	VOUT65	VOUT64	VOUT63	VOUT62	VOUT61	VOUT60
0	1	1	1	VOUT7 register	VOUT77	VOUT76	VOUT75	VOUT74	VOUT73	VOUT72	VOUT71	VOUT70
1	0	0	0	VREF register 0	DA3REF1	DA3REF0	DA2REF1	DA2REF0	DA1REF1	DA1REF0	DA0REF1	DA0REF0
1	0	0	1	VREF register 1	DA7REF1	DA7REF0	DA6REF1	DA6REF0	DA5REF1	DA5REF0	DA4REF1	DA4REF0
1	0	1	0	AVDD/2 register	AVDD2O7	AVDD2O6	AVDD2O5	AVDD2O4	AVDD2O3	AVDD2O2	AVDD2O1	AVDD2O0
1	0	1	1	BUFON register	BUFON7	BUFON6	BUFON5	BUFON4	BUFON3	BUFON2	BUFON1	BUFON0
1	1	0	0	Software reset	SRST[7:0]							
1	1	0	1	Not used	–	–	–	–	–	–	–	–
1	1	1	0	Not used	–	–	–	–	–	–	–	–
1	1	1	1	Not used	–	–	–	–	–	–	–	–

Note   An access to data indicated by "-" does not have any effect on the LSI operation.

2) Descriptions of registers
2.1) VOUT register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	VOUT07	VOUT06	VOUT05	VOUT04	VOUT03	VOUT02	VOUT01	VOUT00
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	VOUT77	VOUT76	VOUT75	VOUT74	VOUT73	VOUT72	VOUT71	VOUT70
Initial value				0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0	VOUT0 to VOUT7 output
0	0	0	0	0	0	0	0	VOUT = (VIN - VREF) • 0/256 + VREF
0	0	0	0	0	0	0	1	VOUT = (VIN - VREF) • 1/256 + VREF
0	0	0	0	0	0	1	0	VOUT = (VIN - VREF) • 2/256 + VREF
0	0	0	0	0	0	1	1	VOUT = (VIN - VREF) • 3/256 + VREF
↓	↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	0	VOUT = (VIN - VREF) • 254/256 + VREF
1	1	1	1	1	1	1	1	VOUT = (VIN - VREF) • 255/256 + VREF

2.2) VREF registers 0 and 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	DA3REF1	DA3REF0	DA2REF1	DA2REF0	DA1REF1	DA1REF0	DA0REF1	DA0REF0
1	0	0	1	DA7REF1	DA7REF0	DA6REF1	DA6REF0	DA5REF1	DA5REF0	DA4REF1	DA4REF0
Initial value				0	0	0	0	0	0	0	0

DA7REF1 to DA0REF1	DA7REF0 to DA0REF0	DAC reference voltage	Remarks
0	0	VSS (internal)	
0	1	AVDD (internal)	
1	0	AVDD/2 (internal)	
1	1	VREF (external)	

2.3) AVDD/2 register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	AVDD2O7	AVDD2O6	AVDD2O5	AVDD2O4	AVDD2O3	AVDD2O2	AVDD2O1	AVDD2O0
Initial value				0	0	0	0	0	0	0	0

Data	Item	Function		Remarks
		0	1	
AVDD2O7 to AVDD2O0	Internal AVDD/2 output	DAC output	Bypasses the DAC and outputs the AVDD/2 level through buffer.	

Note   Internal generated AVDD/2 level can be output to VOUT0 to VOUT7 pins by setting this register.

2.4) BUFON register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	BUFON7	BUFON6	BUFON5	BUFON4	BUFON3	BUFON2	BUFON1	BUFON0
Initial value				0	0	0	0	0	0	0	0

Data	Item	Function		Remarks
		0	1	
BUFON7 to BUFON0	DAC buffer operation	Powers down buffer and outputs Hi-Z.	Buffer output	

2.5) Software reset register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	SRST[7:0]							
Initial value				0	0	0	0	0	0	0	0

When the SRST[7:0] register is set to 0xAA (10101010), a software reset is performed.
This setting initializes all registers.
Upon completion of a software reset, the register is set to 0.

Recommended External Circuit Examples

1) Power supply stabilizing capacitors
   Connect capacitors between the VDD and VSS pins to eliminate ripple and noise included in the power supply as shown below.   For maximum effect, the capacitors should be placed at a shortest distance between the pins.

AVDD

DVDD
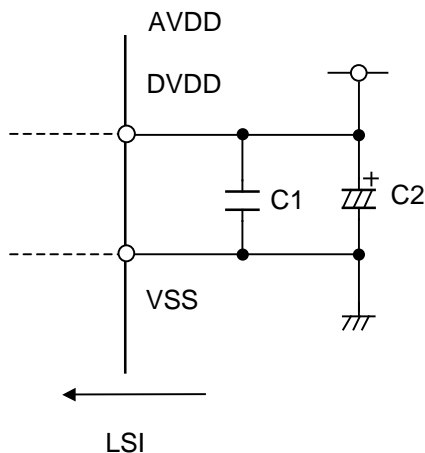
$C1 = 0.1\mu F$ (Ceramic cap)

C1   C2

$C2 = 4.7\mu F$ (Electrolytic cap)

VSS

LSI

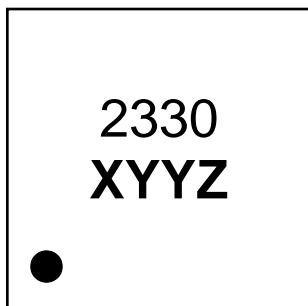2) External VIN0 to VIN7 capacitor
   When inputting an analog signal to the VIN pin, connect a capacitor to adjust the DC offset of the input signal and the internal operation point in the LSI device.   This forms a high-pass filter with fc being about 130Hz.

VIN0 to VIN7

C $C = 0.01\mu F$

LSI

AKM

Package

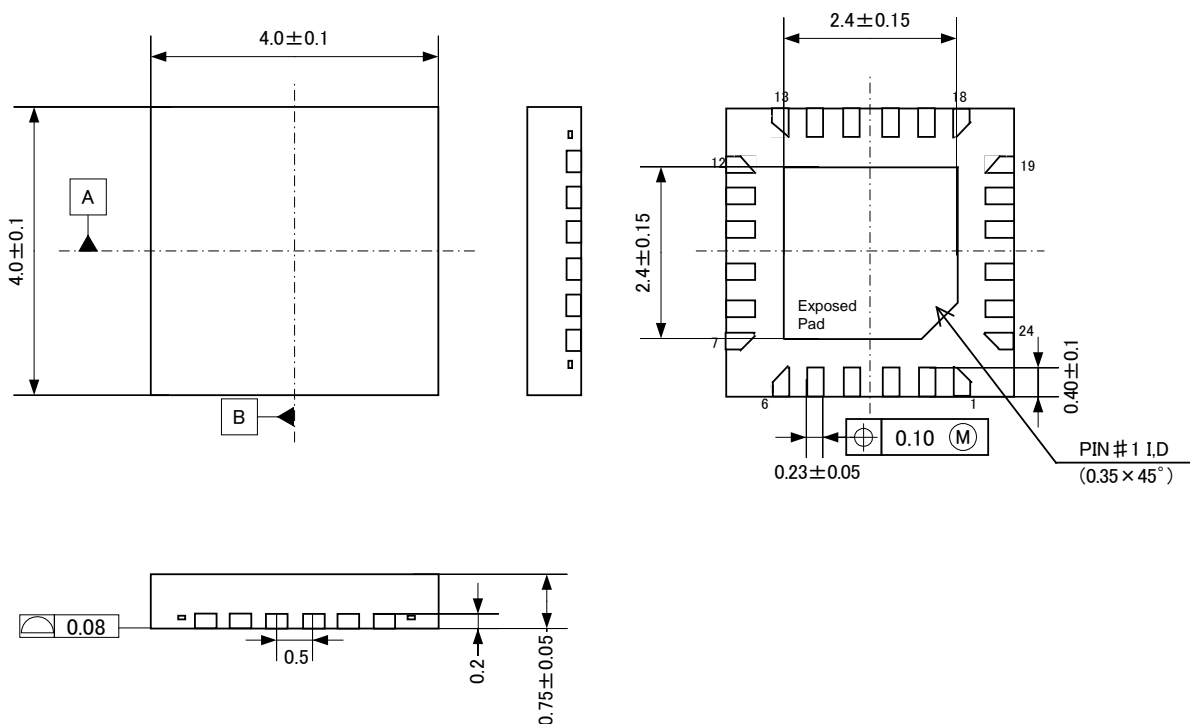1) Marking

2330
XYYZ

●
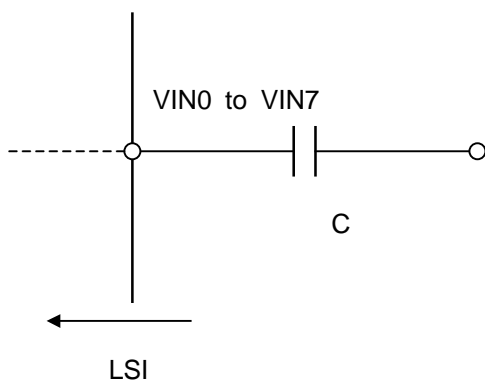
Part number   2330
Date code   X: Least significant digit of the year of production
                  Y: Week of production
                  Z: Identification code of production lot

2) External dimensions
   Package type: 24-pin QFNJ   (4.0mm x 4.0mm x 0.75mm, 0.5-mm pitch)

4.0±0.1

4.0±0.1

A

B

2.4±0.15

2.4±0.15

Exposed
Pad

18

18

12

19

7

24

6

1

0.40±0.1

⊕ 0.10 Ⓜ

0.23±0.05

PIN♯1 I,D
(0.35×45°)

⌒ 0.08

0.5

0.2

0.75±0.05

Note   The exposed pad at the center of the back of the package must be connected to VSS or
        opened.

AKM

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