

N-Channel Power MOSFET

650V, 7A, 1.45Ω

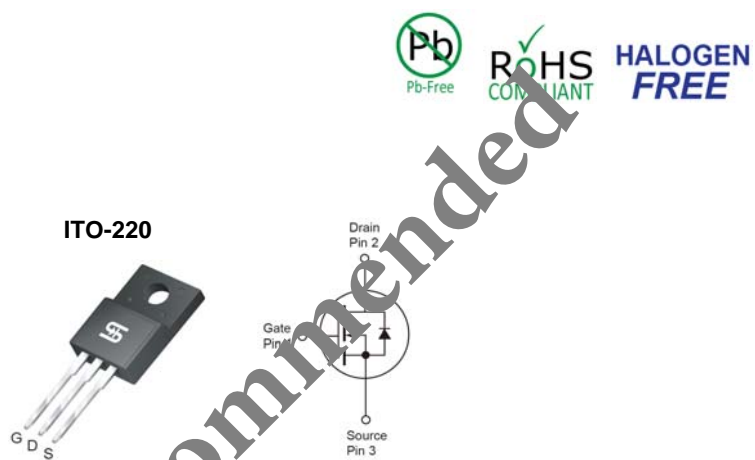
FEATURES

- Low C_{rss} typical @ 15pF (Typ.)
- 100% Avalanche Tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	650	V
$R_{DS(on)}$ (max)	1.45	Ω
Q_g	27.8	nC



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	7
		$T_C = 100^\circ\text{C}$	4.2
Pulsed Drain Current (Note 2)	I_{DM}	28	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	40	W
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	150	mJ
Single Pulsed Avalanche Current (Note 3)	I_{AS}	5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	Limit	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	3.1	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	65	°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	650	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.0	3.0	4.0	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 3.0A	R _{DS(on)}	--	1.2	1.45	Ω
Dynamic (Note 5)						
Total Gate Charge	V _{DS} = 480V, I _D = 6.0A, V _{GS} = 10V	Q _g	--	27.8	--	nC
Gate-Source Charge		Q _{gs}	--	5.7	--	
Gate-Drain Charge		Q _{gd}	--	8.8	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	1406	--	pF
Output Capacitance		C _{oss}	--	114	--	
Reverse Transfer Capacitance		C _{rss}	--	15	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	1.5	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V _{DD} = 300V, R _{GEN} = 25Ω, I _D = 6.0A, V _{GS} = 10V,	t _{d(on)}	--	25	--	ns
Turn-On Rise Time		t _r	--	57	--	
Turn-Off Delay Time		t _{d(off)}	--	83	--	
Turn-Off Fall Time		t _f	--	61	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	I _S = 3.0A, V _{GS} = 0V	V _{SD}	--	--	1.5	V
Reverse Recovery Time	I _S = 1A	t _{rr}	--	213	--	ns
Reverse Recovery Charge	di _F /dt = 100A/μs	Q _{rr}	--	2480	--	nC
Source Current	Integral reverse diode in the MOSFET	I _S	--	--	7	A
Source Current (Pulse)		I _{SM}	--	--	28	A

Notes:

- Current limited by package
- Pulse width limited by the maximum junction temperature
- L = 12mH, I_{AS} = 5.0A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
100% Eas Test Condition: L = 12mH, I_{AS} = 2.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
- Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

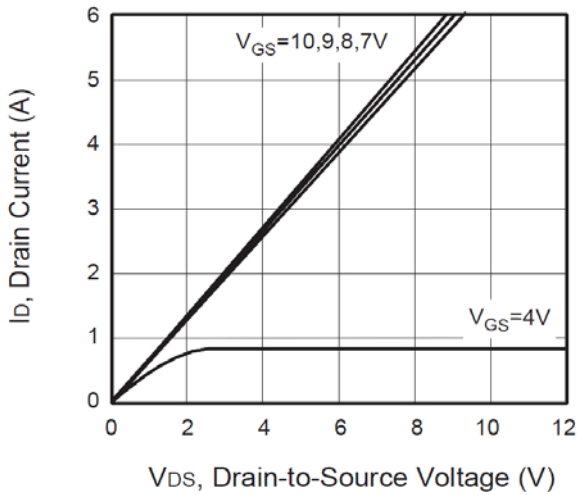
PART NO.	PACKAGE	PACKING
TSM7N65ACI C0G	ITO-220	50pcs / Tube

Not Recommended

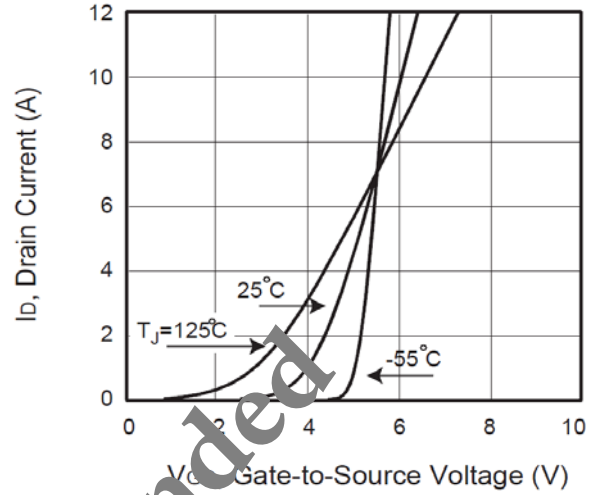
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

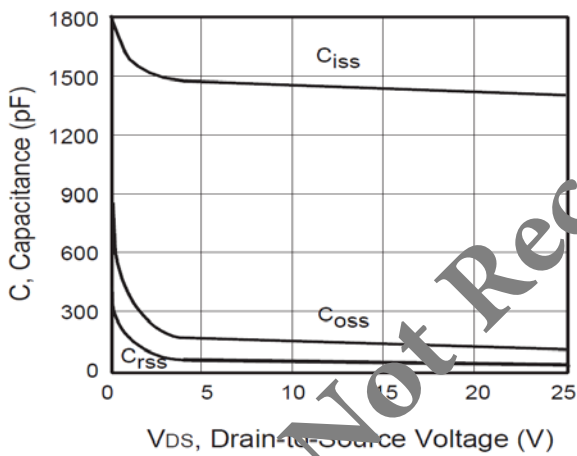
Output Characteristics



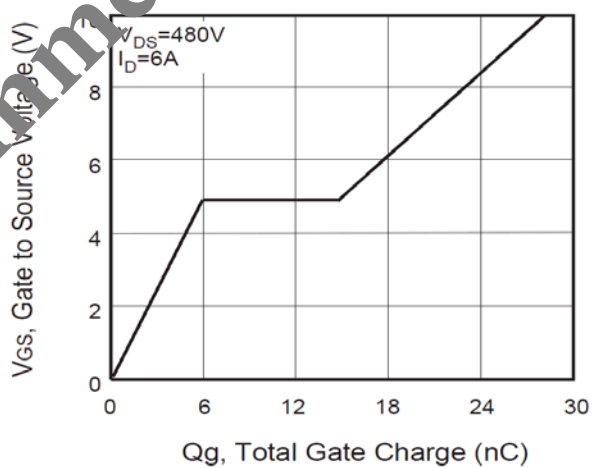
Transfer Characteristics



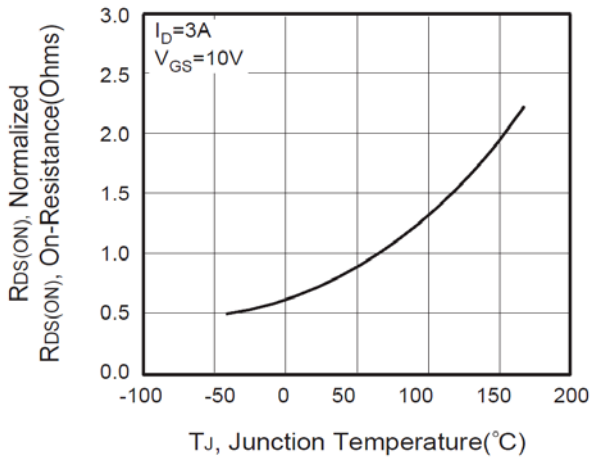
Capacitance



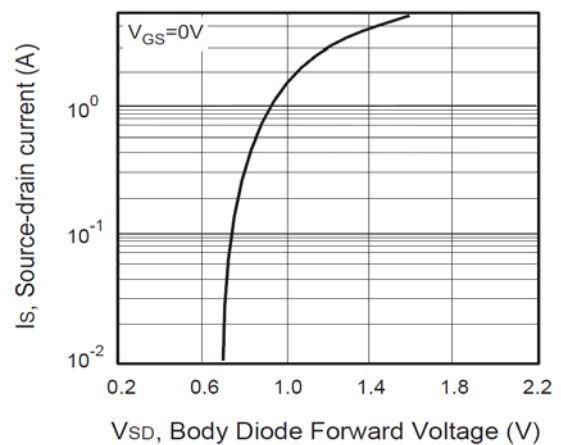
Gate Charge



On-Resistance vs. Junction Temperature



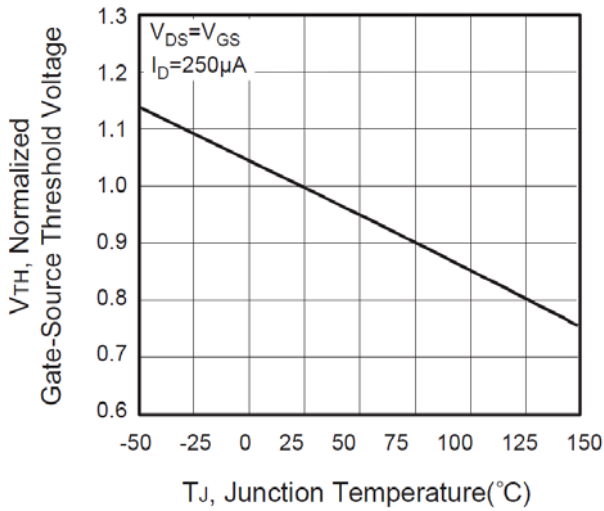
Source-Drain Diode Forward Voltage



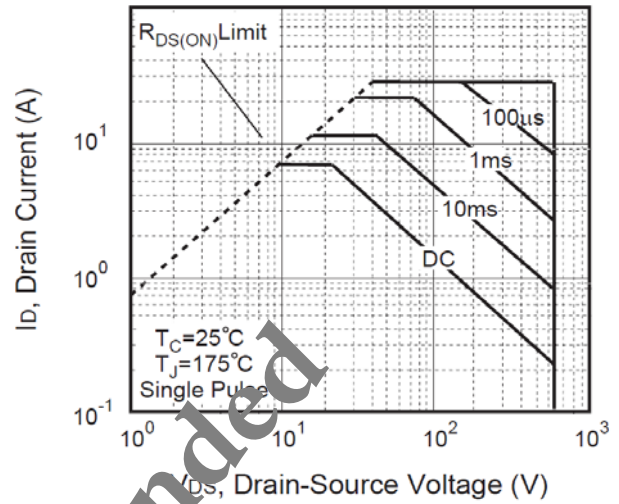
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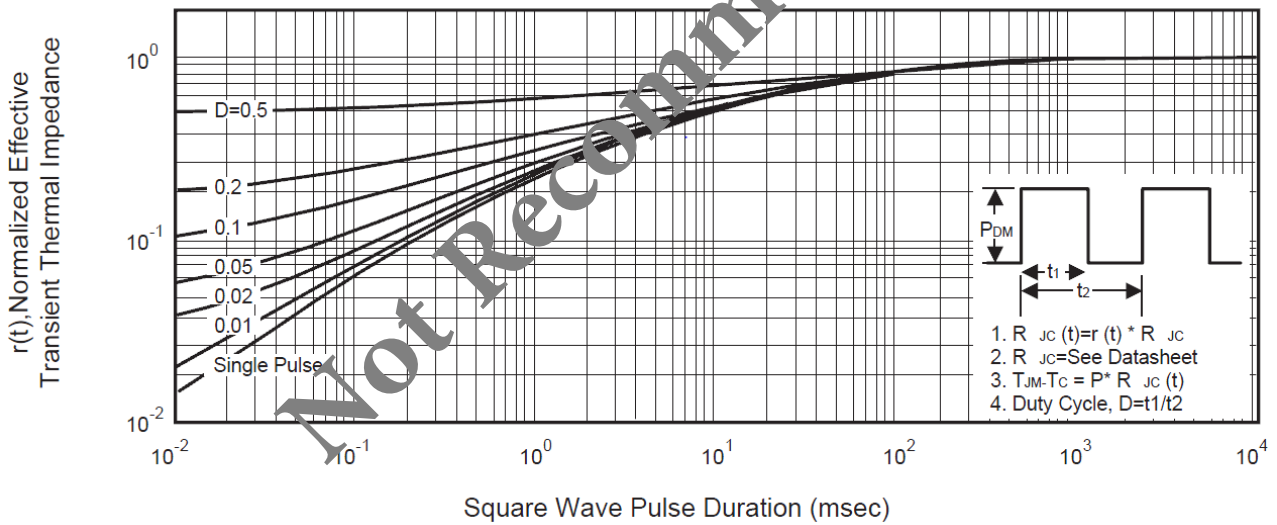
Threshold Voltage vs. Junction Temperature



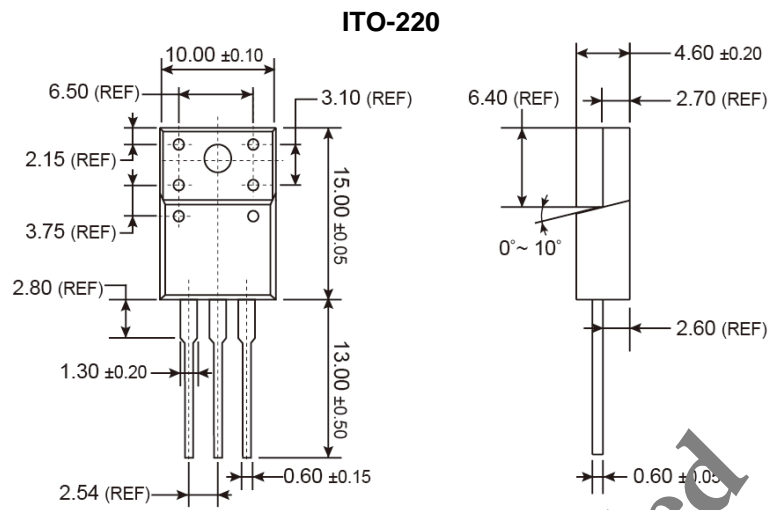
Maximum Safe Operating Area



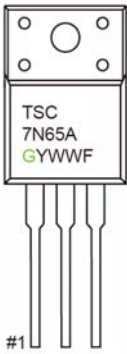
Normalized Thermal Transient Impedance Curve



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

Not Recommended

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