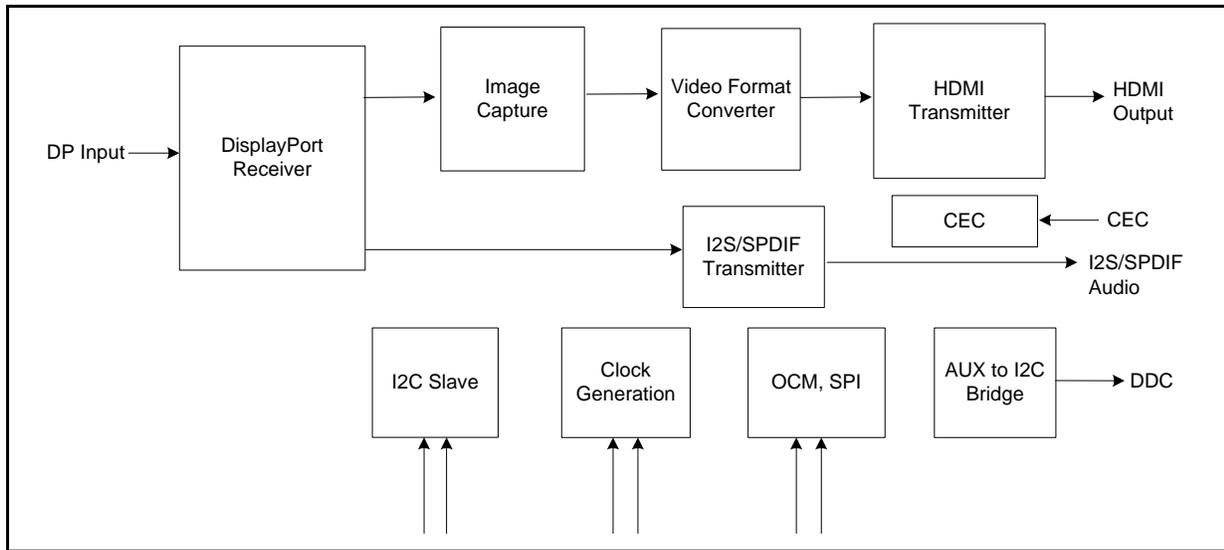# Features

- DisplayPort® (DP) receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - Supports eDP operation
- HDMI 1.4 transmitter
  - Max data rate up to 2.97 Gbps/data pair
  - Color depth up to 48 bits
  - 3D video timings
  - CEC
- SPDIF audio output
  - 192 kHz/24 bits
  - Compressed/LPCM
- HDCP repeater with embedded keys
- ASSR -- eDP display authentication option
- AUX to I2C bridge for EDID/MCCS pass through
- Device configuration options
  - SPI Flash
  - I2C host interface
- Spread spectrum on DisplayPort interface for EMI reduction
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
  - Color space conversion – YUV to RGB and RGB to YUV
- Bandwidth
  - Video resolution up to 4K x 2K @ 30 Hz; 1920 x 1080 @ 120 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation; active 462 mW, standby 21 mW
- Package
  - 81 BGA (8 x 8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- DisplayPort to HDMI bridge for TVs and projectors
- Audio-video accessory (dongle) for desktop, notebook computers, and tablets

```
DP Input ──▶ DisplayPort          Image          Video Format          HDMI          HDMI
             Receiver            Capture           Converter         Transmitter     Output

                                                              I2S/SPDIF       CEC ◀── CEC
                                                              Transmitter          ──▶ I2S/SPDIF
                                                                                       Audio

             I2C Slave           Clock            OCM, SPI          AUX to I2C ──▶ DDC
                                Generation                           Bridge
```

1.   Description

The STDP2650 is a high-speed DisplayPort to HDMI converter IC for applications such as audio-video accessories for docking stations, TV front-end design, etc. This device includes a VESA DP Standard Ver.1.2a compliant receiver and an HDMI 1.4 compliant transmitter. The DisplayPort input port comprises four Main lanes, AUX CH, and HPD signal. The HDMI output port includes DDC, CEC, and HPD support.

The STDP2650 uses MegaChips latest generation DisplayPort receiver technology that supports HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. The HDMI transmitter is capable of supporting link rate up to 2.97 Gbps that corresponds to a pixel rate of 297 MHz, adequate for handling video resolution up to FHD 120 Hz 3D formats. This device delivers deep color video up to 16-bits per color at 1080p 60 Hz and lower video resolutions. The STDP2650 allows audio transport from the source to desired audio rendering devices over the HDMI output or through the SPDIF port. The audio signal from the source can be routed simultaneously to HDMI and SPDIF output ports. For example, the STDP2650 allows routing of any two audio channels on the SPDIF port, while transporting up to eight channels on the HDMI port.

The STDP2650 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. This device features HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content. It also operates as an HDCP repeater for the downstream sink. The eDP authentication option ASSR (Alternative Scrambler Seed Reset) is supported for embedded application.

The AUX-to-I2C translator in the STDP2650 allows the upstream DisplayPort source to access EDID and transfer MCCS commands to a downstream sink over the HDMI interface. This device has an on-chip microcontroller with SPI and I2C host interface for system configuration purposes. The STDP2650 can be configured with an external SPI Flash for custom applications. In addition, it allows register level configuration from an external host controller through I2C interface.

2. Application overview
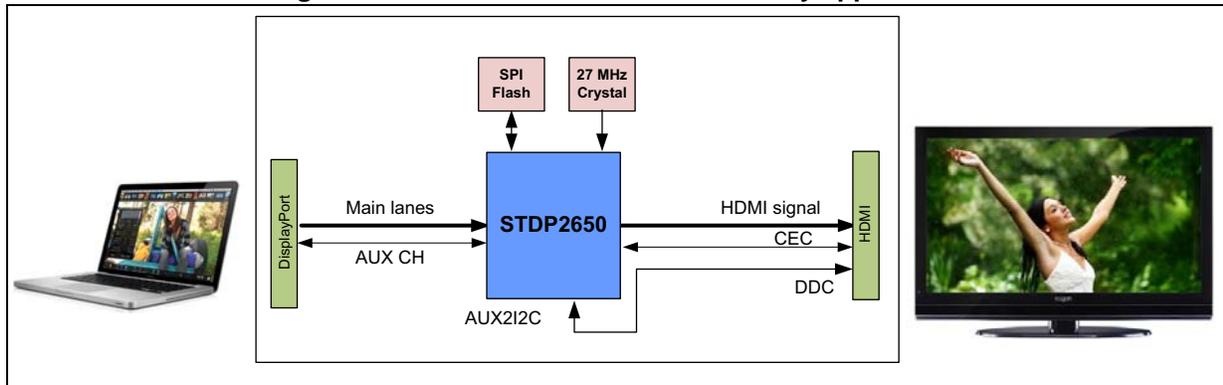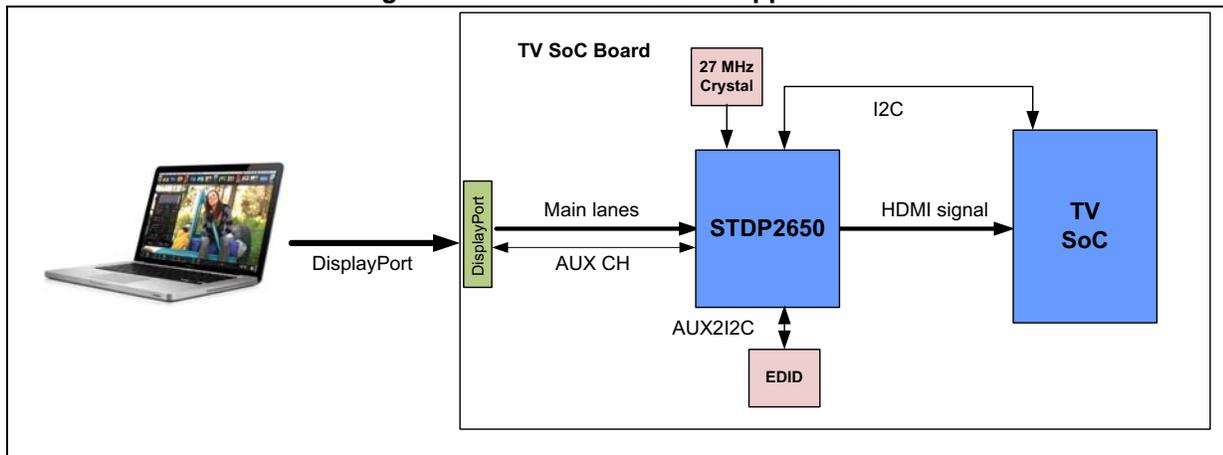
Figure 1. STDP2650 in notebook accessory application

Figure 2. STDP2650 inside TV application

3. Feature attributes

3.1 Input interface

- DP standard Ver. 1.2a compliant
- Main link configuration (SST format only, no MST format support)
    - HBR2/HBR/RBR link rate
    - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB or YCC422 or YcC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates

3.2 Output interface

- HDMI standard Ver. 1.4 compliant
- Link rate: 2.97 Gbps/data pair max
- Video: HDMI 1.4 primary and secondary timing formats, as well as CEA861 timing formats with pixel repetition for lower resolutions
- Deep color encoding up to 48 bits/pixel in 444 and 422; encoding in 601, 709, and IEC61966 color spaces
- Audio: IEC60958 L-PCM and IEC61937 streams up to 24 bits/sample from 32 kHz to 192 kHz
- DDC master port
- HPD monitoring
- HDMI RX 3.3 V termination monitoring

3.3 Deep color support

- RGB/YCC (4:4:4) – 16-bit color
- YCC (4:2:2) – 16-bit color
- Color space conversion – YUV to RGB and RGB to YUV

3.4   Supported video timings

• 4096 x 2160 (4K x 2K) 24 Hz/30 Hz: 24 bits/pixel

• 1920 x 1080 (FHD) 120 Hz: 24 bits/pixel

• 2560 x 1600 (WQXGA) 60 Hz: 24 bits/pixel

• Up to 1920 x 1080 (FHD) 60 Hz, 48, 36, 30 bits/pixel

• All compatible 3D formats defined in DP 1.2a and HDMI 1.4 specifications

• All standard CEA861 timing formats

3.5   Supported audio timings

• All audio formats as specified in DP 1.2a and HDMI 1.4 specifications

• SPDIF: 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz

3.6   Control channel interfaces

• AUX CH, I2C host interface, SPI (optional), and UART (UART for test/debug purposes only)

3.7   HDCP 1.3 support

• Key sets for DPRX and HDMI TX integrated in one-time programmable ROM (OTP)

• Standalone HDCP repeater capability

• Supports eDP display authentication option ASSR (Alternate Scrambler Seed Reset)

3.8   Package

• 81 BGA (8 x 8 mm), 0.8 ball pitch

3.9   Power supply voltages

• 3.3 V I/O; 1.2 V core

3.10   ESD

• 2 KV HBM, 500 V CDM

4.   Ordering information

Table 1. Order codes

Part number	Description
STDP2650-AD	81 BGA (8 x 8 mm) delivered in trays
STDP2650-ADT	81 BGA (8 x 8 mm) delivered in tape and reel

5. Revision history

Table 2. Document revision history

Date	Revision	Changes
05-Jun-2012	1	Initial release.
07-May-2013	2	Changed DP1.2 to DP1.2a throughout. Added eDP and ASSR feature in first page, Features, Description, and Feature attributes sections. Cover page: updated low power operation data. Ordering information section: Updated silicon revision in the table.
22-May-2014	3	Updated to comply with MegaChips documentation style/formatting.
15-Sep-2014	4	Updated footers and added copyright information to last page.

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