

### FEATURES

- 100MHz to 200MHz Fundamental or 3<sup>rd</sup> Overtone Crystal input.
- Output range: 100 – 200MHz (no multiplication), 200 – 400MHz (2x multiplier) or 400 – 700MHz (4x multiplier).
- Available outputs: PECL, LVDS, or CMOS (High Drive (30mA) or Standard Drive (10mA) output).
- Supports 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

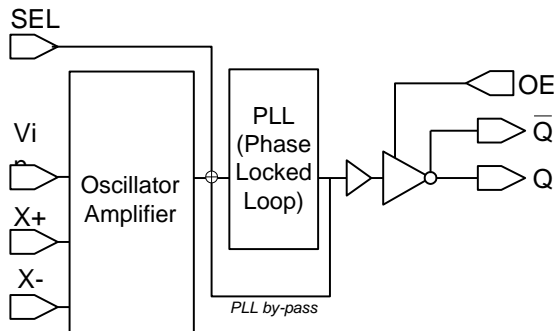
### DESCRIPTION

The PL620-00 is an XO IC specifically designed to work with high frequency fundamental and third overtone crystals. Its design was optimized to tolerate higher limits of interelectrode capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. It is ideal for XO applications requiring LVDS or PECL output levels at high frequencies.

### DIE SPECIFICATIONS

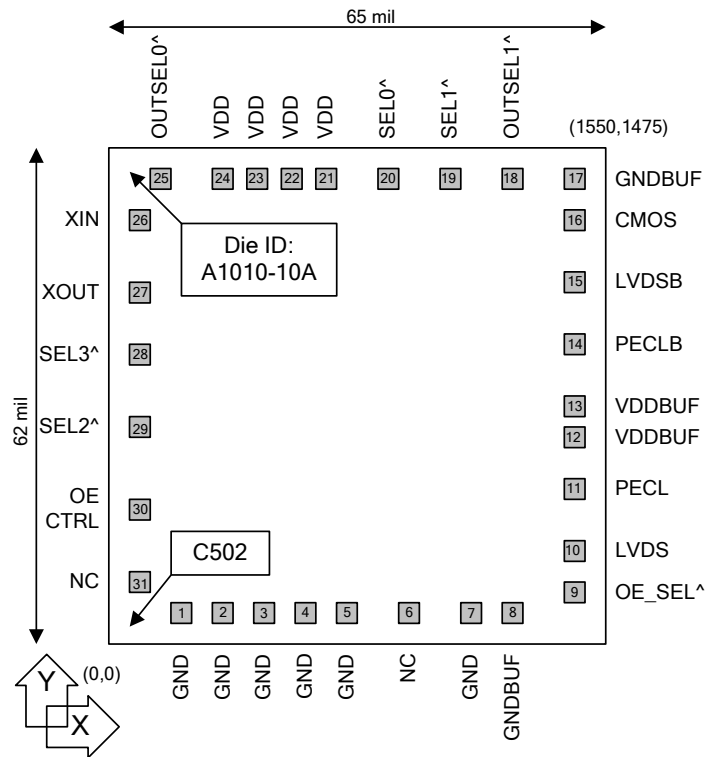
Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

### BLOCK DIAGRAM



PL620-00

### DIE CONFIGURATION



### OUTPUT SELECTION AND ENABLE

OUTSEL1 (Pad #18)	OUTSEL0 (Pad #25)	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	LVDS
1	1	PECL (default)

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"  
 Pad #30: Logical states defined by PECL levels if OE\_SELECT (pad #9) is "1"  
 Logical states defined by CMOS levels if OE\_SELECT is "0"

**Low Phase Noise XO with multipliers (for HF Fund. and 3<sup>rd</sup> O.T.)  
FREQUENCY SELECTION TABLE**

SEL3 (Pad #28)	SEL2 (Pad #29)	SEL1 (Pad #19)	SEL0 (Pad #20)	Selected Multiplier
1	0	1	1	Fin x 4
1	1	1	0	Fin x 2
1	1	1	1	No multiplication (no PLL)

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Fundamental or 3 <sup>rd</sup> overtone*	100		200	MHz
Crystal Loading Rating	$C_L$ (xtal)	Die only		3.0		pF
Interelectrode Capacitance	$C_0$				3	pF
Recommended ESR	$R_E$	$F_{XIN} < 160\text{MHz}$ and $C_0 < 3.0\text{pF}$			30	$\Omega$
		$F_{XIN} < 200\text{MHz}$ and $C_0 < 3.0\text{pF}$			25	$\Omega$
		$F_{XIN} < 200\text{MHz}$ and $C_0 < 2.5\text{pF}$			30	$\Omega$

\* Note: 3<sup>rd</sup> overtone crystals require an external resistor between XIN and XOUT to prevent the fundamental from oscillating.

### 3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	$I_{DD}$	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	$V_{DD}$		2.97		3.63	V
Output Clock Duty Cycle		@ 50% $V_{DD}$ (CMOS)	45	50	55	%
		@ 1.25V (LVDS)	45	50	55	
		@ $V_{DD} - 1.3\text{V}$ (PECL)	45	50	55	
Short Circuit Current				±50		mA

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**4. Jitter Specifications**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period jitter peak-to-peak			18.5	20	
Accumulated jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3	0.4	ps
Period jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		11		ps
Period jitter peak-to-peak			45	49	
Accumulated jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		11		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		3		ps
Integrated jitter RMS at 622MHz	Integrated 12 kHz to 20 MHz		1.6	1.8	ps

Note: Higher Q factor of 3<sup>rd</sup> overtone crystals will result in even better jitter performance.  
Measured on Wavecrest SIA 3000

**5. Phase Noise Specifications**

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz
	622.08MHz	-75	-95	-110	-125	-120	

Note: Higher Q factor of 3<sup>rd</sup> overtone crystals will result in even better phase noise performance.

**6. CMOS Electrical Specifications**

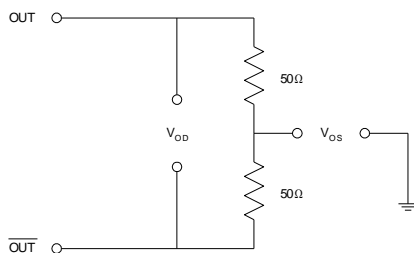
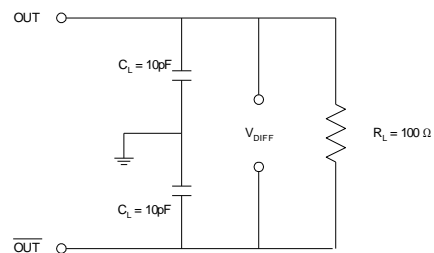
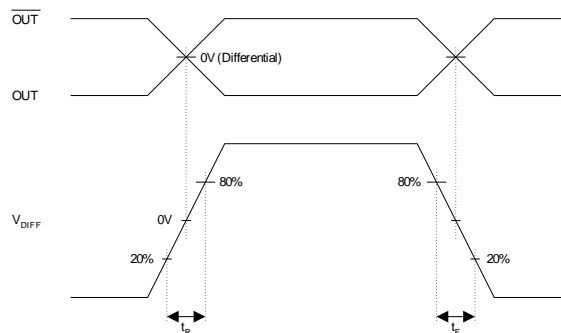
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	30			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	30			mA
Output drive current (Standard Drive)	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	10			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

**Low Phase Noise XO with multipliers (for HF Fund. and 3<sup>rd</sup> O.T.)**
**7. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$		1.4	1.6	V	
Output Low Voltage	$V_{OL}$		0.9	1.1	V	
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

**8. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

LVDS Levels Test Circuit

LVDS Switching Test Circuit

LVDS Transistion Time Waveform


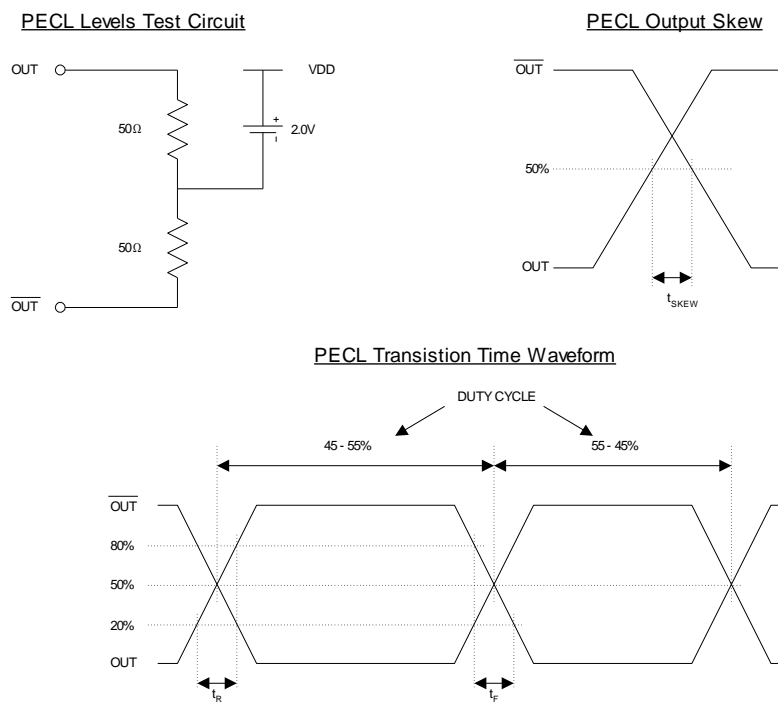
## Low Phase Noise XO with multipliers (for HF Fund. and 3<sup>rd</sup> O.T.)

### 9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

### 10. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	$t_f$	@80/20% - PECL		0.5	1.5	ns



**Low Phase Noise XO with multipliers (for HF Fund. and 3<sup>rd</sup> O.T.)**
**PAD ASSIGNMENT**

Pad #	Name	X (μm)	Y (μm)	Description
1	GND	248	109	Ground.
2	GND	361	109	Ground.
3	GND	473	109	Ground.
4	GND	587	109	Ground.
5	GND	702	109	Ground.
6	N/C	874	109	No Connection.
7	GND	1042	109	Ground.
8	GNDBUF	1171	109	Ground, Buffer circuitry.
9	OE_SELECT	1400	125	Used to select between PECL or CMOS logic states for OE. See Output Selection and Enable table on page 1. Internal pull up.
10	LVDS	1400	259	LVDS output.
11	PECL	1400	476	PECL output.
12	VDDBUF	1400	616	3.3V power supply, Buffer circuitry.
13	VDDBUF	1400	716	3.3V power supply, Buffer circuitry.
14	PECLB	1400	871	Complementary PECL output.
15	LVDSB	1400	1089	Complementary LVDS output.
16	CMOS	1400	1227	CMOS output
17	GNDBUF	1389	1365	Ground, Buffer Circuitry.
18	OUTSEL1	1232	1365	Used to select CMOS, PECL or LVDS output type. See Output Selection and Enable table on page 1. Internal pull up.
19	SEL1	1042	1365	Used to select multiplication factor. See Frequency Selection table on page 1. Internal pull up.
20	SEL0	854	1365	Used to select multiplication factor. See Frequency Selection table on page 1. Internal pull up.
21	VDD	659	1365	3.3V power supply.
22	VDD	559	1365	3.3V power supply.
23	VDD	459	1365	3.3V power supply.
24	VDD	358	1365	3.3V power supply.
25	OUTSEL0	194	1365	Used to select CMOS, PECL or LVDS output type. See Output Selection and Enable table on page 1. Internal pull up.
26	XIN	109	1223	Crystal input. See crystal specification page 2.
27	XOUT	109	1017	Crystal output. See crystal specification page 2.
28	SEL3	109	858	Used to select multiplication factor. See Frequency Selection table on page 1. Internal pull up.
29	SEL2	109	646	Used to select multiplication factor. See Frequency Selection table on page 1. Internal pull up.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Enable table on page 1.
31	NC	109	181	No Connection.

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**ORDERING INFORMATION**

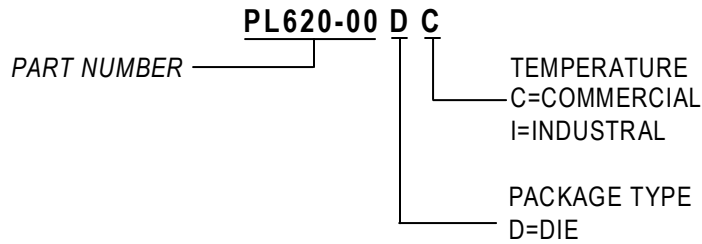
**For part ordering, please contact our Sales Department:**

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PL620-00DC	P620-00DC	Die – Waffle Pack

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