PIC16(L)F184XX Memory Programming Specification

Overview

The PIC16(L)F184XX Memory Programming Specification describes the programming method for the PIC16(L)F184XX family of 8-bit microcontrollers. The programming specification describes the programming commands, programming algorithms, and electrical specifications which are used in that particular programming method. *"Appendix B"* contains individual part numbers, device identification and checksum values, pinout and packaging information, and Configuration Words.

Note: To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

Related Links

Appendix B: Device ID, Checksums and Pinout Descriptions

Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming™ (ICSP™) interface. Data can be programmed into the Program Flash Memory, EEPROM, dedicated "User ID" locations, and the Configuration Words.

Write and/or Erase Selection

Erasing or writing is selected according to the command used to begin operation (see the *"Program/Verify Commands"* section for more details). The terminologies used in this document related to erasing/writing to the Program Flash Memory are defined in the table below.

Table 1. Programming Terms

Term	Definition
Programmed Cell	A memory cell with a logic '0'
Erased Cell	A memory cell with a logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

Related Links

Program/Verify Commands

1 Erasing Memory

Program Flash Memory is erased by row or in bulk, where ‘bulk’ includes many subsets of the total memory space. The duration of the erase is always determined internally. Here, ‘row’ refers to the minimum erasable size and ‘bulk’ is one of the many possible subsets of all memory rows. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Row Erase and write requirements.

Related Links

Electrical Specifications

2 Writing Memory

Program Flash Memory is written one row at a time, while EEPROM is written one byte at a time. Multiple load data for NVM commands are used to fill the Program Flash Memory’s row data latches. The duration of the write is determined either internally or externally.

Related Links

Electrical Specifications

3 Multi-Word Programming Interface

Program Flash Memory panels include a 32-word (one row) programming interface. The row to be programmed must first be erased either with a Bulk Erase or a Row Erase.

Related Links

Electrical Specifications

Hardware Requirements

1 High-Voltage ICSP Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

2 Low-Voltage ICSP Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

2.1 Single-Supply ICSP Programming

The LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a ‘1’ (enabled) from the factory. The LVP bit may only be programmed to ‘0’ by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a ‘0’, only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note:

1. The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
2. While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in the table below.

Table 1. Pin Descriptions during Programming

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ICSPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ICSPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}/V_{PP}$	Program/Verify mode	I(1)	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground
Legend: I = Input, O = Output, P = Power			

Note:

1. The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

Related Links

Programming Pin Locations by Package Type

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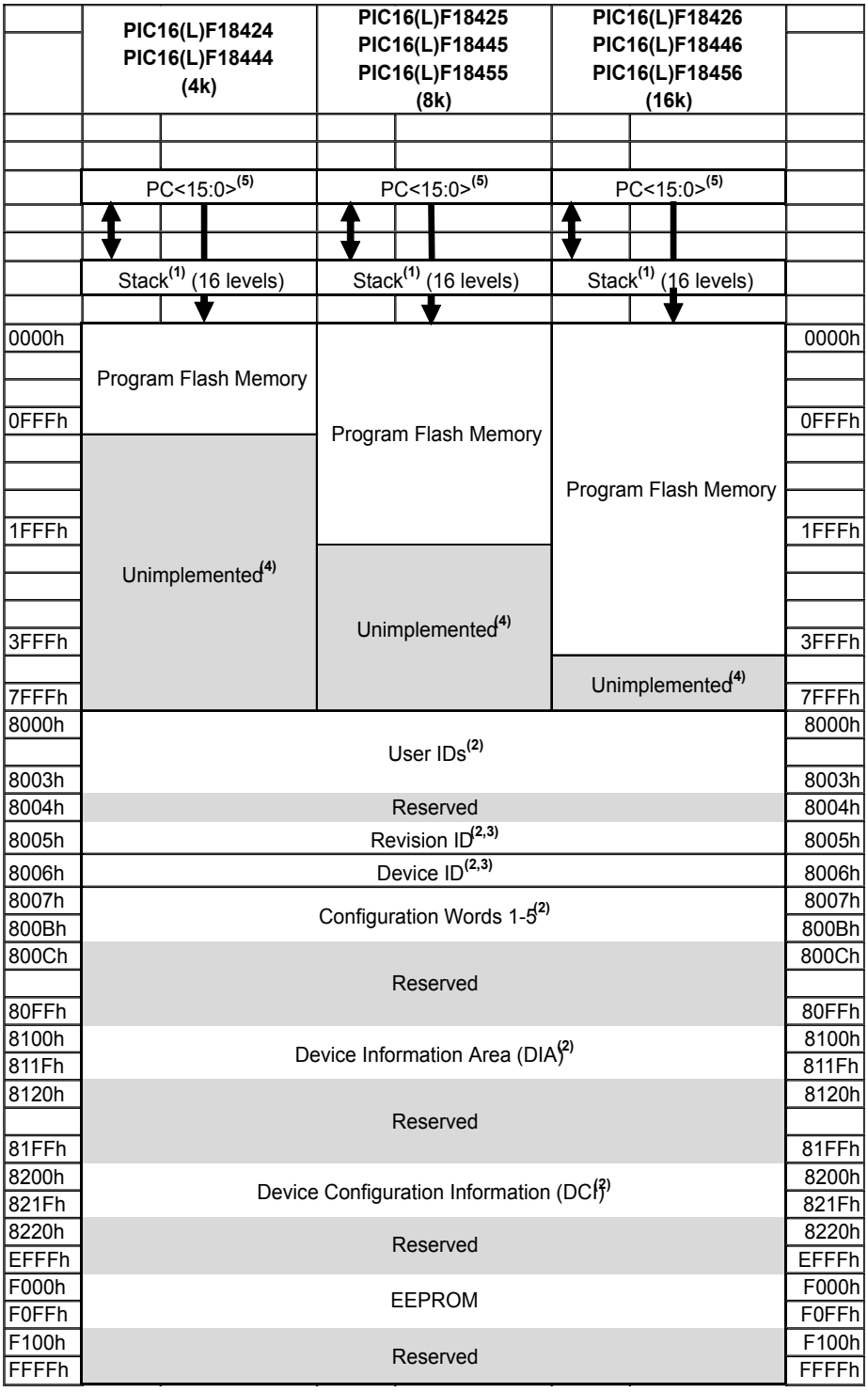
1. Memory Map

1.1 Program Memory Mapping



Note:

1. The stack is a separate SRAM panel, apart from all user memory panels.
2. Not code-protected.
3. Device Configuration Information, Device/Revision IDs are hard-coded in silicon.
4. The addresses do not roll over. The region is read as '0'.
5. For the purposes of instruction fetching during program execution, only 15 bits (PC<14:0>) are used. However, for the purposes of nonvolatile memory reading and writing through ICSP™ programming operations, the PC uses all16 bits (PC<15:0>), and the "Load PC Address" command requires a full 16-bit data payload.

1.2 User ID Location

A user may store identification information (User ID) in four designated locations. The User ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

1.3 Device/Revision ID

The 14 bits Device ID word is located at 0x8006 and the 14 bits Revision ID is located at 0x8005. These locations are read-only and cannot be erased or modified.

1.3.1 Register Summary - Device and Revision

Offset	Name	Bit Pos.									
0x8005	REVISION ID	7:0	MJRREV[1:0]		MNRREV[5:0]						
		13:8			1	0	MJRREV[5:2]				
0x8006	DEVICE ID	7:0	DEV[7:0]								
		13:8			1	1	DEV[11:8]				

1.3.2 Register Definitions: Device and Revision

1.3.2.1 DEVICE ID

Name: DEVICE ID
Offset: 0x8006

Device ID Register

Bit	15	14	13	12	11	10	9	8
			1	1	DEV[11:8]			
Access			R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit 13 – 1
These bit must be '1' to be distinguishable from the previous Device ID scheme

Bit 12 – 1
These bit must be '1' to be distinguishable from the previous Device ID scheme

Bits 11:0 – DEV[11:0]
Device ID bits

Device	Device ID
PIC16F18424	30CA
PIC16LF18424	30CB
PIC16F18425	30CC
PIC16LF18425	30CD
PIC16F18426	30D2
PIC16LF18426	30D3
PIC16F18444	30CE
PIC16LF18444	30CF
PIC16F18445	30D0
PIC16LF18445	30D1
PIC16F18446	30D4
PIC16LF18446	30D5
PIC16F18455	30D7
PIC16LF18455	30D8
PIC16F18456	30D9
PIC16LF18456	30DA

Related Links

Device IDs and Checksums

1.3.2.2 REVISION ID

Name: REVISION ID
Offset: 0x8005

Revision ID Register

Bit	15	14	13	12	11	10	9	8
			1	0	MJRREV[5:2]			
Access			R	R	R	R	R	R
Reset			1	0				

Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	R	R	R	R	R	R	R	R
Reset								

Bit 13 – 1 Read as '1'
These bits are fixed with value '1' for all devices in this family.

Bit 12 – 0 Read as '0'
These bits are fixed with value '0' for all devices in this family.

Bits 11:6 – MJRREV[5:0] Major Revision ID bits
These bits are used to identify a major revision.

Bits 5:0 – MNRREV[5:0] Minor Revision ID bits
These bits are used to identify a minor revision.

1.4 Configuration Words

The devices have five Configuration Words starting at address 8007h through 800Bh. The Configuration bits establish configuration values prior to the execution of any software; Configuration bits enable or disable device-specific features.

In terms of programming, these important Configuration bits should be considered:

1. **LVP: Low-Voltage Programming Enable Bit**
   - 1 = ON – Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
   - 0 = OFF – HV on $\overline{MCLR}/V_{PP}$ must be used for programming.
2. **$\overline{CP}$: User Nonvolatile Memory (NVM) Program Memory Code Protection bit**
   - 1 = OFF – User NVM code protection disabled
   - 0 = ON – User NVM code protection enabled

Related Links

Low-Voltage Programming (LVP) Mode
Code Protection

1.4.1 Register Summary - Configuration Words

Offset	Name	Bit Pos.								
0x8007	CONFIG1	7:0			RSTOSC[2:0]			FEXTOSC[2:0]		
		13:8			FCMEN		CSWEN			$\overline{\text{CLKOUTEN}}$
0x8008	CONFIG2	7:0	BOREN		$\overline{\text{LPBOREN}}$			PWRTS[1:0]		MCLRE
		13:8			$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	
0x8009	CONFIG3	7:0		WDTE[1:0]		WDTCPS[4:0]				
		13:8			WDTCCS[2:0]			WDTCWS[2:0]		
0x800A	CONFIG4	7:0	$\overline{\text{WRTAPP}}$			$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
		13:8			LVP		$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
0x800B	CONFIG5	7:0								$\overline{\text{CP}}$
		13:8								

1.4.2 Register Definitions: Configuration Words

1.4.2.1 CONFIG1

Name: CONFIG1
Offset: 0x8007

Configuration word 1

Oscillators

Bit	15	14	13	12	11	10	9	8
			FCMEN		CSWEN			$\overline{\text{CLKOUTEN}}$
Access			R/P	U	R/P	U	U	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access	U	R/P	R/P	R/P	U	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bit 13 – FCMEN Fail-Safe Clock Monitor Enable bit

Value	Description
1	FSCM timer enabled
0	FSCM timer disabled

Bit 11 – CSWEN Clock Switch Enable bit

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 8 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable bit

Value	Condition	Description
1	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is disabled; I/O or oscillator function on OSC2
0	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is enabled; F_{OSC}/4 clock appears at OSC2
	Otherwise	This bit is ignored.

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC bits
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC (1 MHz), with OSCFRQ = '010' (4 MHz) and CDIV = '0010' (4:1)
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits

Value	Description
001	HFINTOSC with 2x PLL (32 MHz), with OSCFRQ = '101' (16 MHz) and CDIV = '0000' (1:1)
000	Reserved

Bits 2:0 – FEXTOSC[2:0] FEXTOSC External Oscillator Mode Selection bits

Value	Description
111	ECH (External Clock) above 8 MHz
110	ECM (External Clock) for 100 kHz to 8 MHz
101	ECL (External Clock) below 100 kHz
100	Oscillator not enabled
011	Reserved (do not use)
010	HS (Crystal oscillator) above 4 MHz
001	XT (Crystal oscillator) above 100 kHz, below 4 MHz
000	LP (crystal oscillator) optimized for 32.768 kHz

1.4.2.2 CONFIG2

Name: CONFIG2
Offset: 0x8008

Configuration Word 2

Supervisor

Bit	15	14	13	12	11	10	9	8
			$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	
Access			R/P	R/P	R/P	R/P	R/P	U
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]		$\overline{\text{LPBOREN}}$			PWRTS[1:0]		MCLRE
Access	R/P	R/P	R/P	U	U	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bit 13 – $\overline{\text{DEBUG}}$ Debugger Enable bit(1)

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 12 – STVREN Stack Overflow/Underflow Reset Enable bit

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 11 – PPS1WAY PPSLOCKED bit One-Way Set Enable bit

Value	Description
1	The PPSLOCKED bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0	The PPSLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 10 – ZCDDIS ZCD Disable bit

Value	Description
1	ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of the ZCDCON register.
0	ZCD always enabled, ZCDSEN bit is ignored

Bit 9 – BORV Brown-out Reset Voltage Selection bit

Value	Description
1	Brown-out Reset voltage (V_{BOR}) set to lower trip point level
0	Brown-out Reset voltage (V_{BOR}) set to higher trip point level

Bits 7:6 – BOREN[1:0] Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by BORV bit

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – $\overline{\text{LPBOREN}}$ Low-Power BOR Enable bit

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection bits

Value	Description
11	PWRT disabled
10	PWRT set at 64 ms
01	PWRT set at 16 ms
00	PWRT set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable bit

Value	Condition	Description
	If LVP = 1	RE3 pin function is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is port defined function

Note:

1. The $\overline{\text{DEBUG}}$ bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

1.4.2.3 CONFIG3

Name: CONFIG3
Offset: 0x8009

Configuration Word 3

Windowed Watchdog Timer

Bit	15	14	13	12	11	10	9	8
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/P	R/P	R/P	R/P	R/P	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access	U	R/P	R/P	R/P	R/P	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bits 13:11 – WDTCCS[2:0] WDT Input Clock Selector bits

Value	Description
111	Software Control
110 to 011	Reserved
010	Reserved (no clock)/32 kHz SOSC
001	WDT reference clock is the 31.25 kHz HFINTOSC (MFINTOSC) output
000	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 10:8 – WDTCWS[2:0] WDT Window Select bits

WDTCWS	WDTCON1 [WINDOW] at POR			Software control of WINDOW?	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

Bits 6:5 – WDTE[1:0] WDT Operating Mode bits

Value	Description
11	WDT enabled regardless of Sleep; SEN is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; SEN bit is ignored
01	WDT enabled/disabled by SEN bit
00	WDT disabled, SEN bit is ignored

Bits 4:0 – WDTCPS[4:0] WDT Period Select bits

WDTCPS	WDTCON0[WDTPS] at POR				Software Control of WDTPS?
	Value	Divider Ratio		Typical Time Out (F_{IN} = 31 kHz)	
11111	01011	1:65536	2^{16}	2s	Yes
11110 ... 10011	11110 ... 10011	1:32	2^5	1 ms	No
10010	10010	1:8388608	2^{23}	256s	No
10001	10001	1:4194304	2^{22}	128s	
10000	10000	1:2097152	2^{21}	64s	
01111	01111	1:1048576	2^{20}	32s	
01110	01110	1:524299	2^{19}	16s	
01101	01101	1:262144	2^{18}	8s	
01100	01100	1:131072	2^{17}	4s	
01011	01011	1:65536	2^{16}	2s	
01010	01010	1:32768	2^{15}	1s	
01001	01001	1:16384	2^{14}	512 ms	
01000	01000	1:8192	2^{13}	256 ms	
00111	00111	1:4096	2^{12}	128 ms	
00110	00110	1:2048	2^{11}	64 ms	
00101	00101	1:1024	2^{10}	32 ms	
00100	00100	1:512	2^9	16 ms	
00011	00011	1:256	2^8	8 ms	
00010	00010	1:128	2^7	4 ms	
00001	00001	1:64	2^6	2 ms	
00000	00000	1:32	2^5	1 ms	

1.4.2.4 CONFIG4

Name: CONFIG4
Offset: 0x800A

Configuration Word 4

Memory Write Protection

Bit	15	14	13	12	11	10	9	8
			LVP		$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access			R/W	U	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$			$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
Access	R/W	U	U	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	1

Bit 13 – LVP Low-Voltage Programming Enable bit
The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

The preconditioned (erased) state for this bit is critical.

Value	Description
1	Low-voltage programming enabled. $\overline{\text{MCLR}}/V_{PP}$ pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
0	HV on $\overline{\text{MCLR}}/V_{PP}$ must be used for programming

Bit 11 – $\overline{\text{WRTSAF}}$ Storage Area Flash Write Protection bit(1)

Value	Description
1	SAF NOT write-protected
0	SAF write-protected

Bit 10 – $\overline{\text{WRTD}}$ Data EEPROM Write Protection bit(1)

Value	Description
1	Data EEPROM NOT write-protected
0	Data EEPROM write-protected

Bit 9 – $\overline{\text{WRTC}}$ Configuration Register Write Protection bit(1)

Value	Description
1	Configuration Registers NOT write-protected
0	Configuration Registers write-protected

Bit 8 – $\overline{\text{WRTB}}$ Boot Block Write Protection bit(1)

Value	Description
1	Boot Block NOT write-protected
0	Boot Block write-protected

Bit 7 – $\overline{\text{WRTAPP}}$ Application Block Write Protection bit(1)

Value	Description
1	Application Block NOT write-protected
0	Application Block write-protected

Bit 4 – $\overline{\text{SAFEN}}$ SAF Enable bit(1)

Value	Description
1	SAF disabled
0	SAF enabled

Bit 3 – $\overline{\text{BBEN}}$ Boot Block Enable bit(1)

Value	Description
1	Boot Block disabled
0	Boot Block enabled

Bits 2:0 – BBSIZE[2:0] Boot Block Size Selection bits
BBSIZE is used only when $\overline{\text{BBEN}}$ = 0

BBSIZE bits can only be written while $\overline{\text{BBEN}}$ = 1; after $\overline{\text{BBEN}}$ = 0, BBSIZ is write-protected.

Table 1-1. Boot Block Size Bits

$\overline{\text{BBEN}}$	BBSIZE	Actual Boot Block Size User Program Memory Size (words)			Last Boot Block Memory Access
		4k	8k	16k	
1	xxx	0	0	0	—
0	111	512	512	512	01FFh
0	110	1024	1024	1024	03FFh
0	101	2048	2048	2048	07FFh
0	100		4096	4096	0FFFh
0	011			8192	1FFFh
0	010				
0	001				
0	000				

Note: The maximum boot block size is half the user program memory size. All selections higher than the maximum are set to half size. For example, all BBSIZE = 000 – 100 produce a boot block size of 4 kW on a 8 kW device.

Note:

1. Bits are implemented as sticky bits. Once protection is enabled, it can only be reset through a Bulk Erase.

1.4.2.5 CONFIG5

Name: CONFIG5
Offset: 0x800B

Configuration Word 5

Code Protection

Bit	15	14	13	12	11	10	9	8
Access			U	U	U	U	U	U
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access	U	U	U	U	U	U	U	R/P
Reset	1	1	1	1	1	1	1	1

Bit 0 – $\overline{CP}$ Program Flash Memory Code Protection bit

Value	Description
1	Program Flash Memory code protection disabled
0	Program Flash Memory code protection enabled

1.5 Device Information Area

The Device Information Area (DIA) is a dedicated region in the Program Flash Memory. The data is mapped from 8100h to 811Fh. These locations are read-only and cannot be erased or modified. The DIA holds the calibration data for the temperature indicator module and the FVR voltages, which are useful for temperature sensing applications and calibration.

Related Links

Appendix D: Device Information Area (DIA)

1.6 Device Configuration Information

The Device Configuration Information (DCI) is a dedicated region in the Program Flash Memory mapped from 8200h to 821Fh. The data stored in the DCI memory is hard-coded into the device during manufacturing. The DCI holds information about the device which is useful for programming and bootloaders. These locations are read-only and cannot be erased or modified. For more information, refer to the product-specific data sheet.

Related Links

Appendix C: Device Configuration Information (DCI)

2. Programming Algorithms

2.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs. On entering the Program/Verify mode, the address is cleared.

2.1.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high voltage:

- V_{PP} – First Entry mode
- V_{DD} – First Entry mode

2.1.1.1 V_{PP} – First Entry Mode

To enter Program/Verify mode via the V_{PP}-First mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer is disabled ($\overline{PWRTS}$ = 0), the internal oscillator is selected (F_{OSC} = 100), and ICSPDAT and ICSPCLK are driven by the user application, the device will execute code and may drive the ICSPDAT and ISCPCLK I/O pins. Since code execution may prevent first entry, V_{PP}-First Entry mode is strongly recommended, as it prevents user code from changing EEPROM contents or driving pins to affect Test mode entry.

Related Links

Program/Verify Mode Exit

2.1.1.2 V_{DD} – First Entry Mode

To enter Program/Verify mode via the V_{DD}-First mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-First mode is useful when programming the device when V_{DD} is already applied, for it is not necessary to disconnect V_{DD} to enter Program/Verify mode. During this cycle, any executing code will be interrupted and halted.

Related Links

Program/Verify Mode Exit

2.1.1.3 Program/Verify Mode Exit

To exit Program/Verify mode, lower $\overline{MCLR}$ from V_{IHH} to V_{IL}. V_{DD}-First Entry mode should use V_{DD}-Last Exit mode (see Figure 2-1). V_{PP}-First Entry mode should use V_{PP}-Last Exit mode (see Figure 2-2).

Figure 2-1. Programming Entry and Exit Modes – V_{PP} First and Last

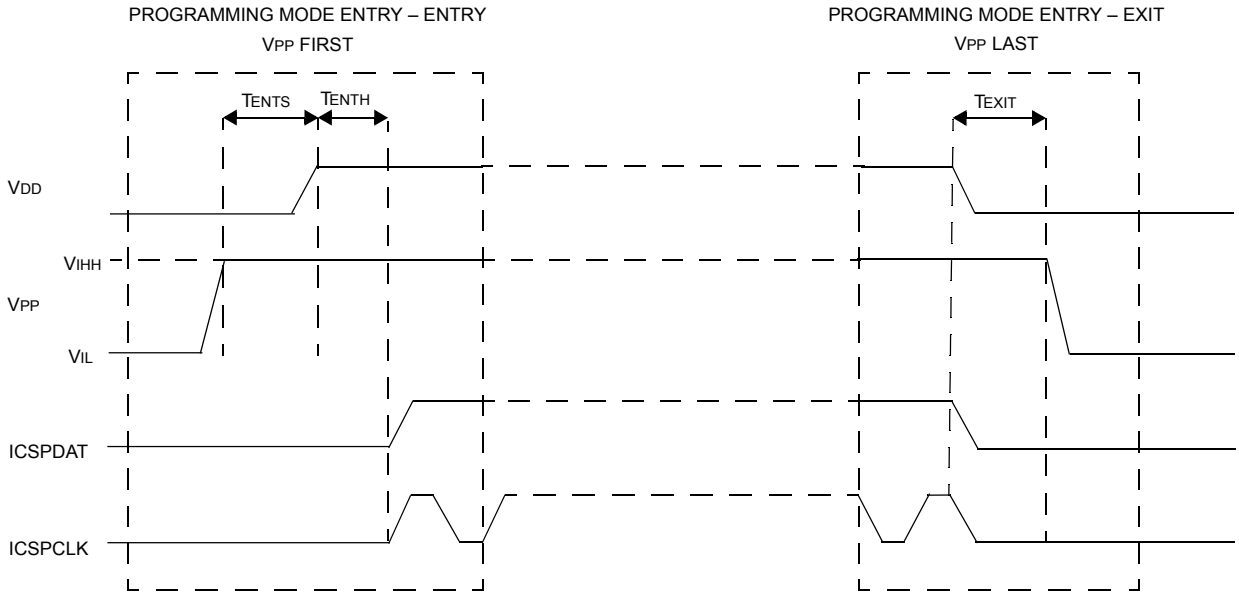
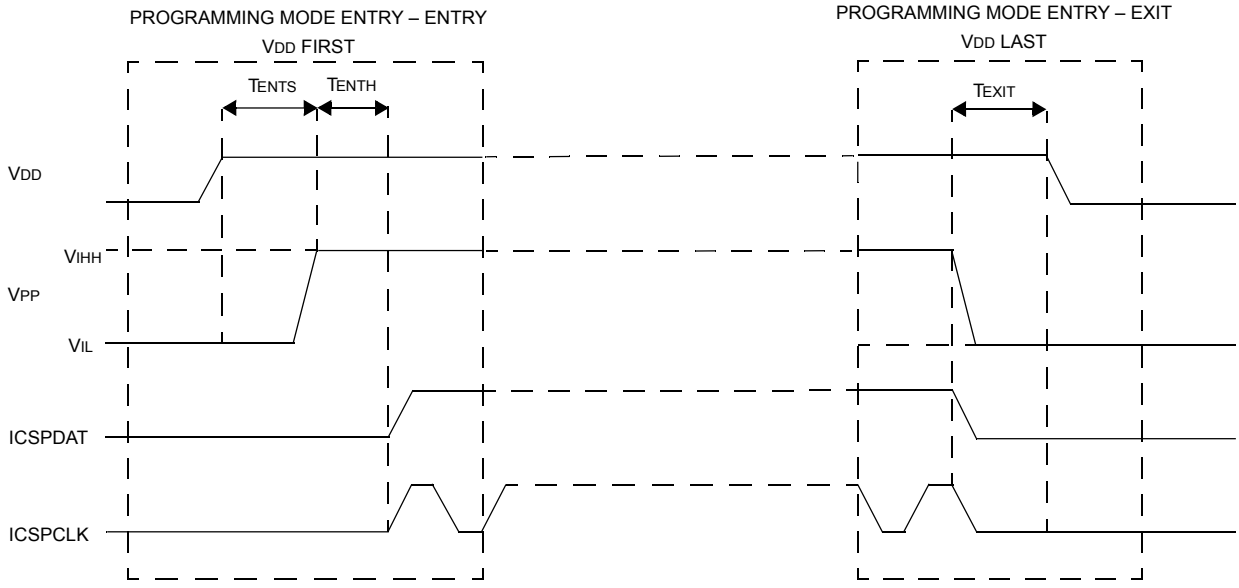


Figure 2-2. Programming Entry and Exit Modes – V_{DD} First and Last



2.1.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit of the Configuration Word 4 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.

2. A 32-bit key sequence is presented on ICSPDAT. The LSb of the pattern is a “don’t care x”. The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required to activate the Program/Verify mode.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant nibble must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained. For low-voltage programming timing, see Figure 2-3 and Figure 2-4.

Figure 2-3. LVP Entry (Powering-Up)

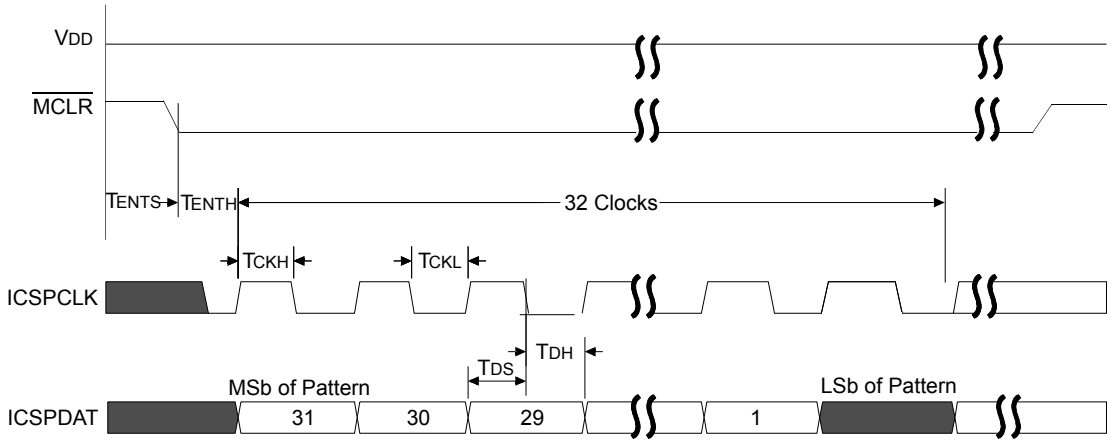
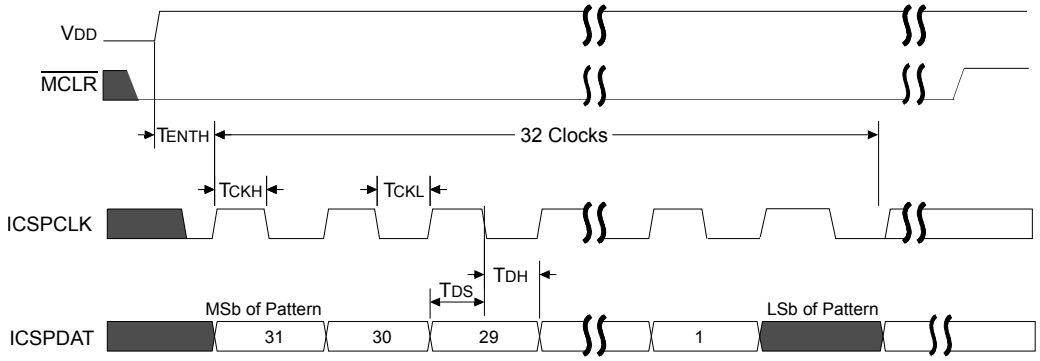


Figure 2-4. LVP Entry (Powered)



Exiting Program/Verify mode is done by raising $\overline{MCLR}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).
Note: To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

2.1.3 Program/Verify Commands

Once a device has entered ICSP Program/Verify mode (using either high voltage or LVP entry), the programming host device may issue commands to the microcontroller, each eight bits in length. The commands are summarized in the following table. The commands are used to erase and program the device. The commands load and use the Program Counter (PC).

Some of the 8-bit commands also have a data payload associated with it (such as Load Data for NVM and Read Data from NVM).

If the programming host device issues an 8-bit command byte that has a data payload associated with it, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes), in order to send or receive the payload data associated with the command.

The actual payload bits associated with a command are command-specific and will be fewer than 24 bits. However, the payload field is always padded with additional Start, Stop and Pad bits, to bring the total payload field size to 24 bits, so as to be compatible with many 8-bit SPI-based systems.

Within a 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a minimum amount of delay (see the following table) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

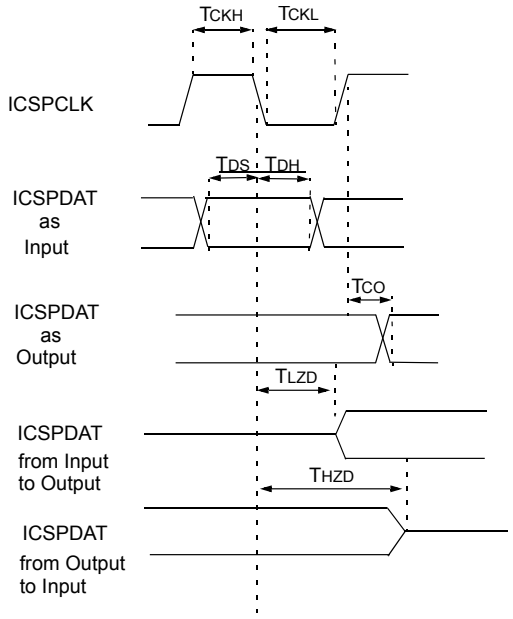
Table 2-1. ICSP™ Command Set Summary

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb...LSb)	Hex			
Load PC Address	1000 0000	80	Yes	T_{DLY}	PC = payload value
Bulk Erase Program Memory	0001 1000	18	No	T_{ERAB}	Depending on the current value of the PC, one or more memory regions.
Row Erase Program Memory	1111 0000	F0	No	T_{ERAR}	The row addressed by the MSbs of the PC is erased; LSbs are ignored.
Load Data for NVM	0000 00J0	00/02	Yes	T_{DLY}	J = 1: PC = PC + 1 after writing J = 0: PC is unchanged
Read Data from NVM	1111 11J0	FE/FC	Yes	T_{DLY}	J = 1: PC = PC + 1 after reading J = 0:

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb...LSb)	Hex			
					PC is unchanged
Increment Address	1111 1000	F8	No	T_{DLY}	PC = PC + 1
Begin Internally Timed Programming	1110 0000	E0	No	T_{PINT}	Commits latched data to NVM (self timed)
Begin Externally Timed Programming	1100 0000	C0	No	T_{PEXT}	Commits latched data to NVM (externally timed). After T_{PEXT}, "End Externally Timed Programming" command must be issued.
End Externally Timed Programming	1000 0010	82	No	T_{DIS}	Should be issued within required time delay (T_{PEXT}) after "Begin Externally Timed Programming" command.

Note: All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. ISCPDAT timing will be met as per Figure 2-5.

Figure 2-5. Clock and Data Timing



2.1.3.1 Load Data for NVM

The Load Data for NVM command is used to load one programming data latch (for example, one 14-bit instruction word for program memory/configuration memory/User ID memory, or one 8-bit byte for an EEPROM data memory address). The Load Data for NVM command can be used to load data for Program Flash Memory (see Figure 2-6) or the EEPROM, if available (see Figure 2-7). The word writes into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming commands write the entire row of data latches, not just one word. The lower five bits of the address are considered, while the other bits are ignored. Depending on the value of bit 1 of the command, the Program Counter (PC) may or may not be incremented (see Table 2-1).

Figure 2-6. Load Data for NVM (Program Flash Memory)

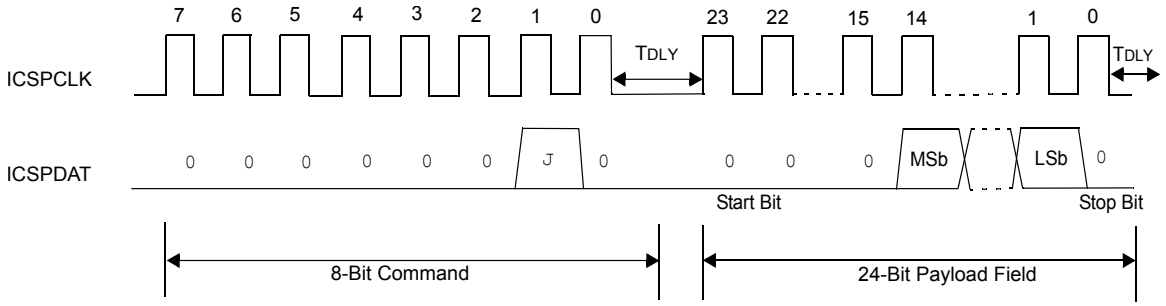
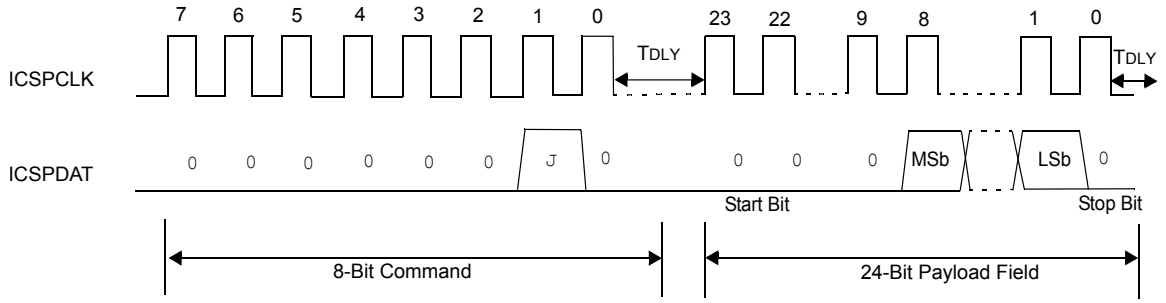


Figure 2-7. Load Data for NVM (EEPROM)



Related Links

Row Erase Memory

2.1.3.2 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of ICSPCLK, and it will revert to Input mode (high-impedance) after the 24th falling edge of the clock. The Start and Stop bits are only one half of a bit time wide, and should, therefore, be ignored by the host programmer device (since the latched value may be indeterminate). Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid, and should ignore the values of the pad bits. If the program memory is code-protected ($\overline{CP}$ = 0), the data will be read as zeros (see Figure 2-8 and Figure 2-9). Depending on the value of bit '1' of the command, the PC may or may not be incremented (see Table 2-1). The Read Data for NVM command can be used to read data for Program Flash Memory (see Figure 2-8) or the EEPROM (see Figure 2-9).

Figure 2-8. Read Data from NVM (Program Flash Memory or Configuration Words)

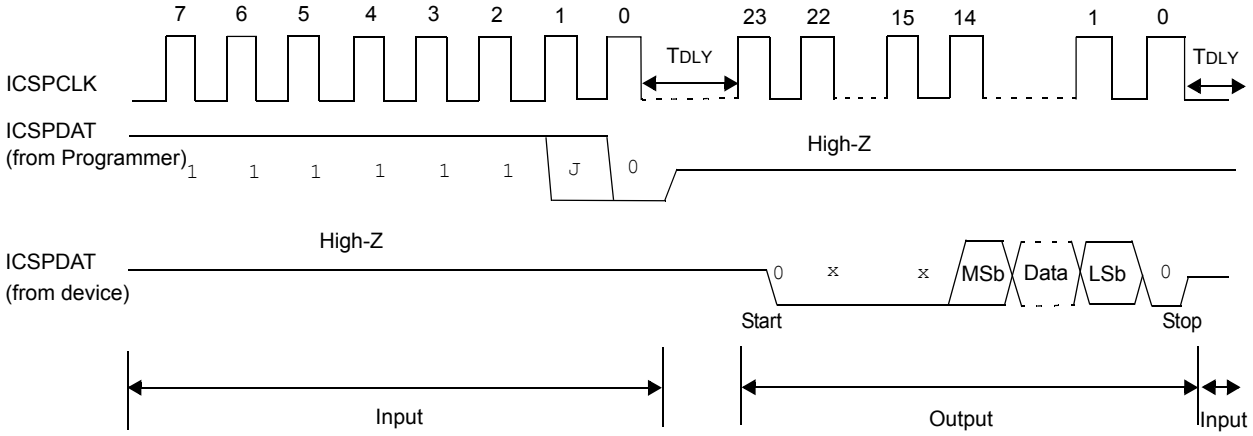
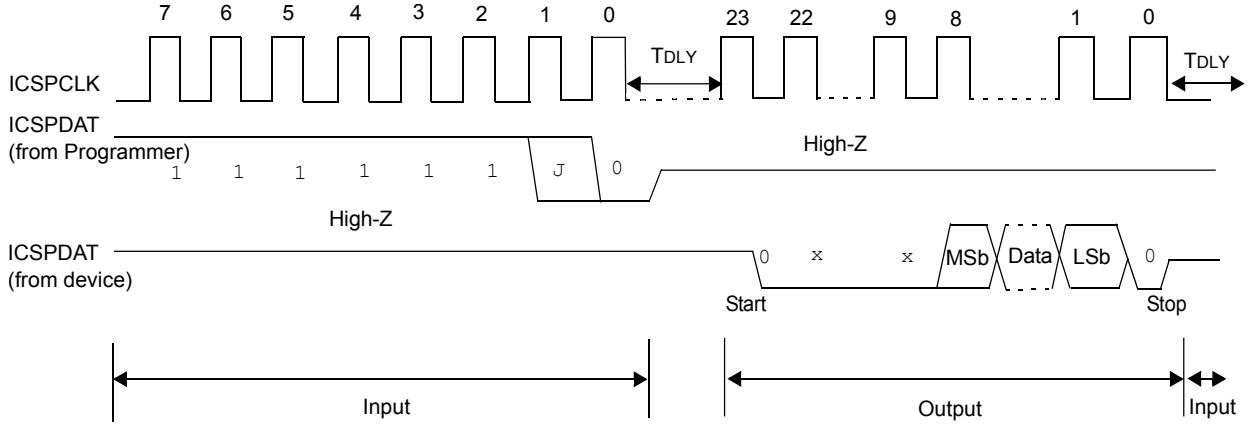


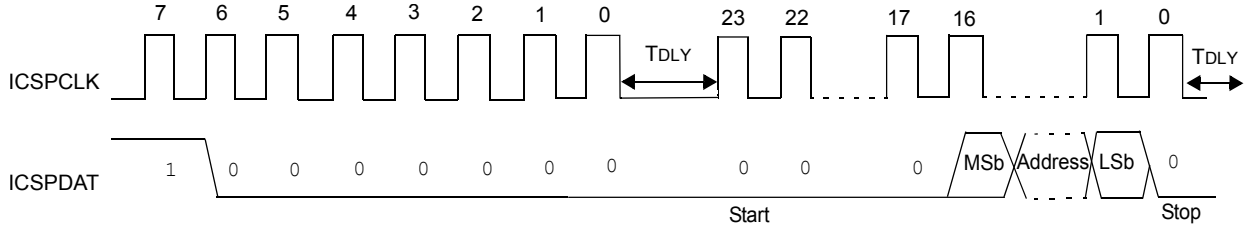
Figure 2-9. Read Data from NVM (EEPROM)



2.1.3.3 Load PC Address

The PC value is set using the supplied data. The address implies the memory panel (Program Flash Memory or EEPROM) to be accessed (see the figure below).

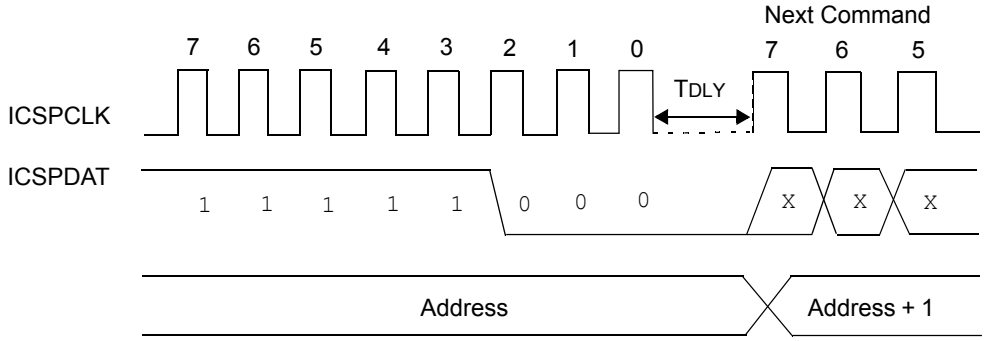
Figure 2-10. Load PC Address



2.1.3.4 Increment Address

The PC is incremented by one when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Load PC Address command. This command performs the same action as the J bit in the Load/Read commands. See the figure below.

Figure 2-11. Increment Address

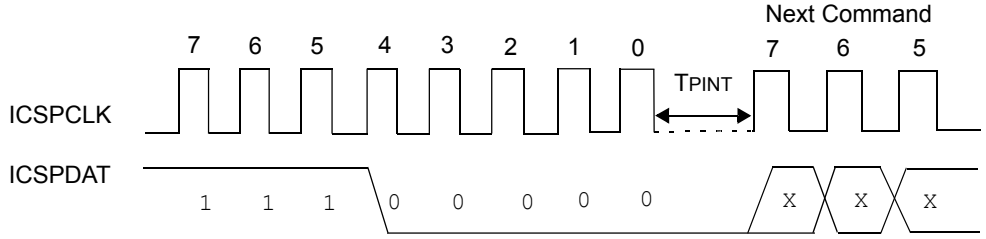


2.1.3.5 Begin Internally Timed Programming

The write programming latches must already have been loaded using the Load Data for NVM command, prior to issuing the Begin Programming command. Programming of the addressed memory row will begin after this command is received. The lower LSBs of the address are ignored. An internal timing mechanism executes the write. The user must allow for the Erase/Write cycle time, T_{PINT}, in order for the programming to complete, prior to issuing the next command (see the figure below).

After the programming cycle is complete all the data latches are reset to '1'.

Figure 2-12. Begin Internally Timed Programming

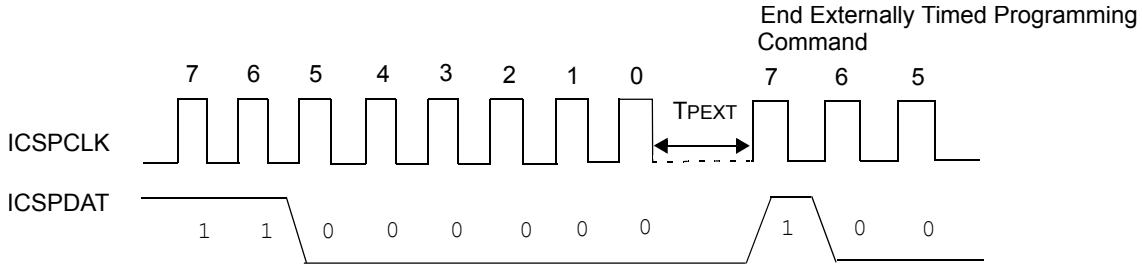


2.1.3.6 Begin Externally Timed Programming

Data to be programmed must be previously loaded by Load Data for NVM command before every Begin Programming command. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see the figure below). The lower LSBs of the address are ignored.

Externally timed writes are not supported for Configuration bits. Any externally timed write to the Configuration Word will have no effect on the targeted word.

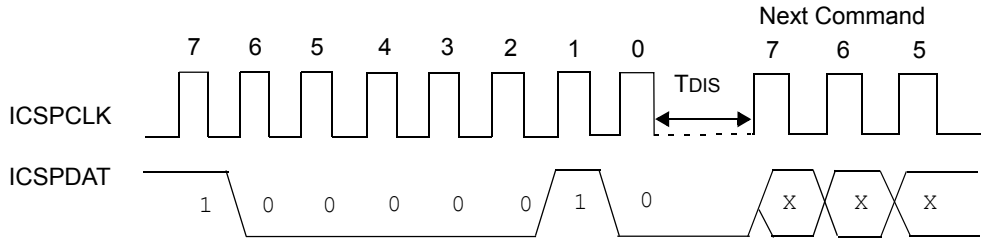
Figure 2-13. Begin Externally Timed Programming



2.1.3.7 End Externally Timed Programming

This command is required to terminate the programming sequence after a Begin Externally Timed Programming command is given. If no programming command is in progress or if the programming cycle is internally timed, this command will execute as a No Operation (NOP) (see the figure below).

Figure 2-14. End Program Timing



2.1.3.8 Bulk Erase Memory

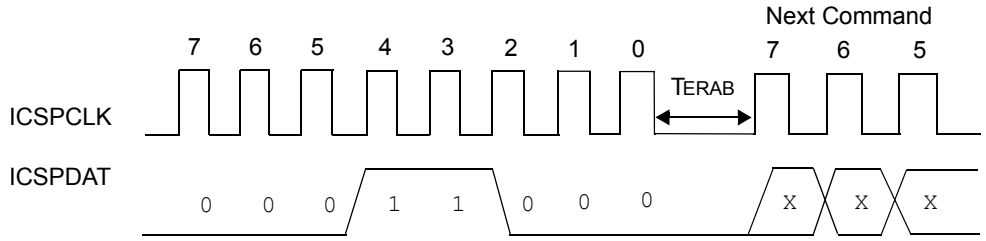
The Bulk Erase Memory command performs different functions dependent on the current PC address. The Bulk Erase command affects specific portions of the memory depending on the initial value of the Program Counter. Whenever a Bulk Erase command is executed, the device will erase all bytes within the regions listed in Table 2-2. While a programming command is in progress, this command executes as a NOP.

After receiving the Bulk Erase Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired (see Figure 2-15). The programming host device should not issue another 8-bit command until after the T_{ERAB} interval has fully elapsed.

Table 2-2. Bulk Erase Table

Address	Area(s) Erased	
	$\overline{CP}$=1	$\overline{CP}$=0
0000h-7FFFh	User Flash	User Flash
	Configuration Words	Configuration Words
8000h-80FDh	User Flash	User Flash
	Configuration Words	Configuration Words
	User ID words	User ID words
80FEh-80FFh	User Flash	User Flash
8100h-E7FFh	No Operation	No Operation
E800h-FFFFh	User Flash	User Flash
	Configuration Words	Configuration Words
	User ID words	User ID words

Figure 2-15. Bulk Erase Memory

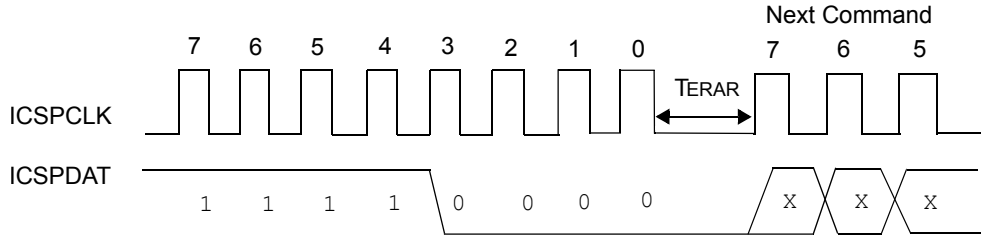


2.1.3.9 Row Erase Memory

If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8004h, the Row Erase Program Memory command will only erase the User ID locations regardless of the setting of the $\overline{CP}$ Configuration bit. The Row Erase Memory command will erase an individual row. When write and erase operations are done on a row basis, the row size (number of 14-bit words) for erase operation is 32 and the row size (number of 14-bit latches) for the write operation is 32.

The Flash memory row defined by the current PC will be erased. The user must wait T_{ERAR} for erasing to complete (see the figure below).

Figure 2-16. Row Erase Memory



2.2 Programming Algorithms

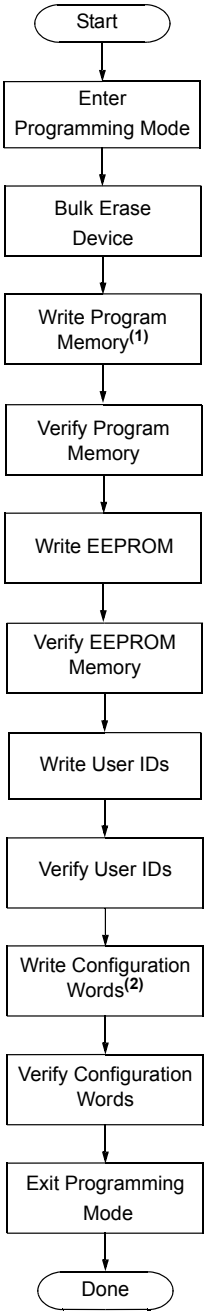
The device uses internal latches to temporarily store the 14-bit words used for programming. The data latches allow the user to program a full row with a single Begin Internally Timed Programming or Begin Externally Timed Programming command. The Load Data for NVM command is used to load a single data latch. The data latch will hold the data until the Begin Internally Timed Programming or Begin Externally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The address at the time the Begin Internally Timed Programming or Begin Externally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address 0002h-0021h in a 32-latch device will result in data being written to 0020h-003Fh.

If more than the maximum number of latches are written without a Begin Internally Timed Programming or Begin Externally Timed Programming command, the data in the data latches will be overwritten. The following flowcharts show the recommended flowcharts for programming.

Note: The Program Flash Memory region is programmed one row (32 words) at a time (Figure 2-20), while the Configuration words are programmed one word at a time (Figure 2-19). The EEPROM region is programmed one byte at a time. The value of the PC at the time of issuing the Begin Internally Timed Programming or Begin Externally Timed Programming command determines what row (of Program Flash Memory), what word (of Configuration Word), or what byte (EEPROM) will get programmed.

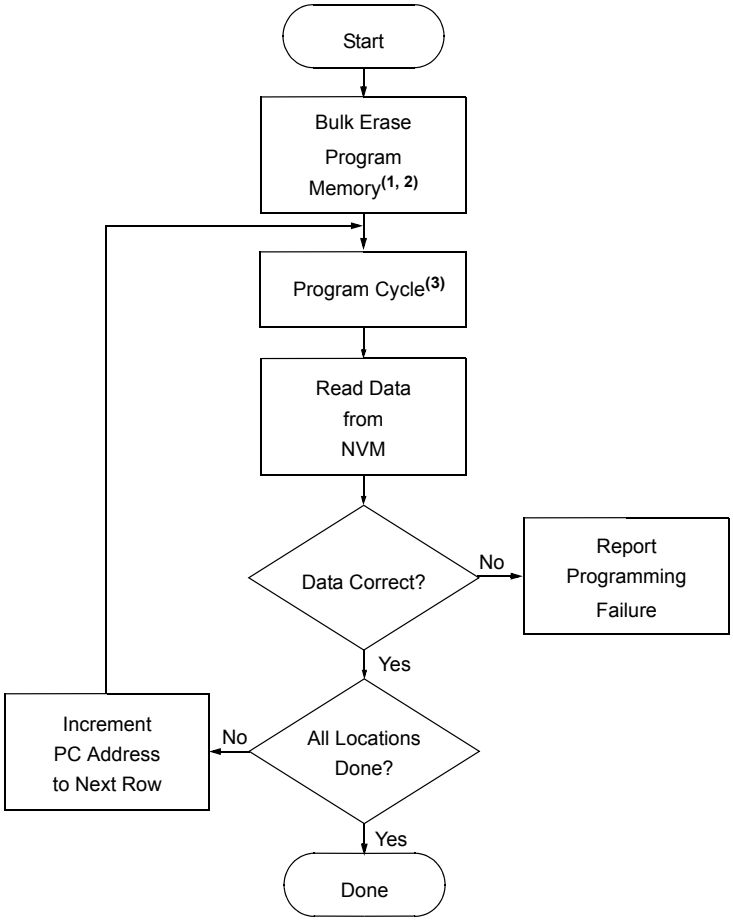
Figure 2-17. Device Program/Verify Flowchart



Note:

1. See Figure 2-10.
2. See Figure 2-16.

Figure 2-18. Program Memory Flowchart



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 3-17.
3. See Figure 2-15.

Figure 2-19. One-Word Program Cycle

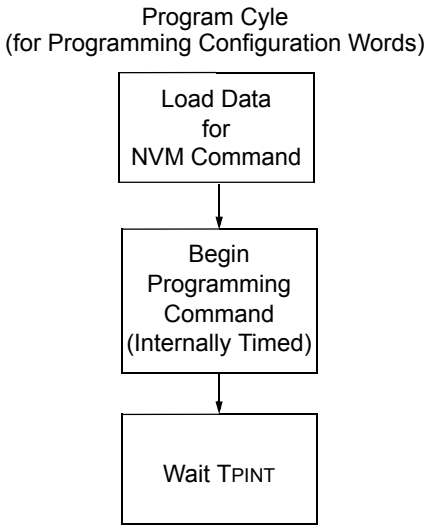


Figure 2-20. Multiple-Word Program Cycle

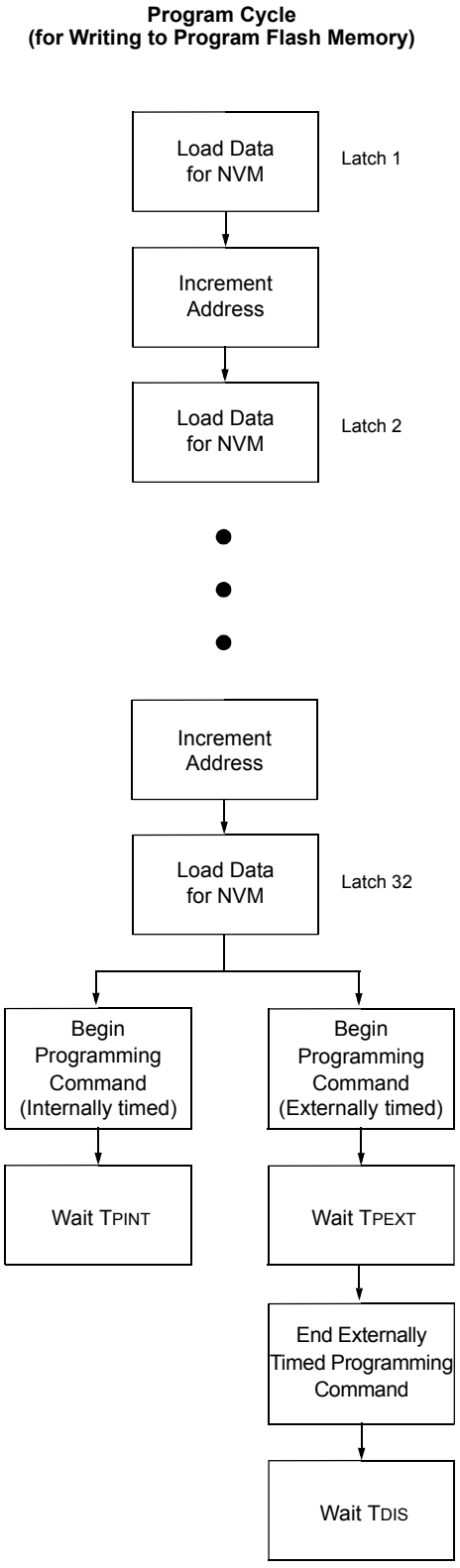
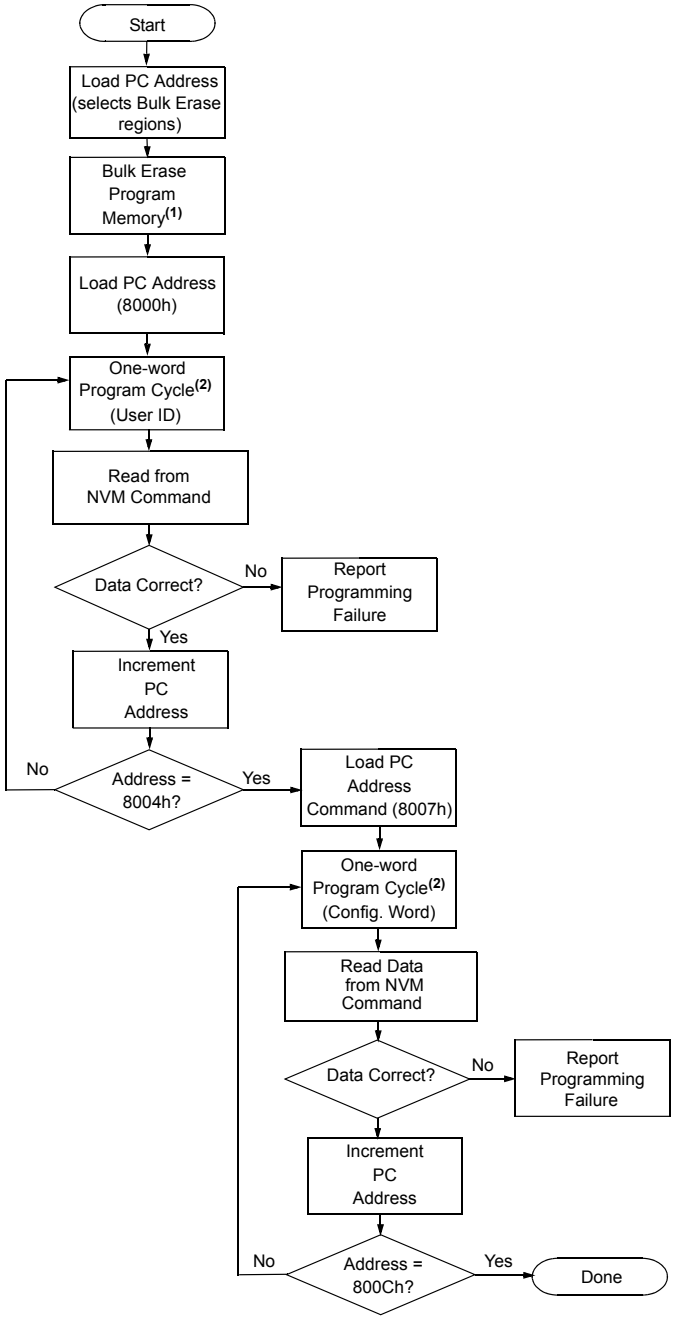


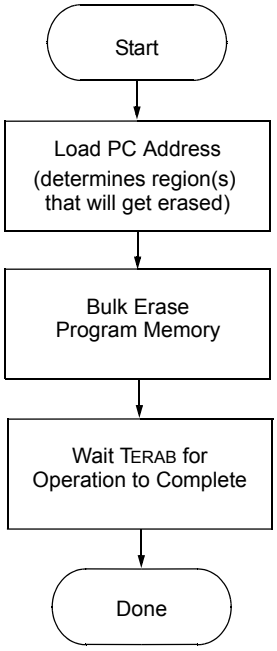
Figure 2-21. Configuration Memory Program Flowchart



Note:

1. This step is optional if the device is erased or not previously programmed.
2. See Figure 2-12.

Figure 2-22. Bulk Erase Flowchart



2.3 Code Protection

Code protection is controlled using the $\overline{CP}$ bit. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh), until the next Bulk Erase operation is performed. Program memory can still be programmed and read during program execution.

The Revision ID, Device ID, Device Information Area, Device Configuration Information, User IDs and Configuration Words can be read out regardless of the code protection settings.

2.3.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit to '0'. The only way to disable code protection is to use the Bulk Erase Memory command (with the PC set to an address so as to Bulk Erase all program Flash contents).

2.4 Hex File Usage

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. For example, if the Configuration Word 1 is stored at 8007h, in the hex file this will be referenced as 1000Eh-1000Fh.

2.4.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and User ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and User ID information should be included.

2.4.2 Device ID

If a Device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the Device ID against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

2.4.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

2.4.3.1 Program Code Protection Disabled

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and summing up the program memory data starting at address 0000h, up to the maximum user addressable location (e.g., 0FFFh). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. For PIC16 devices (14-bit program memory word), the two MSBs are taken as zero. All unimplemented Configuration bits are masked to '0'

Related Links

Device IDs and Checksums

2.4.3.2 Program Code Protection Enabled

When the MPLABX® IDE check box for Project Properties - Building - Insert unprotected checksum in User ID memory is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the User ID. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four User ID locations. The Most Significant checksum nibble is stored in the User ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each User ID is used to create a 16-bit value. The Least Significant nibble of User ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of User ID location 8001h is the second Most Significant nibble, and so forth for the remaining User IDs and 16-bit value nibbles. The resulting 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to '0'.

2.5 Electrical Specifications

Refer to device-specific data sheet for absolute maximum ratings.

Table 2-3. AC/DC Characteristics Timing Requirements for Program/Verify Mode

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics		Min.	Typ.	Max.	Units	Conditions/ Comments
Programming Supply Voltages and Currents							
V_{DD}	Supply Voltage (V_{DDMIN}(1), V_{DDMAX})	PIC16LF184XX	1.80	—	3.60	V	
		PIC16F184XX	2.30	—	5.50	V	
V_{PEW}	Read/Write and Row Erase operations		V_{DDMIN}	—	V_{DDMAX}	V	

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/ Comments
V_{BE}	Bulk Erase operations	V_{BORMAX}(2)	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	5.0	mA	
I_{PP}	**V_{PP}**					
	Current on $\overline{MCLR}/V_{PP}$	—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify Mode Entry	7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/Verify Mode Entry	—	—	1.0	µs	
	I/O pins					
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input High Level	0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input Low Level	—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level	V_{DD}-0.7 V_{DD}-0.7 V_{DD}-0.7	—	—	V	I_{OH} = -3.5 mA, V_{DD} = 5V I_{OH} = -3 mA, V_{DD} = 3.3V I_{OH} = -1 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT Output Low Level	—	—	V_{SS}+0.6 V_{SS}+0.6 V_{SS}+0.6	V	I_{OL} = 8 mA, V_{DD} = 5V I_{OL} = 6 mA, V_{DD} = 3.3V I_{OL} = 1.8 mA, V_{DD} = 1.8V
Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time Before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time after V_{DD} or $\overline{MCLR}$↑	250	—	—	µs	
Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in SETUP TIME before Clock↓	100	—	—	ns	
T_{DH}	Data in HOLD TIME after Clock↓	100	—	—	ns	
T_{CO}	Clock↑ to DATA OUT VALID (during a Read Data Command)	0	—	80	ns	
T_{LZD}	Clock↓ to Data Low-impedance (during a Read Data Command)	0	—	80	ns	
T_{HZD}	Clock↓ to Data High-impedance (during a Read Data command)	0	—	80	ns	

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/ Comments
T_{DLY}	Data Input not Driven To Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase Cycle Time	—	—	8.4	ms	PIC16(L)F184XX devices
T_{ERAR}	Row Erase Cycle Time	—	—	2.8	ms	
T_{PINT}	Internally Timed Programming Operation Time	—	—	2.8	ms	Program memory Configuration Words
		—	—	5.6	ms	
T_{PEXT}	Delay Required between Begin Externally Timed Programming and End Externally Timed Programming Commands	1.0	—	2.1	ms	(Note 3)
T_{DIS}	Delay Required after End Externally Timed Programming Command	300	—	—	µs	
T_{EXIT}	Time Delay when Exiting Program/ Verify Mode	1	—	—	µs	

Note:

1. In case of Bulk Erase, the devices default to brown-out enabled, with BORV = 1 (low trip point). In order to ensure that the device is not held in Brown-out Reset, V_{DDMIN} becomes the V_{BOR} threshold (with BORV = 1) when performing low-voltage programming on a Bulk Erased device.
2. Bulk Erase operation overrides the BOR setting and the minimum V_{BE} threshold is the same for F and LF devices. Refer to the microcontroller data sheet specification for the exact value of V_{BORMAX}.
3. Externally timed writes are not supported for Configuration bits.

3. Appendix A: Revision History (12/2017)

Initial release of this document.

4. Appendix B: Device ID, Checksums and Pinout Descriptions

4.1 Device IDs and Checksums

Device	Device ID	Config. 1		Config. 2		Config. 3		Config. 4		Config. 5			Checksum			
													Unprotected		Code-protected	
		Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (unprotected)	Word (protected)	Mask	Blank (HEX)	00AAh First and Last (HEX)	Blank (HEX)	00AAh First and Last (HEX)
PIC16F18424	30CA	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	C77D	48D3	9EF9	204F
PIC16LF18424	30CB	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	C77D	48D3	9EF9	204F
PIC16F18425	30CC	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16LF18425	30CD	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16F18426	30D2	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F
PIC16LF18426	30D3	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F
PIC16F18444	30CE	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	C77D	48D3	9EF9	204F
PIC16LF18444	30CF	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	C77D	48D3	9EF9	204F
PIC16F18445	30D0	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16LF18445	30D1	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16F18446	30D4	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F
PIC16LF18446	30D5	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F
PIC16F18455	30D7	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16LF18455	30D8	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	B77D	38D3	8EF9	104F
PIC16F18456	30D9	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F
PIC16LF18456	30DA	3FFF	2977	3FFF	3EE7	3FFF	3F7F	3FFF	2F9F	3FFF	3FFE	0001	977D	18D3	6EF9	F04F

4.2 Example: Checksum Computed with Program Code Protection Disabled, Blank Device

Device	Sum of Memory addresses 0000h-0FFFh	F000h (1000h*3FFFh)
PIC16F18424	Configuration Word 1	3FFFh
	Configuration Word 1 mask	2977h
	Configuration Word 2	3FFFh
	Configuration Word 2 mask	3EE7h
	Configuration Word 3	3FFFh
	Configuration Word 3 mask	3F7Fh
	Configuration Word 4	3FFFh

Device	Sum of Memory addresses 0000h-0FFFh	F000h (1000h*3FFFh)
	Configuration Word 4 mask	2F9Fh
	Configuration Word 5 Unprotected	3FFFh
	Configuration Word 5 mask	0001h
	Checksum	= F000h + (3FFFh and 2977h) + (3FFFh and 3EE7h) + (3FFFh and 3F7Fh) + (3FFFh and 2F9Fh) + (3FFFh and 0001h)
		= F000h + 2977h + 3EE7h + 3F7Fh + 2F9Fh + 0001h
		= C77Dh

4.3 Example: Checksum Computed with Program Code Protection Disabled, 00AAh at First and Last Address

Device	Sum of Memory addresses 0000h-0FFFh	7156h (AAh + (FFEh*3FFFh) + AAh)
	Configuration Word 1	3FFFh
	Configuration Word 1 mask	2977h
	Configuration Word 2	3FFFh
	Configuration Word 2 mask	3EE7h
	Configuration Word 3	3FFFh
	Configuration Word 3 mask	3F7Fh
	Configuration Word 4	3FFFh
PIC16F18424	Configuration Word 4 mask	2F9Fh
	Configuration Word 5 Unprotected	3FFFh
	Configuration Word 5 mask	0001h
	Checksum	= 7156h + (3FFFh and 2977h) + (3FFFh and 3EE7h) + (3FFFh and 3F7Fh) + (3FFFh and 2F9Fh) + (3FFFh and 0001h)
		= 7156h + 2977h + 3EE7h + 3F7Fh + 2F9Fh + 0001h
		= 48D3h

4.4 Example: Checksum Computed with Program Code Protection Enabled, Blank Device

Device		
PIC16F18424	Configuration Word 1	3FFFh
	Configuration Word 1 mask	2977h
	Configuration Word 2	3FFFh
	Configuration Word 2 mask	3EE7h
	Configuration Word 3	3FFFh
	Configuration Word 3 mask	3F7Fh
	Configuration Word 4	3FFFh
	Configuration Word 4 mask	2F9Fh
	Configuration Word 5 Unprotected	3FFFh
	Configuration Word 5 mask	0001h
	Sum of User IDs	= (000Ch and 000Fh) << 12 + (0007h and 000Fh) << 8 + (0007h and 000Fh) << 4 + (000Dh and 000Fh)
		= C000h + 0700h + 0070h + 000Dh
		= C77Dh
	Checksum	= (3FFFh and 2977h) + (3FFFh and 3EE7h) + (3FFFh and 3F7Fh) + (3FFFh and 2F9Fh) + (3FFEh and 0001h) + C77Dh
		= 2977h + 3EE7h + 3F7Fh + 2F9Fh + 0000h + C77Dh
		= 9EF9h

Related Links

Program Code Protection Enabled

4.5 Example: Checksum Computed with Program Code Protection Enabled, 00AAh at First and Last Address

Device		
PIC16F18424	Configuration Word 1	3FFFh
	Configuration Word 1 mask	2977h
	Configuration Word 2	3FFFh
	Configuration Word 2 mask	3EE7h
	Configuration Word 3	3FFFh

Device		
	Configuration Word 3 mask	3F7Fh
	Configuration Word 4	3FFFh
	Configuration Word 4 mask	2F9Fh
	Configuration Word 5 Unprotected	3FFFh
	Configuration Word 5 mask	0001h
	Sum of User IDs	(0004h and 000Fh) << 12 + (0008h and 000Fh) << 8 + (000Dh and 000Fh) << 4 + (0003h and 000Fh) = 4000h + 0800h + 00D0h + 0003h = 48D3h
	Checksum	= (3FFFh and 2977h) + (3FFFh and 3EE7h) + (3FFFh and 3F7Fh) + (3FFFh and 2F9Fh) + (3FFEh and 0001h) + 48D3h = 2977h + 3EE7h + 3F7Fh + 2F9Fh + 0000h + 48D3h = 204Fh

Related Links

Program Code Protection Enabled

4.6 Programming Pin Locations by Package Type

Device	Package Type	Pkg. Code	Package Drawing Number(1)	VDD PIN	VSS PIN	MCLR		ICSPCLK		ICSPDAT	
						PIN	PORT	PIN	PORT	PIN	PORT
PIC16(L)F18424 PIC16(L)F18425 PIC16(L)F18426	14 - PDIP	(P)	C04-005	1	14	4	RA3	12	RA1	13	RA0
	14 - SOIC (3.9mm)	(SL)	C04-065	1	14	4	RA3	12	RA1	13	RA0
	14 - TSSOP	(ST)	C04-087	1	14	4	RA3	12	RA1	13	RA0
	16 - uQFN (4x4)	(JQ)	C04-257	16	13	3	RA3	11	RA1	12	RA0
PIC16(L)F18444 PIC16(L)F18445 PIC16(L)F18446	20 - PDIP	(P)	C04-019	1	20	4	RA3	18	RA1	19	RA0
	20 - SOIC	(SO)	C04-094	1	20	4	RA3	18	RA1	19	RA0
	20 - SSOP	(SS)	C04-072	1	20	4	RA3	18	RA1	19	RA0
	20 - uQFN (4x4)	(GZ)	C04-255	18	17	1	RA3	15	RA1	16	RA0
PIC16(L)F18455 PIC16(L)F18456	28 - SPDIP	(SP)	C04-070	20	19	1	RE3	27	RB6	28	RB7
	28 - SSOP	(SS)	C04-073	20	19	1	RE3	27	RB6	28	RB7
	28 - SOIC	(SO)	C04-052	20	19	1	RE3	27	RB6	28	RB7
	28 - uQFN (4x4)	(MV)	C04-152	17	16	26	RE3	24	RB6	25	RB7

Note:

Device	Package Type	Pkg. Code	Package Drawing Number(1)	VDD PIN	VSS PIN	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
						PIN	PORT	PIN	PORT	PIN	PORT

1. The most current package drawings can be found in the Microchip Packaging Specification DS00049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

5. Appendix C: Device Configuration Information (DCI)

Table 5-1. Device Configuration Information

Address	Description	Value	Units
8200h	Erase Row Size	32	Words
8201h	Number of Write Latches	32	—
8202h	Number of User Rows	See Table 5-2	Rows
8203h	EE Data Memory Size	256	Bytes
8204h	Pin Count	See Table 5-3	Pins

Table 5-2. Number of User Rows

Part Name	Memory Size	Number of User Rows
PIC16(L)F18424/18444	4k	128
PIC16(L)F18425/18445/18455	8k	256
PIC16(L)F18426/18446/18456	16k	512

Table 5-3. Pin Count

Part Number	Pin Count
PIC16(L)F18424/25/26	14(1)
PIC16(L)F18444/45/46	20
PIC16(L)F18455/18456	28

Note:

1. 16 pin-count devices will show ‘14’ in location `8204h`

6. Appendix D: Device Information Area (DIA)

Table 6-1. Device Information Area Address Locations and Descriptions

Address Range	Standard Device Information	Description
8100h 8108h	Microchip Unique Identifier (MUI)	Unique indentifier based on silicon die information
8109h	Reserved	Reserved
810Ah 8111h	External Unique Indentifier (EUI)	Optional area for placing customer-specific data
8112h	Unassigned	Unassigned
8113h	Temp Sensor (Low-Range setting) @ 90°C	ADC conversion data of the Temperature Sensor (Low-Range setting) at 90°C setpoint V_{DD} = 3.0V, V_{REF+} = 2.048 from FVR1
8114h	Reserved	Reserved
8115h	Unassigned	Unassigned
8116h	Temp Sensor (High-Range setting) @ 90°C	ADC conversion data of the Temperature Sensor (High-Range setting) at 90°C setpoint V_{DD} = 3.0V, V_{REF+} = 2.048 from FVR1
8117h	Reserved	Reserved
8118h	ADC FVR1 Output Voltage for 1x setting	FVR1 1x measured output voltage (mV)
8119h	ADC FVR1 Output Voltage for 2x setting	FVR1 2x measured output voltage (mV)
811Ah	ADC FVR1 Output Voltage for 4x setting	FVR1 4x measured output voltage (mV)
811Bh	CMP FVR2 Output Voltage for 1x setting	FVR2 1x measured output voltage (mV)
811Ch	CMP FVR2 Output Voltage for 2x setting	FVR2 2x measured output voltage (mV)
811Dh	CMP FVR2 Output Voltage for 4x setting	FVR2 4x measured output voltage (mV)
811Eh 811Fh	Reserved	Reserved

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