FM28V100

1-Mbit (128 K × 8) F-RAM Memory

Features

- 1-Mbit ferroelectric random access memory (F-RAM) logically organized as 128 K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (see the Data Retention and Endurance table)
  - NoDelay™ writes
  - Page mode operation to 30 ns cycle time
  - Advanced high-reliability ferroelectric process
- SRAM compatible
  - Industry-standard 128 K × 8 SRAM pinout
  - 60-ns access time, 90-ns cycle time
- Superior to battery-backed SRAM modules
  - No battery concerns
  - Monolithic reliability
  - True surface mount solution, no rework steps
  - Superior for moisture, shock, and vibration
- Low power consumption
  - Active current 7 mA (typ)
  - Standby current 90 µA (typ)
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- 32-pin thin small outline package (TSOP) Type I
- Restriction of hazardous substances (RoHS) compliant

Functional Overview

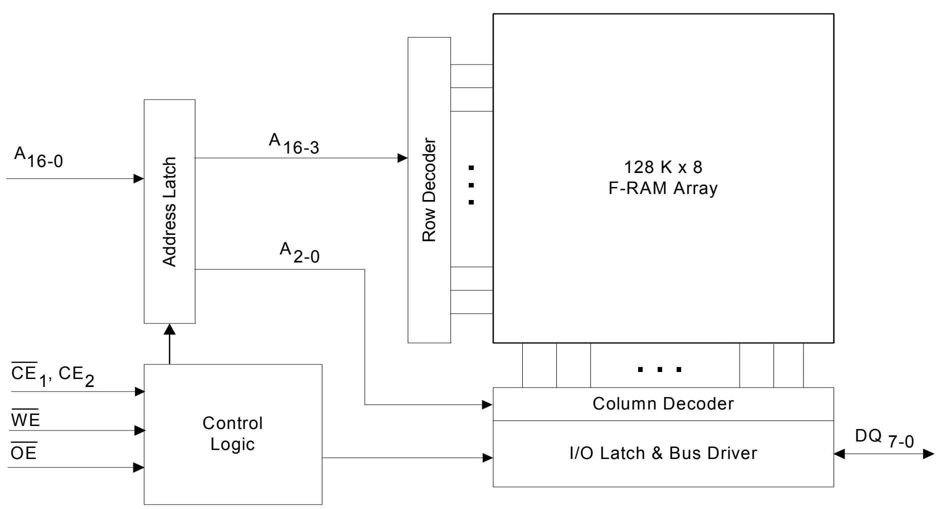
The FM28V100 is a 128 K × 8 nonvolatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 151 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

The FM28V100 operation is similar to that of other RAM devices and therefore, it can be used as a drop-in replacement for a standard SRAM in a system. Read and write cycles may be triggered by chip enable or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM28V100 ideal for nonvolatile memory applications requiring frequent or rapid writes.

The device is available in a 32-pin TSOP I surface mount package. Device specifications are guaranteed over the industrial temperature range –40 °C to +85 °C.

For a complete list of related documentation, click here.

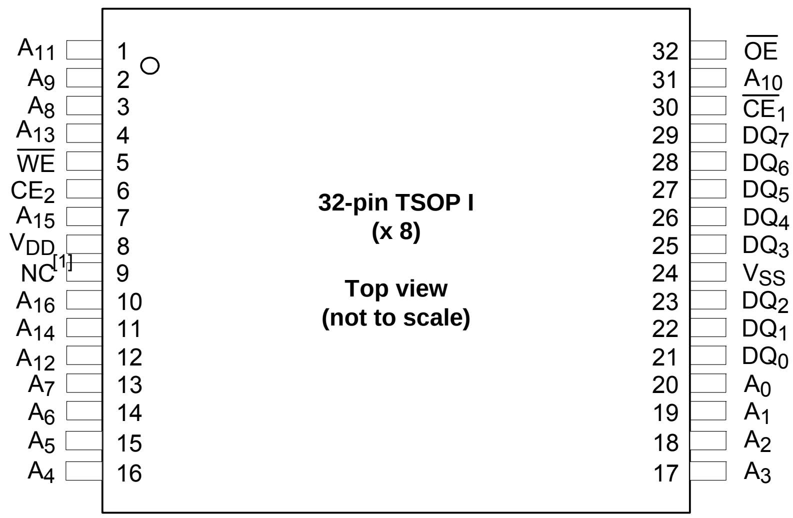
Logic Block Diagram



Contents

Pinout

Figure 1. 32-pin TSOP I pinout



Pin Definitions

Pin Name	I/O Type	Description
A_{16}–A_0	Input	**Address inputs**: The 17 address lines select one of 131,072 bytes in the F-RAM array. The lowest two address lines A_2–A_0 may be used for page mode read and write operations.
DQ_7–DQ_0	Input/Output	**Data I/O Lines**: 8-bit bidirectional data bus for accessing the F-RAM array.
$\overline{WE}$	Input	**Write Enable**: A write cycle begins when $\overline{WE}$ is asserted. The rising edge causes the FM28V100 to write the data on the DQ bus to the F-RAM array. The falling edge of $\overline{WE}$ latches a new column address for page mode write cycles.
$\overline{CE}_1$, CE_2	Input	**Chip Enable**: The device is selected and a new memory access begins on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH) or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW). The entire address is latched internally at this point. The CE_2 pin is pulled up internally. Subsequent changes to the A_2–A_0 address inputs allow page mode operation.
$\overline{OE}$	Input	**Output Enable**: When $\overline{OE}$ is LOW, the FM28V100 drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.
NC	No connect	No connect. This pin is not connected to the die.

Note
1. Reserved for address A_{17} on 2-Mbit device.

Device Operation

The FM28V100 is a byte-wide F-RAM memory logically organized as 131,072 × 8 and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation, which provides high-speed access to addresses within a page (row). Access to a different page requires that either chip enable transitions LOW or the upper address (A_{16}–A_3) changes. See the Functional Truth Table on page 13 for a complete description of read and write modes.

Memory Operation

Users access 131,072 memory locations, each with 8 data bits through a parallel interface. The F-RAM array is organized as 16,384 rows and each row has eight column locations, which allow fast access in page mode operation. When an initial address is latched by the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH), or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW), subsequent column locations may be accessed without the need to toggle chip enable. When chip enable pin is deasserted HIGH, a pre-charge operation begins. Writes occur immediately at the end of the access with no delay. The $\overline{WE}$ pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay writes.

Read Operation

A read operation begins on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH), or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW). The chip enable initiated access causes the address to be latched and starts a memory read cycle if $\overline{WE}$ is HIGH. Data becomes available on the bus after the access time is met. When the address is latched and the access completed, a new access to a random location (different row) may begin while both chip enables are still active. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM28V100's chip enable-initiated access time is faster than the address access time.

The FM28V100 will drive the data bus when $\overline{OE}$ is asserted LOW and the memory access time is met. If $\overline{OE}$ is asserted after the memory access time is met, the data bus will be driven with valid data. If $\overline{OE}$ is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven to the bus. When $\overline{OE}$ is deasserted HIGH, the data bus will remain in a HI-Z state.

Write Operation

In the FM28V100, writes occur in the same interval as reads. The FM28V100 supports both chip enable and $\overline{WE}$ controlled write cycles. In both cases, the address is latched on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH), or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW).

In a chip enable-controlled write, the $\overline{WE}$ signal is asserted before beginning the memory cycle. That is, $\overline{WE}$ is LOW when the device is activated with the chip enable. In this case, the device begins the memory cycle as a write. The FM28V100 will not drive the data bus regardless of the state of $\overline{OE}$ as long as $\overline{WE}$ is LOW. Input data must be valid when the device is deselected with a chip enable. In a $\overline{WE}$-controlled write, the memory cycle begins when the device is activated with a chip enable. The $\overline{WE}$ signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if $\overline{OE}$ is LOW; however, it will be HI-Z when $\overline{WE}$ is asserted LOW. The chip enable and $\overline{WE}$ controlled write timing cases are shown in the page 11. In the Figure 8 on page 11 diagram, the data bus is shown as a HI-Z condition while the chip is write-enabled and before the required setup time. Although this is drawn to look like a mid-level voltage, it is recommended that all DQ pins comply with the minimum V_{IH}/V_{IL} operating levels.

Write access to the array begins on the falling edge of $\overline{WE}$ after the memory cycle is initiated. The write access terminates on the deassertion of $\overline{WE}$ or $\overline{CE}_1$ or CE_2, whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting $\overline{WE}$ or chip enable. The data setup time indicates the interval during which data cannot change before the end of the write access.

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The FM28V100 provides the user fast access to any data within a row element. Each row has eight column-address locations (bytes). Address inputs A_2–A_0 define the column address to be accessed. An access can start anywhere within a row and other column locations may be accessed without the need to toggle the chip enable pins. For fast access reads, after the first data byte is driven to the bus, the column address inputs A_2–A_0 may be changed to a new value. A new data byte is then driven to the DQ pins. For fast access writes, the first write pulse defines the first write access. While the device is selected (both chip enables asserted), a subsequent write pulse along with a new column address provides a page mode write access.

Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. Pre-charge is user-initiated by driving at least one of the chip enable signals to an inactive state. The chip enable must remain inactive at least the minimum pre-charge time, t_{PC}.

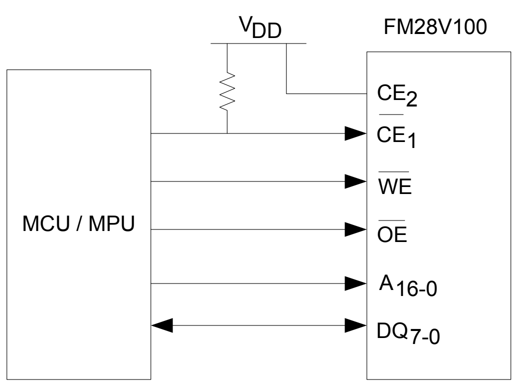
Pre-charge is also activated by changing the upper addresses, A_{16}–A_3. The current row is first closed before accessing the new row. The device automatically detects an upper order address change, which starts a pre-charge operation. The new address is latched and the new read data is valid within the t_{AA} address access time; see Figure 4 on page 10. A similar sequence occurs for write cycles; see Figure 9 on page 11. The rate at which random addresses can be issued is t_{RC} and t_{WC}, respectively.

SRAM Drop-In Replacement

The FM28V100 is designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require chip enable pins to toggle for each new address. Both chip enable pins may remain active indefinitely while V_{DD} is applied. When both chip enable pins are active, the device automatically detects address changes and a new access begins. It also allows page mode operation at speeds up to 33 MHz.

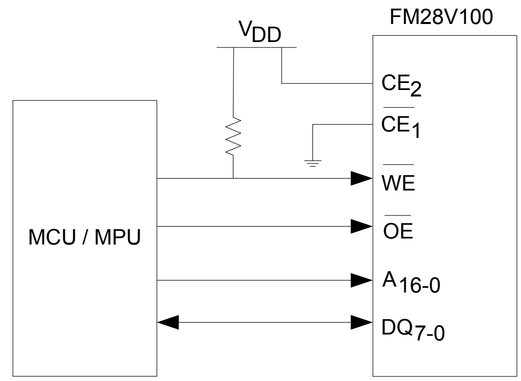
A typical application is shown in Figure 2. It shows a pull-up resistor on $\overline{CE}_1$, which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin tristates during the reset condition.The pull-up resistor value should be chosen to ensure the $\overline{CE}_1$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{CE}_1$ is LOW is not an issue. Although not required, it is recommended that CE_2 be tied to V_{DD} if the controller provides an active-low chip enable. A 10-kΩ resistor draws 330 μA when $\overline{CE}_1$ is LOW and V_{DD} = 3.3 V.

Figure 2. Use of Pull-up Resistor on $\overline{CE}_1$



Note that if $\overline{CE}_1$ is tied to ground and CE2 tied to V_{DD}, the user must be sure $\overline{WE}$ is not LOW at power-up or power-down events. If the chip is enabled and $\overline{WE}$ is LOW during power cycles, data will be corrupted. Figure 3 shows a pull-up resistor on $\overline{WE}$, which will keep the pin HIGH during power cycles, assuming the MCU/MPU pin tristates during the reset condition.The pull-up resistor value should be chosen to ensure the $\overline{WE}$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{WE}$ is LOW is not an issue. A 10-kΩ resistor draws 330 μA when $\overline{WE}$ is LOW and V_{DD} = 3.3 V.

Figure 3. Use of Pull-up Resistor on $\overline{WE}$



For applications that require the lowest power consumption, the chip enable signal should be active only during memory accesses. Due to the external pull-up resistor, some supply current will be drawn while $\overline{CE}_1$ is LOW. When $\overline{CE}_1$ is HIGH, the device draws no more than the maximum standby current I_{SB}.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .... –55 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature .... 1000 h
At 85 °C ambient temperature .... 10 Years

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} ....–1.0 V to + 4.5 V

Voltage applied to outputs
in High Z state ....–0.5 V to V_{DD} + 0.5 V

Input voltage .... –1.0 V to + 4.5 V and $V_{IN} < V_{DD}$ + 1.0 V

Transient voltage (< 20 ns) on
any pin to ground potential ....–2.0 V to V_{CC} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) .... 1.0 W

Surface mount Pb soldering
temperature (3 seconds) .... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Static discharge voltage
Human Body Model (AEC-Q100-002 Rev. E) .... 2 kV
Charged Device Model (AEC-Q100-011 Rev. B) .. 1.25 kV
Machine Model (AEC-Q100-003 Rev. E) .... 200 V

Latch-up current .... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [2]	Max	Unit
V_{DD}	Power supply voltage		2.0	3.3	3.6	V
I_{DD}	V_{DD} supply current	V_{DD} = 3.6 V, chip enable cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V_{DD} – 0.2 V), all DQ pins unloaded.	–	7	12	mA
I_{SB}	Standby current	V_{DD} = 3.6 V, $\overline{CE}_1$ at V_{DD} or CE_2 at V_{SS}, All other pins are static and at CMOS levels (0.2 V or V_{DD} – 0.2 V)	–	90	150	μA
I_{LI}	Input leakage current	V_{IN} between V_{DD} and V_{SS}	–	–	±1	μA
I_{LO}	Output leakage current	V_{OUT} between V_{DD} and V_{SS}	–	–	±1	μA
V_{IH}	Input HIGH voltage		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		– 0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1.0 mA, V_{DD} > 2.7 V	2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 μA	V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} > 2.7 V	–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 μA	–	–	0.2	V
R_{IN}[3]	Address input resistance (CE_2)	For $V_{IN} = V_{IH}$(min)	40	–	–	kΩ
		For $V_{IN} = V_{IL}$(max)	1	–	–	MΩ

Note
2. Typical values are at 25 °C, $V_{DD} = V_{DD}$ (typ). Not 100% tested.
3. The input pull-up circuit is strong (> 40 kΩ) when the input voltage is above V_{IH} and weak (> 1 MΩ) when the input voltage is below V_{IL}.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	At +85 °C	10	–	Years
		At +75 °C	38	–	
		At +65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

Parameter	Description	Test Conditions	Max	Unit
$C_{I/O}$	Input/Output capacitance (DQ)	T_A = 25 °C, f = 1 MHz, $V_{DD} = V_{DD}$(Typ)	8	pF
C_{IN}	Input capacitance		6	pF

Thermal Resistance

Parameter	Description	Test Conditions	32-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	80	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21	°C/W

AC Test Conditions

Input pulse levels ....0 V to 3 V

Input rise and fall times (10%–90%) .... $\leq$ 3 ns

Input and output timing reference levels .... 1.5 V

Output load capacitance... 30 pF

AC Switching Characteristics

Over the Operating Range

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{CE}	t_{ACE}	Chip enable access time	–	70	–	60	ns
t_{RC}	–	Read cycle time	105	–	90	–	ns
t_{AA}	–	Address access time	–	105	–	90	ns
t_{OH}	t_{OHA}	Output hold time	20	–	20	–	ns
t_{AAP}	–	Page mode address access time	–	40	–	30	ns
t_{OHP}	–	Page mode output hold time	3	–	3	–	ns
t_{CA}	–	Chip enable active time	70	–	60	–	ns
t_{PC}	–	Pre-charge time	35	–	30	–	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}_1$, CE_2 active)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time (Chip Enable Controlled)	70	–	60	–	ns
t_{OE}	t_{DOE}	Output enable access time	–	25	–	15	ns
t_{HZ}[5, 6]	t_{HZCE}	Chip Enable to output HI-Z	–	10	–	10	ns
t_{OHZ}[5, 6]	t_{HZOE}	Output enable HIGH to output HI-Z	–	10	–	10	ns

Notes

4. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 0 to 3 V, output loading of the specified I_{OL}/I_{OH} and load capacitance shown in AC Test Conditions on page 7.
5. t_{HZ} and t_{OHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.

AC Switching Characteristics (continued)

Over the Operating Range

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	105	–	90	–	ns
t_{CA}	–	Chip enable active time	70	–	60	–	ns
t_{CW}	t_{SCE}	Chip enable to write enable HIGH	70	–	60	–	ns
t_{PC}	–	Pre-charge time	35	–	30	–	ns
t_{PWC}	–	Page mode write enable cycle time	40	–	30	–	ns
t_{WP}	t_{PWE}	Write enable pulse width	22	–	18	–	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}_1$, CE_2 active)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time (Chip Enable Controlled)	70	–	60	–	ns
t_{ASP}	–	Page mode address setup time (to $\overline{WE}$ LOW)	8	–	5	–	ns
t_{AHP}	–	Page mode address hold time (to $\overline{WE}$ LOW)	20	–	15	–	ns
t_{WLC}	t_{PWE}	Write enable LOW to chip disabled	30	–	25	–	ns
t_{WLA}	–	Write enable LOW to A_{16-3} change	30	–	25	–	ns
t_{AWH}	–	A_{16-3} change to write enable HIGH	105	–	90	–	ns
t_{DS}	t_{SD}	Data input setup time	20	–	15	–	ns
t_{DH}	t_{HD}	Data input hold time	0	–	0	–	ns
t_{WZ} [7, 8]	t_{HZWE}	Write enable LOW to output HI-Z	–	10	–	10	ns
t_{WX} [8]	–	Write enable HIGH to output driven	5	–	5	–	ns
t_{WS} [8, 9]	–	Write enable to $\overline{CE}$ LOW setup time	0	–	0	–	ns
t_{WH} [8, 9]	–	Write enable to $\overline{CE}$ HIGH hold time	0	–	0	–	ns

Notes
7. t_{WZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
8. This parameter is characterized but not 100% tested.
9. The relationship between $\overline{CE}$ (falling edge of $\overline{CE}_1$ (while CE_2 is HIGH), or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW) and $\overline{WE}$ determines if a chip enable or $\overline{WE}$ controlled write occurs.

Figure 4. Read Cycle Timing 1 ($\overline{CE_1}$ LOW, CE_2 HIGH, $\overline{OE}$ LOW)

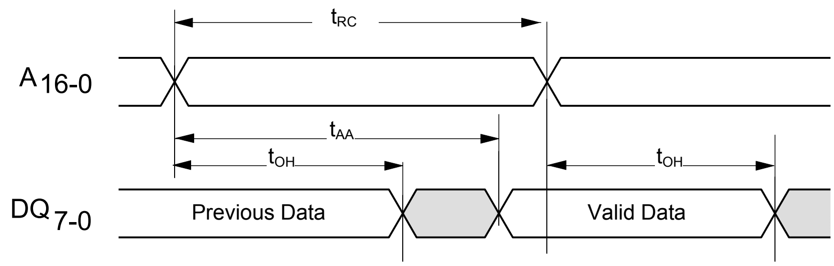


Figure 5. Read Cycle Timing 2 (Chip Enable Controlled)

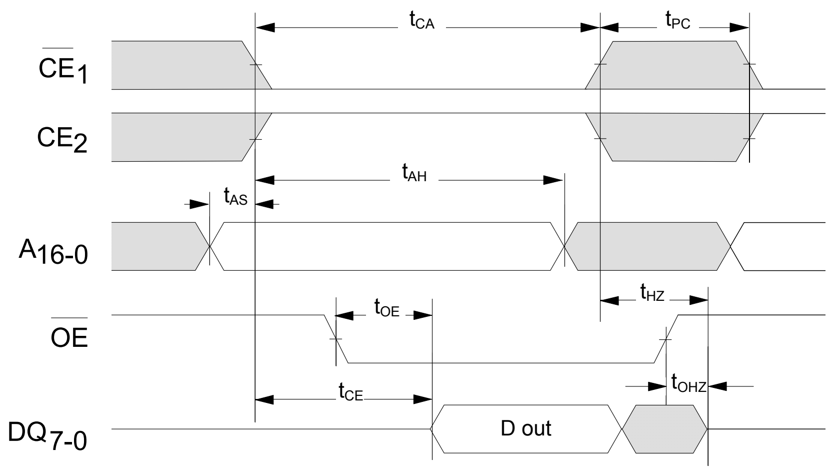
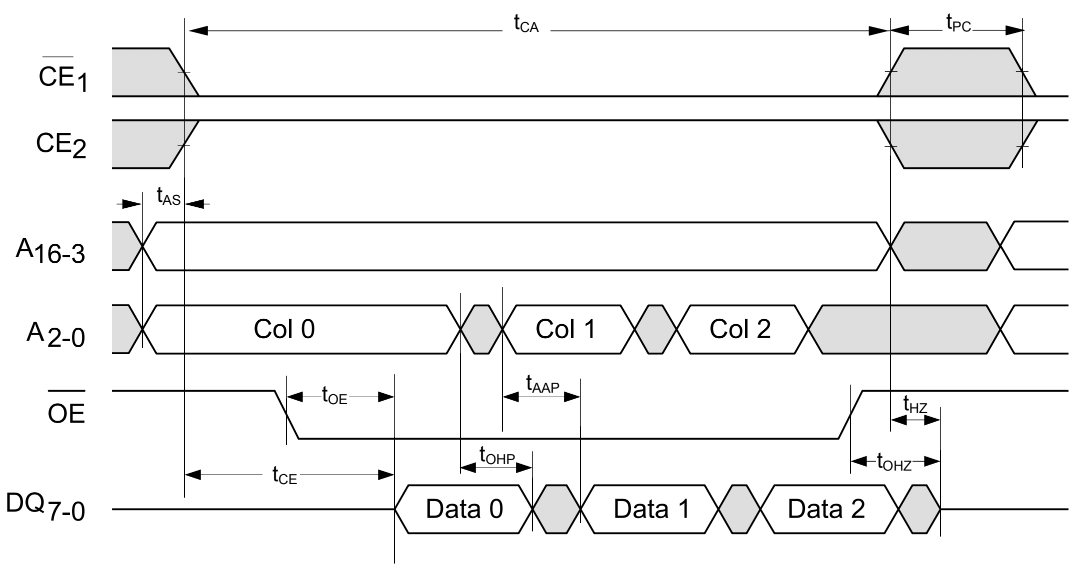


Figure 6. Page Mode Read Cycle Timing [10]



Note

10. Although sequential column addressing is shown, it is not required

Figure 7. Write Cycle Timing 1 ($\overline{WE}$ Controlled) [11]

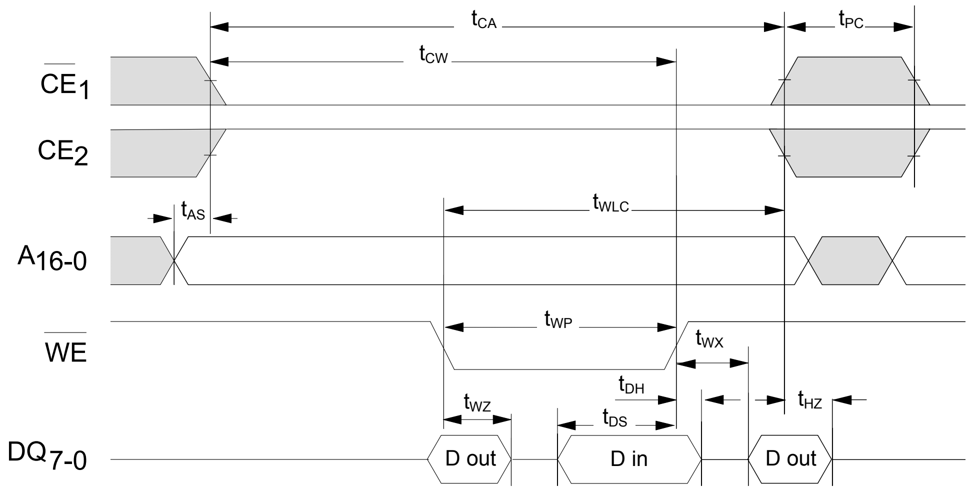


Figure 8. Write Cycle Timing 2 ($\overline{CE}$ Controlled)

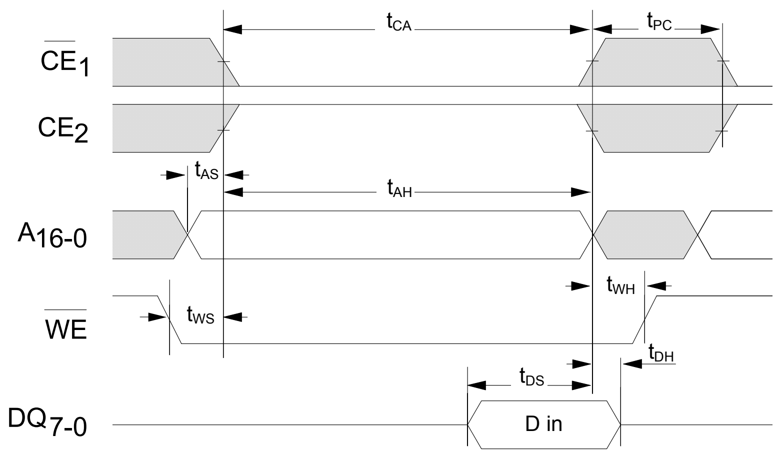
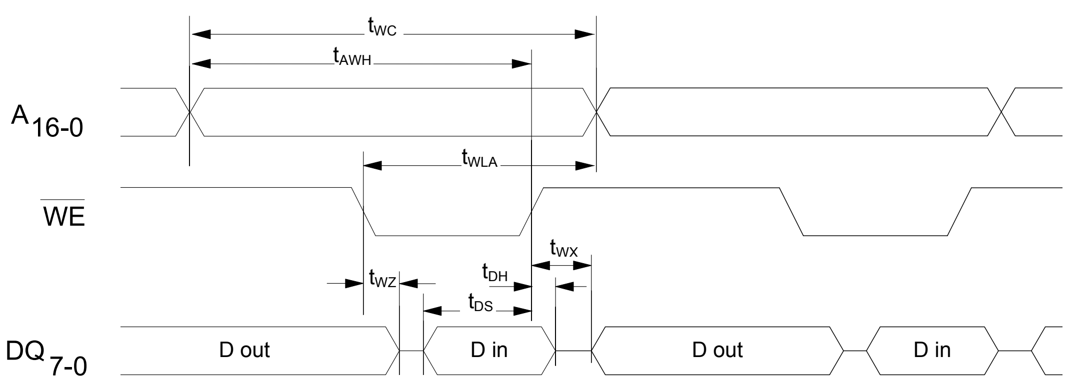


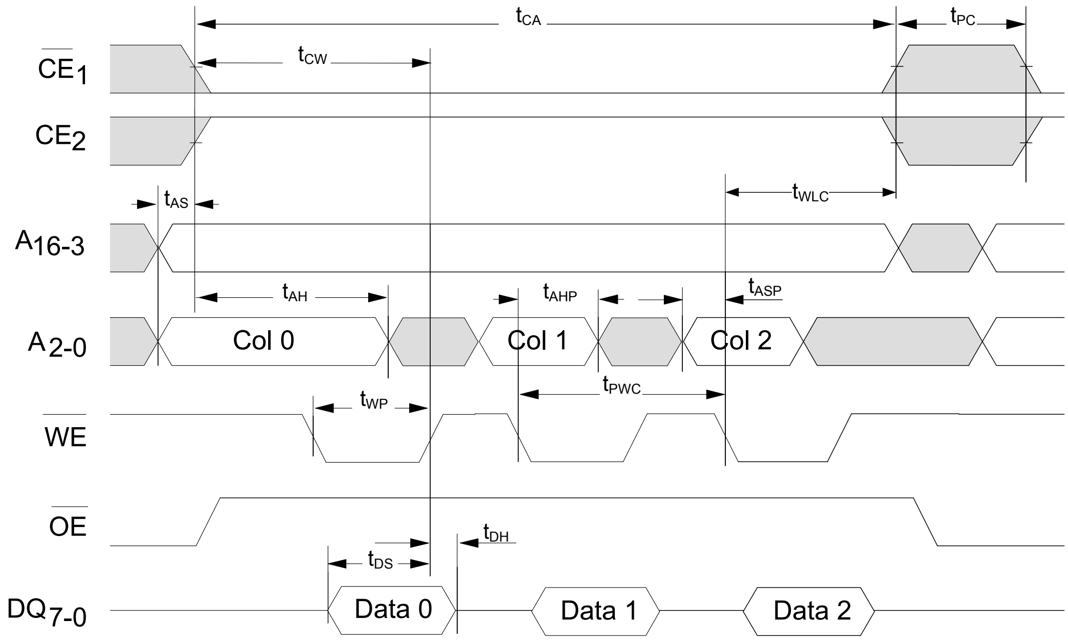
Figure 9. Write Cycle Timing 3 ($\overline{CE_1}$ LOW, CE_2 HIGH) [11]



Note

11. $\overline{OE}$ (not shown) is LOW only to show the effect of $\overline{WE}$ on DQ pins.

Figure 10. Page Mode Write Cycle Timing

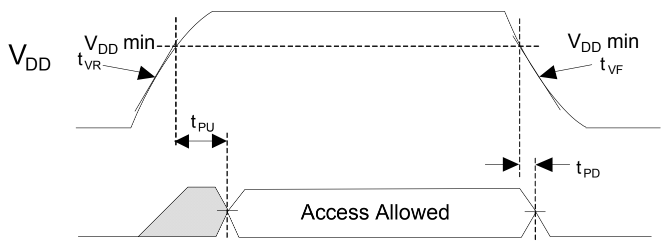


Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up (after V_{DD} min. is reached) to first access time	250	–	μs
t_{PD}	Last write ($\overline{WE}$ HIGH) to power down time	0	–	μs
t_{VR}[12]	V_{DD} power-up ramp rate	50	–	μs/V
t_{VF}[12]	V_{DD} power-down ramp rate	100	–	μs/V

Figure 11. Power Cycle Timing



Note
12. Slope measured at any point on the V_{DD} waveform.

Functional Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	A_{16}-A_3	A_2-A_0	Operation [13, 14]
H	X	X	X	X	Standby/Idle
X	L	X	X	X	
↓ L	H ↑	H H	V V	V V	Read
L	H	H	No Change	Change	Page Mode Read
L	H	H	Change	V	Random Read
↓ L	H ↑	L L	V V	V V	Chip Enable -Controlled Write[14]
L	H	↓	V	V	$\overline{WE}$-Controlled Write [14, 15]
L	H	↓	No Change	V	Page Mode Write [16]
↑ L	H ↓	X X	X X	X X	Starts pre-charge

Notes

13. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.
14. For write cycles, data-in is latched on the rising edge of $\overline{CE_1}$ or $\overline{WE}$ of the falling edge of CE_2, whichever comes first.
15. $\overline{WE}$-controlled write cycle begins as a Read cycle and then A_{16}-A_3 is latched.
16. Addresses A_2-A_0 must remain stable for at least 15 ns during page mode operation.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM28V100-TG	001-91156	32-pin TSOP I	Industrial
FM28V100-TGTR	001-91156	32-pin TSOP I	

All the above parts are Pb-free.

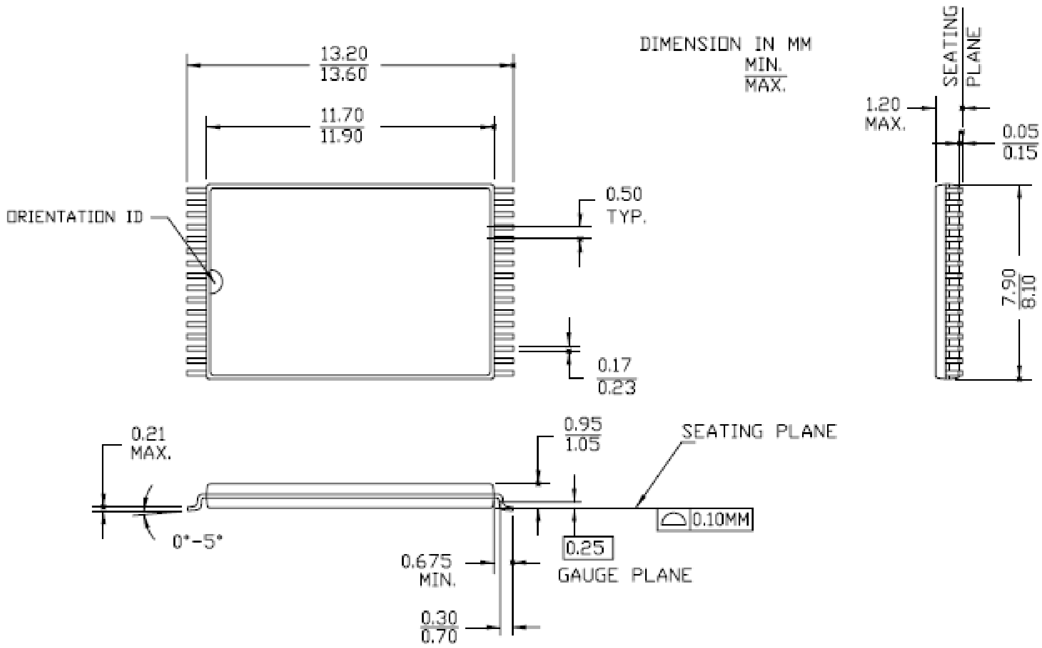
Ordering Code Definitions

FM 28 V 100 - TG TR

- Option: blank = Standard; TR = Tape and Reel
- Package Type: TG = 32-pin TSOP I
- Density: 100 = 1-Mbit
- Voltage: V = 2.0 V to 3.6 V
- Parallel F-RAM
- Cypress

Package Diagrams

Figure 12. 32-pin TSOP I Package Outline, 001-91156



001-91156 **

Acronyms

Acronym	Description
CPU	Central Processing Unit
CMOS	Complementary Metal Oxide Semiconductor
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
MCU	Microcontroller Unit
MPU	Microprocessor Unit
RoHS	Restriction of Hazardous Substances
R/W	Read and Write
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kiloohm
Mb	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
MΩ	megaohm
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM28V100, 1-Mbit (128 K × 8) F-RAM Memory Document Number: 001-86202				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3912933	GVCH	02/25/2013	New data sheet.
*A	4191946	GVCH	11/14/2013	Added watermark as "Not recommended for new designs."
*B	4274812	GVCH	03/11/2014	Converted to Cypress standard format Updated Maximum Ratings table - Removed Moisture Sensitivity Level (MSL) - Added junction temperature and latch up current Updated Data Retention and Endurance table Added Thermal Resistance table Removed Package Marking Scheme (top mark)
*C	4481463	GVCH	08/22/2014	Removed watermark as "Not recommended for new designs."
*D	4579647	GVCH	11/25/2014	Added related documentation hyperlink in page 1.
*E	4881722	ZSK / PSR	08/12/2015	Updated Maximum Ratings: Removed "Maximum junction temperature". Added "Maximum accumulated storage time". Added "Ambient temperature with power applied". Updated to new template.

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