EPC2036ENGRT – Enhancement Mode Power Transistor
Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS}, 100 V
- Maximum $R_{DS(on)}$, 73 mΩ
- I_D, 1 A

Applications:

- High Frequency DC-DC Conversion
- Wireless Power Transfer
- LiDAR/Pulsed Power Applications

EPC2036ENGRT eGaN® FETs are supplied in passivated die form with solder bumps.
Die Size: 0.9 mm x 0.9 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 125˚C)	120	
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$= 340 ˚C/W)	1.7	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	18	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V		20	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	0.9	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	250	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.6 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 1 A		62	73	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.9		V

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.5	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	65	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		75	90	pF
C_{OSS}	Output Capacitance			50	75	
C_{RSS}	Reverse Transfer Capacitance			0.7	1.1	
R_G	Gate Resistance			0.6		O
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D=1 A		700	910	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 1 A		170		
Q_{GD}	Gate-to-Drain Charge			140	240	
$Q_{G(TH)}$	Gate Charge at Threshold			120		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		3900	5900	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

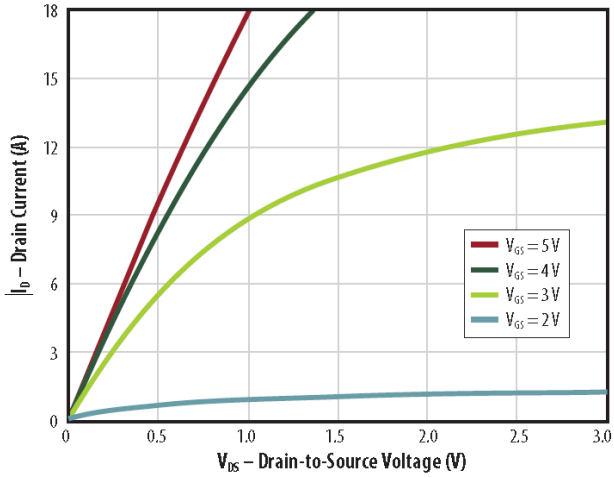


Figure 2: Transfer Characteristics

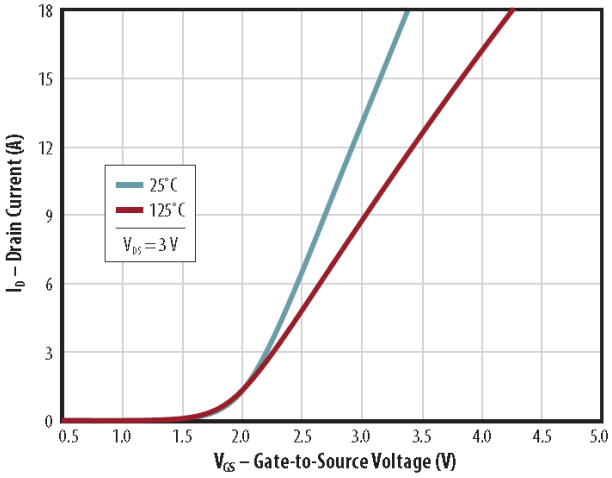


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

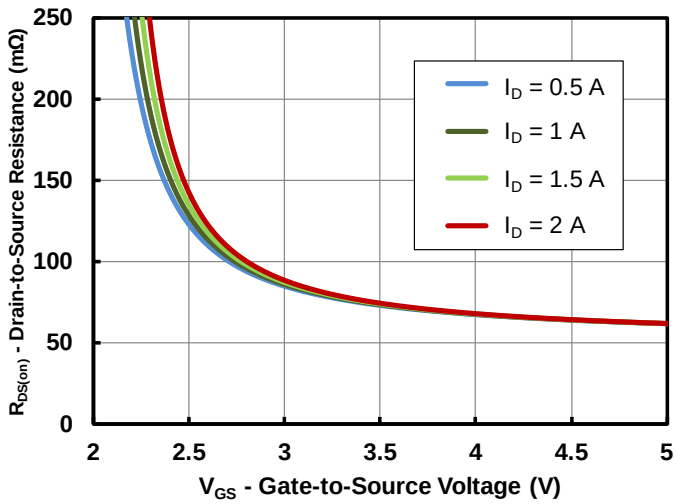


Figure 4: $R_{DS(on)}$ vs VGS for Various Temperatures

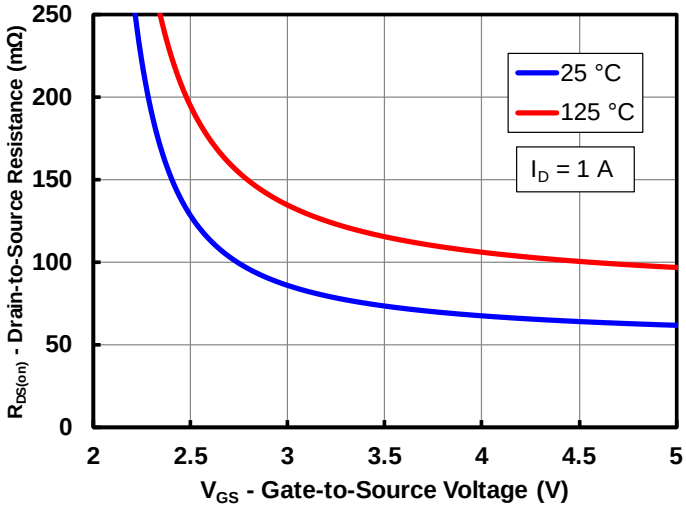


Figure 5a: Capacitance (Linear Scale)

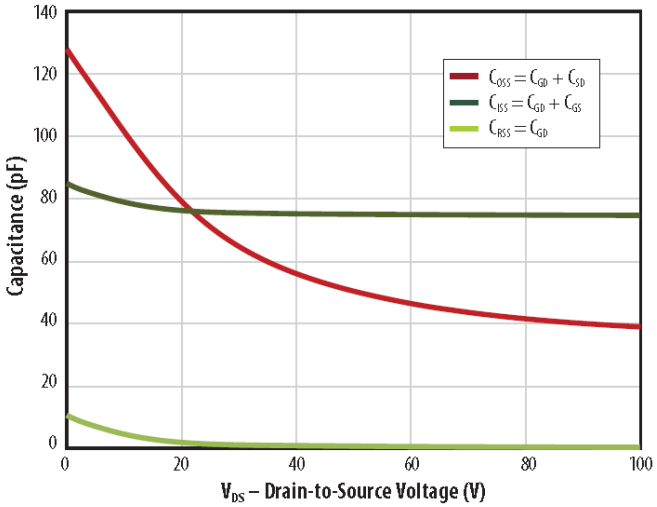


Figure 5b: Capacitance (Log Scale)

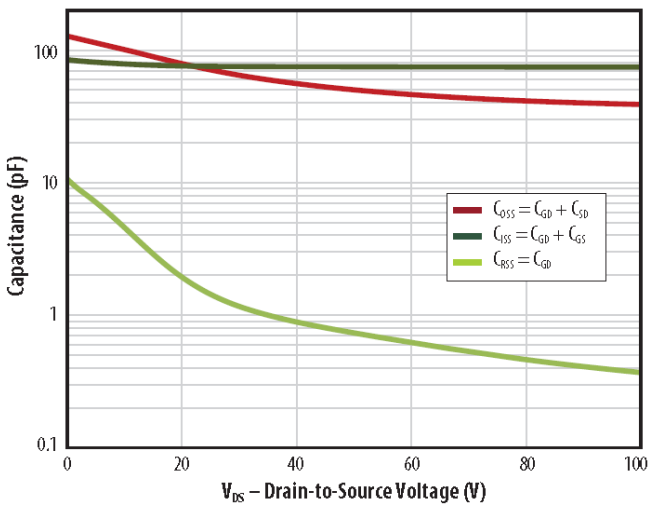


Figure 6: Gate Charge

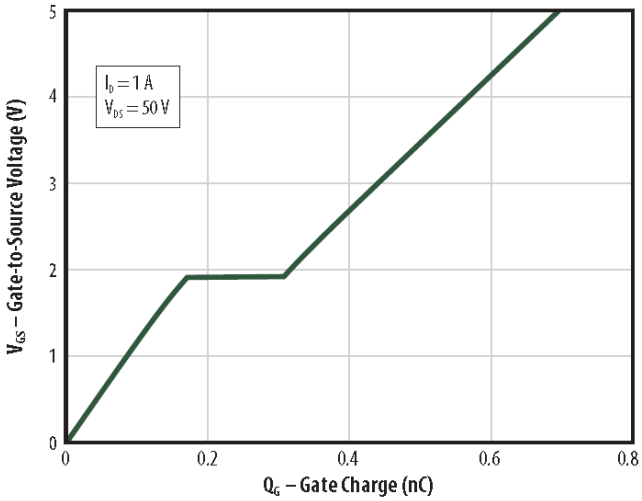


Figure 7: Reverse Drain-Source Characteristics

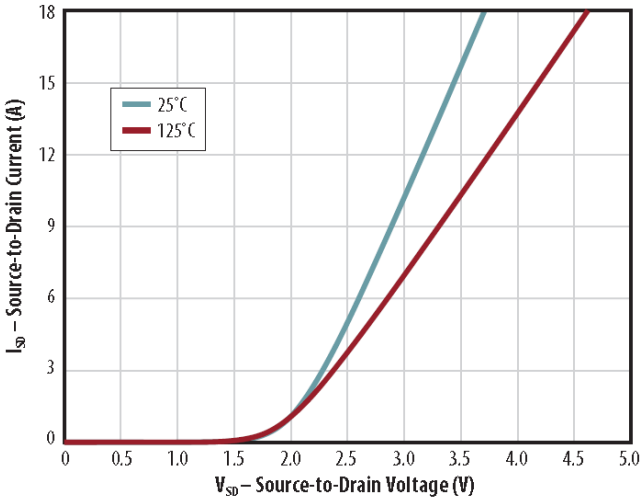


Figure 8: Normalized On Resistance vs. Temperature

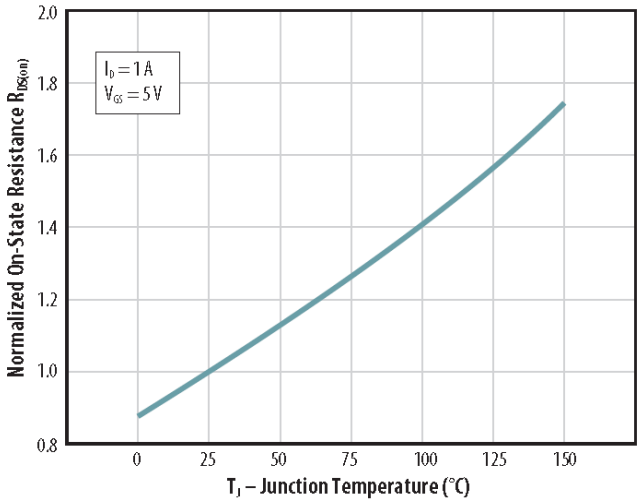


Figure 9: Normalized Threshold Voltage vs. Temperature

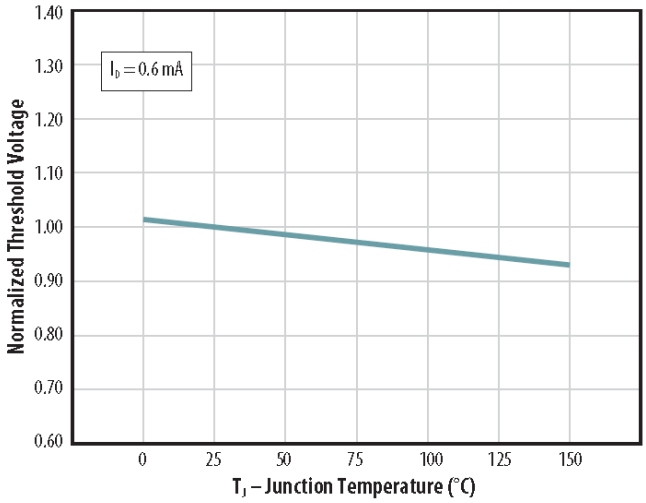


Figure 10: Gate Leakage Current

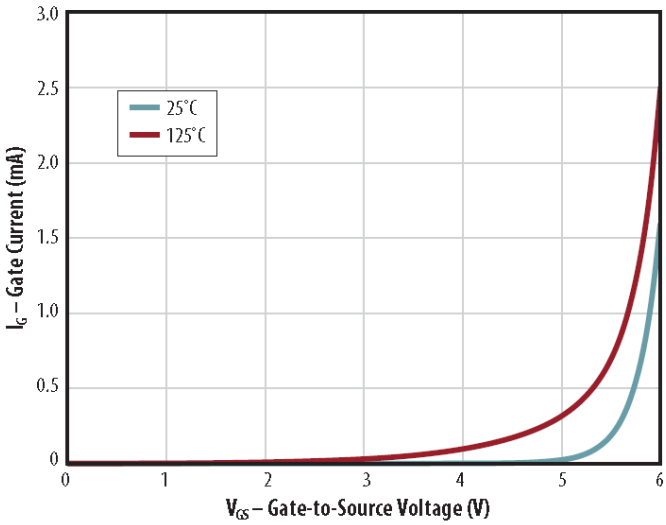


Figure 11: Transient Thermal Response Curves

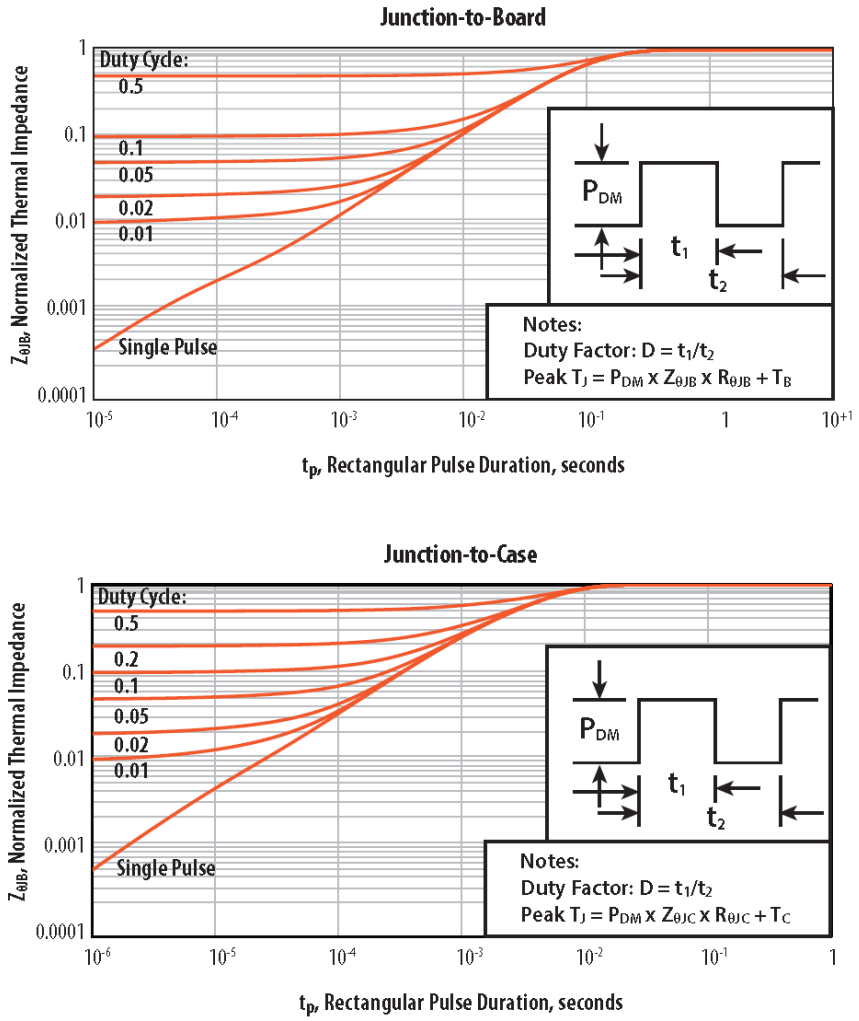
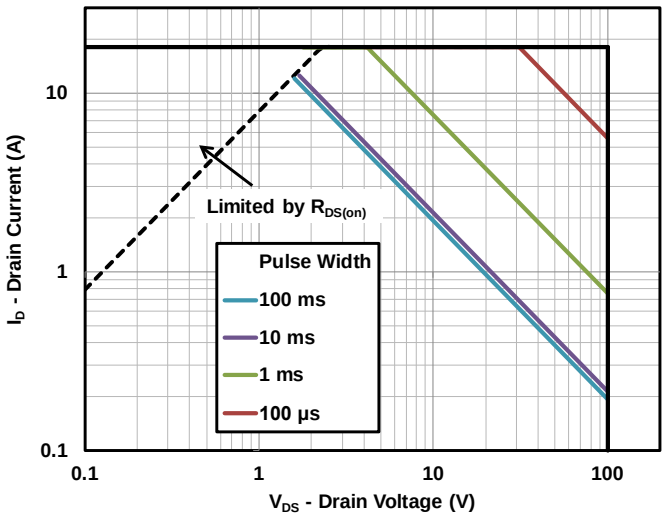
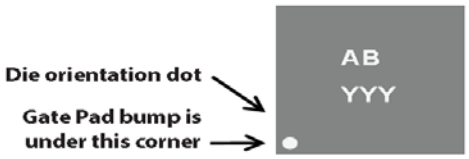


Figure 12: Safe Operating Area



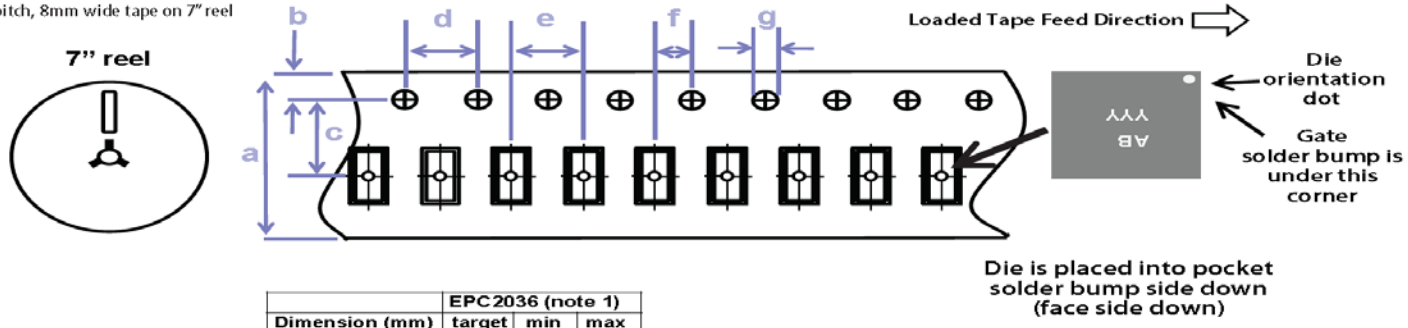
DIE MARKINGS



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking line 2
EPC2036	AB	YYY

TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

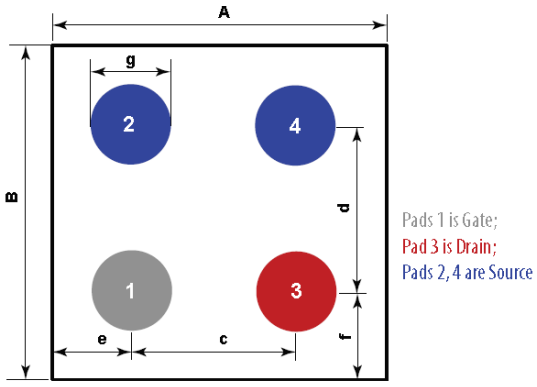


	EPC2036 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

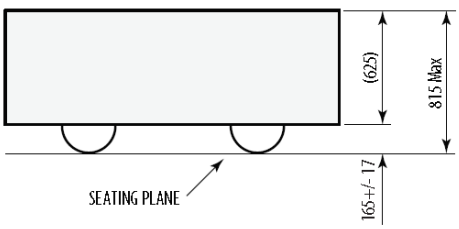
DIE OUTLINE

Solder Bump View



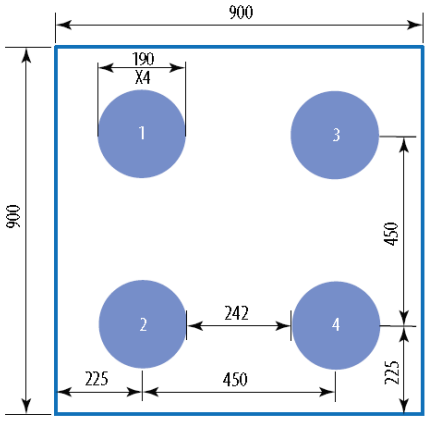
DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined
Solder mask is 10µm smaller per side than bump

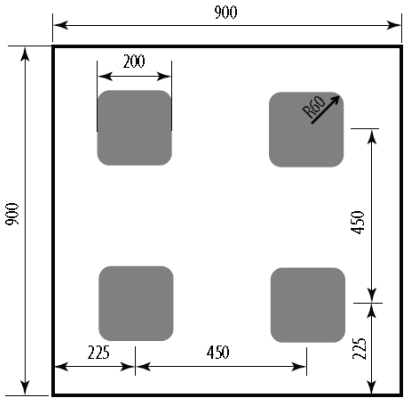
Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised November, 2016